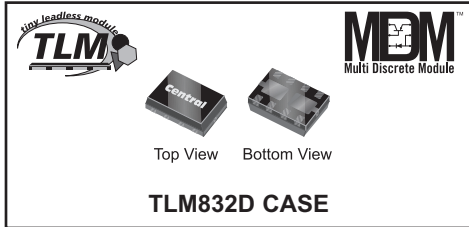


**CTLM8110-M832D**  
**MULTI DISCRETE MODULE™**  
**SURFACE MOUNT P-CHANNEL**  
**ENHANCEMENT-MODE SILICON MOSFET**  
**AND**  
**LOW V<sub>F</sub> SILICON SCHOTTKY RECTIFIER**



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• Device is **Halogen Free** by design

**APPLICATIONS**

- Load Power Switches
- DC - DC Converters
- LCD Backlighting
- Battery powered portable devices including Cell Phones, Digital Cameras, Pagers, PDAs, Notebook PCs, etc.

**MAXIMUM RATINGS - CASE:** (T<sub>A</sub>=25°C)

Power Dissipation (Note 1)  
 Operating and Storage Junction Temperature  
 Thermal Resistance

**MAXIMUM RATINGS - Q1:** (T<sub>A</sub>=25°C)

Drain-Source Voltage  
 Gate-Source Voltage  
 Continuous Drain Current (Steady State)  
 Continuous Drain Current, t<sub>p</sub>≤5.0s  
 Continuous Source Current (Body Diode)  
 Maximum Pulsed Drain Current, t<sub>p</sub>=10μs  
 Maximum Pulsed Source Current, t<sub>p</sub>=10μs

**MAXIMUM RATINGS - D1:** (T<sub>A</sub>=25°C)

Peak Repetitive Reverse Voltage  
 Continuous Forward Current  
 Peak Repetitive Forward Current, t<sub>p</sub>≤1.0ms  
 Peak Forward Surge Current, t<sub>p</sub>=8.0ms

**ELECTRICAL CHARACTERISTICS - Q1:** (T<sub>A</sub>=25°C unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
I <sub>GSSF</sub> , I <sub>GSSR</sub>	V <sub>GS</sub> =8.0V, V <sub>DS</sub> =0		1.0	50	nA
I <sub>DSS</sub>	V <sub>DS</sub> =20V, V <sub>GS</sub> =0		5.0	500	nA
BV <sub>DSS</sub>	V <sub>GS</sub> =0, I <sub>D</sub> =250μA	20	24		V
V <sub>GS(th)</sub>	V <sub>DS</sub> =V <sub>GS</sub> , I <sub>D</sub> =250μA	0.45	0.76	1.0	V
V <sub>SD</sub>	V <sub>GS</sub> =0, I <sub>S</sub> =360mA			0.9	V
r <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.95A		0.085	0.15	Ω
r <sub>DS(ON)</sub>	V <sub>GS</sub> =4.5V, I <sub>D</sub> =0.77A		0.085	0.142	Ω
r <sub>DS(ON)</sub>	V <sub>GS</sub> =2.5V, I <sub>D</sub> =0.67A		0.13	0.2	Ω
r <sub>DS(ON)</sub>	V <sub>GS</sub> =1.8V, I <sub>D</sub> =0.2A		0.19	0.24	Ω
g <sub>FS</sub>	V <sub>DS</sub> =10V, I <sub>D</sub> =0.81A		2.0		S

Notes: (1) FR-4 Epoxy PCB with copper mounting pad area of 54mm<sup>2</sup>.

**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLM8110-M832D consists of an P-Channel Enhancement-mode MOSFET and a Low V<sub>F</sub> Schottky Rectifier. Packaged in a small, thermally efficient, leadless 3x2mm surface mount case, it is designed for applications where small size, operational efficiency, and low energy consumption are the prime requirements.

**MARKING CODE: CFR**

**FEATURES**

- Dual Chip Device
- High Current (0.95A) MOSFET and 1.0A Schottky Rectifier
- Low r<sub>DS(ON)</sub>: 0.24Ω MAX @ V<sub>GS</sub>=1.8V
- Low V<sub>F</sub> Schottky Rectifier (550mV @ 1.0A MAX)
- Small TLM 3x2mm Leadless Surface Mount Package
- Complementary Device: CTLM7110-M832D

**SYMBOL**

SYMBOL	UNITS
P <sub>D</sub>	1.65 W
T <sub>J</sub> , T <sub>stg</sub>	-65 to +150 °C
θ <sub>JA</sub>	76 °C/W
V <sub>DS</sub>	20 V
V <sub>GS</sub>	8.0 V
I <sub>D</sub>	0.86 A
I <sub>D</sub>	0.95 A
I <sub>S</sub>	0.36 A
I <sub>DM</sub>	4.0 A
I <sub>SM</sub>	4.0 A
V <sub>R</sub> RM	40 V
I <sub>F</sub>	1.0 A
I <sub>FRM</sub>	3.5 A
I <sub>FSM</sub>	10 A

R2 (2-August 2011)

**CTLM8110-M832D**  
**MULTI DISCRETE MODULE™**  
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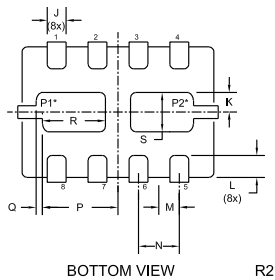
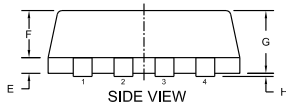
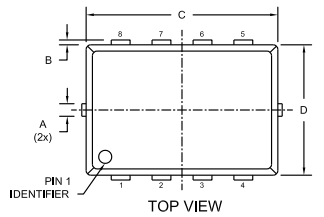
**ELECTRICAL CHARACTERISTICS - Q1 - Continued:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$Q_{g(\text{tot})}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		3.56		nC
$Q_{gs}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		0.36		nC
$Q_{gd}$	$V_{DS}=10\text{V}, V_{GS}=4.5\text{V}, I_D=1.0\text{A}$		1.52		nC
$C_{rss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		80		pF
$C_{iss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		200		pF
$C_{oss}$	$V_{DS}=16\text{V}, V_{GS}=0, f=1.0\text{MHz}$		60		pF
$t_{on}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=0.95\text{A}, R_G=6.0\Omega$		20		ns
$t_{off}$	$V_{DD}=10\text{V}, V_{GS}=4.5\text{V}, I_D=0.95\text{A}, R_G=6.0\Omega$		25		ns

**ELECTRICAL CHARACTERISTICS - D1:** ( $T_A=25^\circ\text{C}$ )

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_R$	$V_R=5.0\text{V}$			10	$\mu\text{A}$
$I_R$	$V_R=8.0\text{V}$			20	$\mu\text{A}$
$I_R$	$V_R=15\text{V}$			50	$\mu\text{A}$
$BV_R$	$I_R=100\mu\text{A}$	40			V
$V_F$	$I_F=10\text{mA}$			0.29	V
$V_F$	$I_F=100\text{mA}$			0.36	V
$V_F$	$I_F=500\text{mA}$			0.45	V
$V_F$	$I_F=1.0\text{A}$			0.55	V
$C_J$	$V_R=4.0\text{V}, f=1.0\text{MHz}$		50		pF

**TLM832D CASE - MECHANICAL OUTLINE**

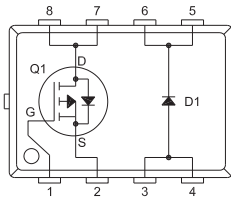


\* Note:  
 - Exposed pad P1 common to pins 7 and 8  
 - Exposed pad P2 common to pins 5 and 6

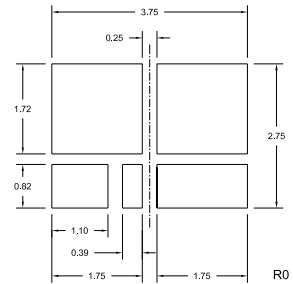
SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.007	0.012	0.170	0.300
B	-	0.005	-	0.125
C	0.114	0.122	2.900	3.100
D	0.075	0.083	1.900	2.100
E	0.006	0.010	0.150	0.250
F	0.026	0.030	0.650	0.750
G	0.031	0.039	0.800	1.000
H	0.000	0.002	0.000	0.050
J	0.009	0.013	0.240	0.340
K	0.006	0.014	0.160	0.360
L	0.008	0.018	0.200	0.450
M		0.013		0.325
N		0.026		0.650
P	0.040	0.048	1.010	1.210
Q		0.004		0.100
R	0.032	0.040	0.820	1.020
S	0.017	0.025	0.430	0.630

TLM832D (REV: R2)

**PIN CONFIGURATION**



**SUGGESTED MOUNTING PADS**  
 For Maximum Power Dissipation  
 (Dimensions in mm)



For standard mounting refer to TLM832D Package Details

**LEAD CODE:**

- 1) Gate Q1      5) Cathode D1
- 2) Source Q1    6) Cathode D1
- 3) Anode D1     7) Drain Q1
- 4) Anode D1     8) Drain Q1

**MARKING CODE: CFR**

R2 (2-August 2011)