

**CWDM305ND****SURFACE MOUNT  
DUAL N-CHANNEL  
ENHANCEMENT-MODE  
SILICON MOSFET****SOIC-8 CASE**[www.centrasemi.com](http://www.centrasemi.com)**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CWDM305ND is a dual, high current N-channel enhancement-mode silicon MOSFET designed for high speed pulsed amplifier and driver applications. This energy efficient MOSFET offers beneficially low  $r_{DS(ON)}$ , low gate charge, and low threshold voltage.

**MARKING CODE: C305****APPLICATIONS:**

- Load/Power switches
- DC-DC converter circuits
- Power management

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Drain-Source Voltage
Gate-Source Voltage
Continuous Drain Current (Steady State)
Maximum Pulsed Drain Current, $t_p=10\mu\text{s}$
Power Dissipation
Operating and Storage Junction Temperature
Thermal Resistance

**FEATURES:**

- Low  $r_{DS(ON)}$
- High current
- Low gate charge

SYMBOL		UNITS
$V_{DS}$	30	V
$V_{GS}$	20	V
$I_D$	5.8	A
$I_{DM}$	23.2	A
$P_D$	2.0	W
$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$
$\theta_{JA}$	62.5	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

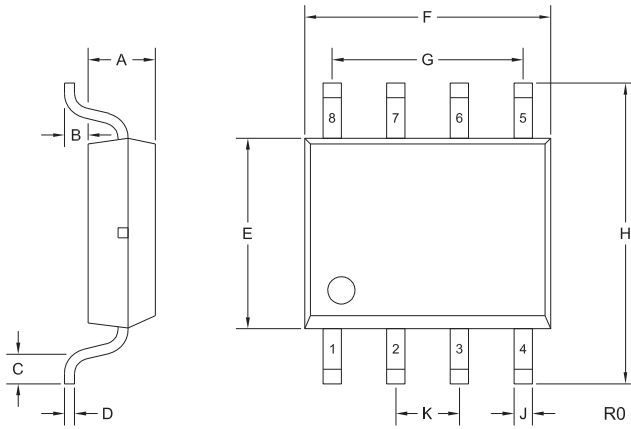
SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{GSSF}, I_{GSSR}$	$V_{GS}=20\text{V}, V_{DS}=0$			100	nA
$I_{DSS}$	$V_{DS}=30\text{V}, V_{GS}=0$			1.0	$\mu\text{A}$
$BV_{DSS}$	$V_{GS}=0, I_D=250\mu\text{A}$	30			V
$V_{GS(th)}$	$V_{GS}=V_{DS}, I_D=250\mu\text{A}$	1.0		3.0	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=2.9\text{A}$		0.024	0.030	$\Omega$
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=2.9\text{A}$		0.028	0.034	$\Omega$
$g_{FS}$	$V_{DS}=5.0\text{V}, I_D=5.8\text{A}$		12		S
$C_{rss}$	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		50	54	pF
$C_{iss}$	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		500	560	pF
$C_{oss}$	$V_{DS}=10\text{V}, V_{GS}=0, f=1.0\text{MHz}$		52	90	pF
$Q_g(tot)$	$V_{DD}=15\text{V}, V_{GS}=5.0\text{V}, I_D=5.8\text{A}$		4.2	6.3	nC
$Q_{gs}$	$V_{DD}=15\text{V}, V_{GS}=5.0\text{V}, I_D=5.8\text{A}$		0.9	1.4	nC
$Q_{gd}$	$V_{DD}=15\text{V}, V_{GS}=5.0\text{V}, I_D=5.8\text{A}$		1.4	2.1	nC
$t_{on}$	$V_{DD}=15\text{V}, I_D=5.8\text{A}, R_G=10\Omega$		6.5		ns
$t_{off}$	$V_{DD}=15\text{V}, I_D=5.8\text{A}, R_G=10\Omega$		8.5		ns

R3 (1-November 2012)

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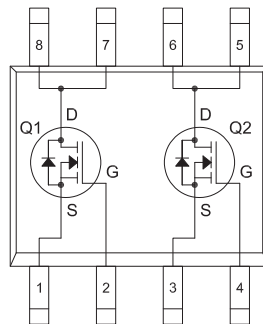
**SOIC-8 CASE - MECHANICAL OUTLINE**



SYMBOL	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.049	0.057	1.24	1.44
B	0.000	0.011	0.00	0.27
C	0.018	-	0.46	-
D	0.006	0.011	0.16	0.27
E	0.145	0.154	3.70	3.90
F	0.189	0.198	4.81	5.01
G	0.150		3.81	
H	0.231	0.244	5.88	6.18
J	0.013	0.021	0.35	0.52
K	0.050		1.27	

SOIC-8 (REV: R0)

**PIN CONFIGURATION**



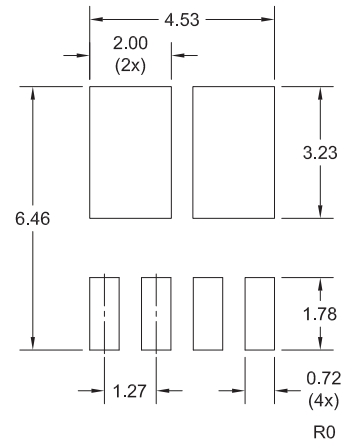
**LEAD CODE:**

- |              |             |
|--------------|-------------|
| 1) Source Q1 | 5) Drain Q2 |
| 2) Gate Q1   | 6) Drain Q2 |
| 3) Source Q2 | 7) Drain Q1 |
| 4) Gate Q2   | 8) Drain Q1 |

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**SUGGESTED MOUNTING PADS**

(Dimensions in mm)



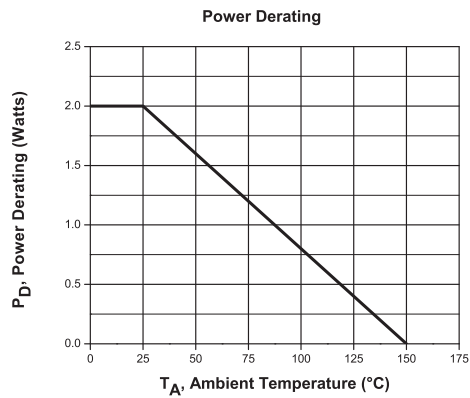
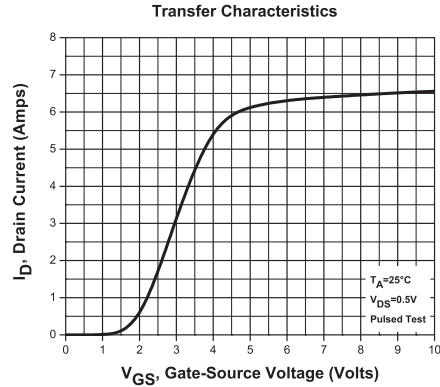
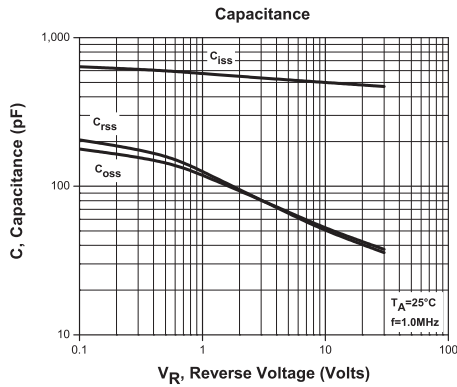
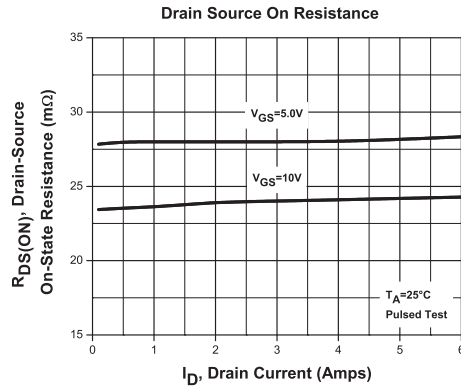
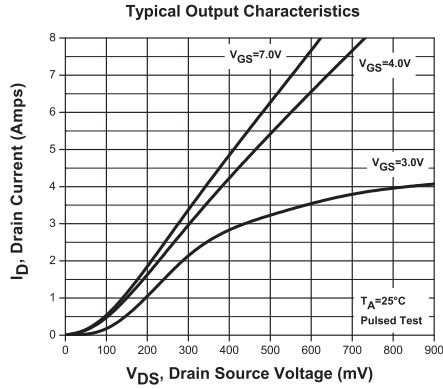
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**TYPICAL ELECTRICAL CHARACTERISTICS**



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