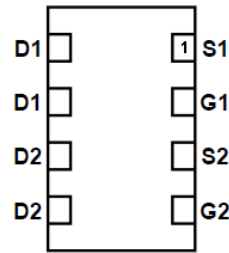
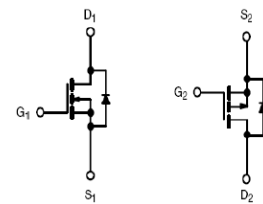


Main Product Characteristics:

	NMOS	PMOS
V_{DSS}	30V	-30V
$R_{DS(on)}$	32.4mohm	61.6mohm
I_D	4A	-3.6A


**DFN 3x2-8L
Bottom View**

**N-Channel Mosfet P-Channel Mosfet
Schematic diagram**
Features and Benefits:

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150°C operating temperature


Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.		Units
		N-Channel	P-Channel	
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	4 ①	-3.6 ①	A
I_{DM}	Pulsed Drain Current ②	16	-14.4	
V_{GS}	Gate to source voltage	± 12	± 12	V
$P_D @ TC = 25^\circ C$	Power Dissipation ③	2.1	1.3	W
$T_J T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 150	-55 to + 150	$^\circ C$

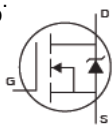
Thermal Resistance

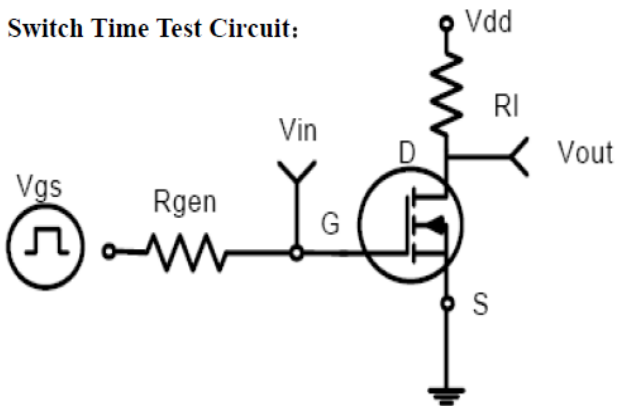
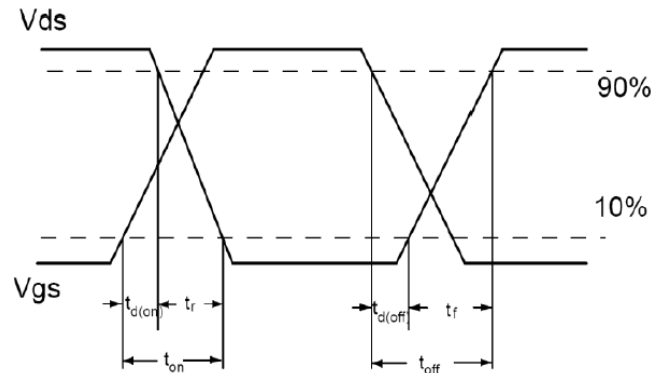
Symbol	Characterizes	Typ.	Max.		Units
			N-channel	P-Channel	
$R_{\theta JA}$	Junction-to-ambient ($t \leq 5s$) ④	—	60	95	$^\circ C/W$

Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

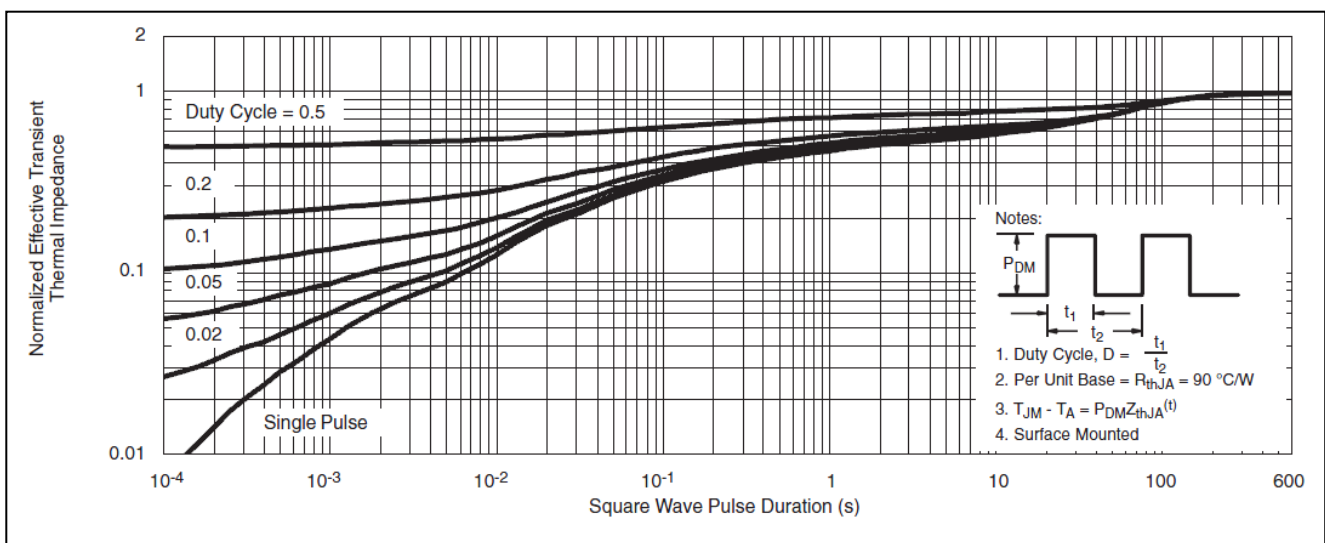
Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	N-channel	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Channel	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	N-channel	—	32.4	36	m Ω	$V_{GS} = 4.5V, I_D = 4.8A$
		P-Channel	—	61.6	65		$V_{GS} = -4.5V, I_D = -2.3A$
$V_{GS(th)}$	Gate threshold voltage	N-channel	0.5	—	2	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Channel	-0.5	—	-2		$V_{DS} = V_{GS}, I_D = -250\mu A$
I_{DSS}	Drain-to-Source leakage current	N-channel	—	—	1	μA	$V_{DS} = 30V, V_{GS} = 0V$
		P-Channel	—	—	-1		$V_{DS} = -30V, V_{GS} = 0V$
I_{GSS}	Gate-to-Source forward leakage	N-channel	—	—	100	nA	$V_{GS} = 12V$
		N-channel	-100	—	—		$V_{GS} = -12V$
		P-Channel	—	—	100		$V_{GS} = 12V$
		P-Channel	-100	—	—		$V_{GS} = -12V$

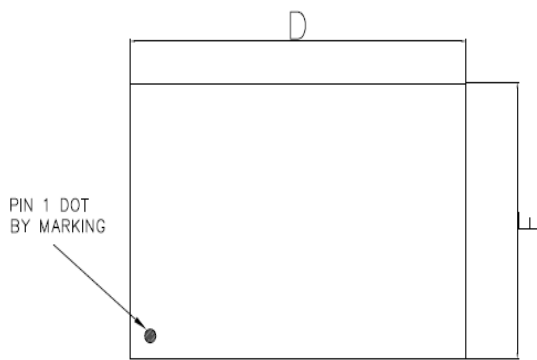
Source-Drain Ratings and Characteristics

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	N-channel	—	—	4	A	MOSFET symbol showing the integral reverse p-n junction diode. 
		P-Channel	—	—	-3.6		
I_{SM}	Pulsed Source Current	N-channel	—	—	16	A	
		P-Channel	—	—	-14.4		
V_{SD}	Diode Forward Voltage	N-channel	—	0.82	1.2	V	$I_S = 2.4A, V_{GS} = 0V$
		P-Channel	—	-0.85	-1.2		$I_S = -1.5A, V_{GS} = 0V$

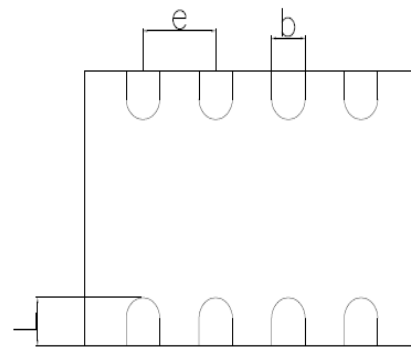
Test circuits and Waveforms:
Switch Time Test Circuit:

Switching time waveform:

Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of R_{θJA} is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A = 25°C

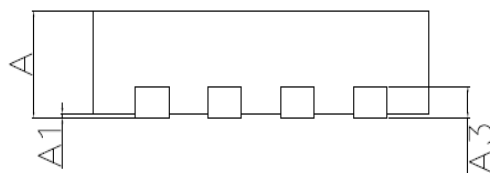
Thermal characteristics

Figure1. Normalized Thermal Transient Impedance, Junction-to-Ambient

Mechanical Data:
DFN 3X2_8L PACKAGE OUTLINE DIMENSION


TOP VIEW



BOTTOM VIEW



SIDE VIEW

Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.700	0.750	0.800	0.028	0.030	0.031
A1	0.000	-	0.050	0.000	-	0.002
A3	0.200REF			0.008REF		
D	2.950	3.000	3.050	0.116	0.118	0.120
E	1.950	2.000	2.050	0.077	0.079	0.081
b	0.250	0.300	0.350	0.010	0.012	0.014
L	0.280	0.350	0.420	0.016	0.014	0.017
e	0.650BSC			0.026BSC		

Ordering and Marking Information
Device Marking: 3036C

Package (Available)
DFN 3x2-8L
Operating Temperature Range
C : -55 to 150 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
DFN 3x2-8L	3000pcs	10pcs	30000pcs	4pcs	120000pcs

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 150°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

ATTENTION:

- Any and all Silikron products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your Silikron representative nearest you before using any Silikron products described or contained herein in such applications.
- Silikron assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all Silikron products described or contained herein.
- Specifications of any and all Silikron products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- Silikron Semiconductor CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all Silikron products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of Silikron Semiconductor CO.,LTD.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. Silikron believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the Silikron product that you intend to use.
- This catalog provides information as of Dec, 2008. Specifications and information herein are subject to change without notice.

Customer Service**Worldwide Sales and Service:**

Sales@silikron.com

Technical Support:

Technical@silikron.com

Suzhou Silikron Semiconductor Corp.

Building 11A Suchun Industrial Square, 428# Xinglong Street, Suzhou P.R. China

TEL: (86-512) 62560688

FAX: (86-512) 65160705

E-mail: Sales@silikron.com