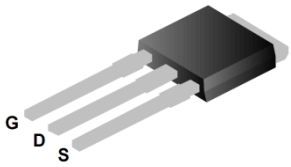
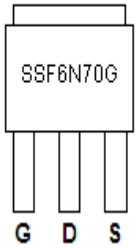
Main Product Characteristics:

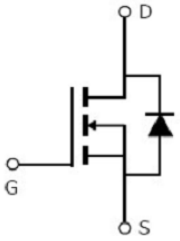
V_{DSS}	700V
R_{DS}(on)	1.49Ω (typ.)
I_D	6A



TO-251



Marking and pin Assignment



Schematic diagram

Features and Benefits:

- Advanced MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 150℃ operating temperature

Description:

It utilizes the latest processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications.

Absolute max Rating:

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V①	6	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V①	3.8	
I_{DM}	Pulsed Drain Current②	24	
P_D @TC = 25°C	Power Dissipation③	113	W
	Linear Derating Factor	0.91	W/°C
V_{DS}	Drain-Source Voltage	700	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=20mH	313	mJ
I_{AS}	Avalanche Current @ L=20mH	5.6	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

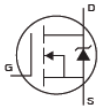
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case③	—	1.1	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	110	℃/W

Electrical Characterizes @T_A=25℃ unless otherwise specified

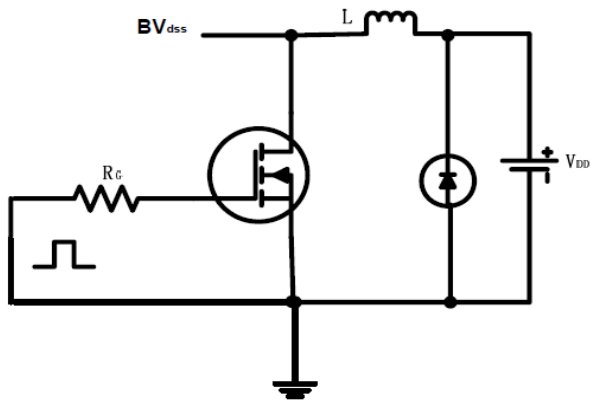
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	700	—	—	V	V_{GS} = 0V, ID = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	1.49	1.7	Ω	V_{GS}=10V,I_D = 3A
		—	3.12	—		T_J = 125℃
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	2.0	—		T_J = 125℃
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 700V,V_{GS} = 0V
		—	—	50		T_J = 125℃
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} =30V
		—	—	-100		V_{GS} = -30V
Q_g	Total gate charge	—	16	—	nC	I_D = 6A,
Q_{gs}	Gate-to-Source charge	—	5.5	—		V_{DS}=400V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	4.6	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	15	—	ns	V_{GS}=10V, VDS=350V, R_{GEN}=25Ω,ID=6A
t_r	Rise time	—	20	—		
$t_{d(off)}$	Turn-Off delay time	—	41	—		
t_f	Fall time	—	24	—		
C_{iss}	Input capacitance	—	881	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	91	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	1.6	—		f = 1MHz

Source-Drain Ratings and Characteristics

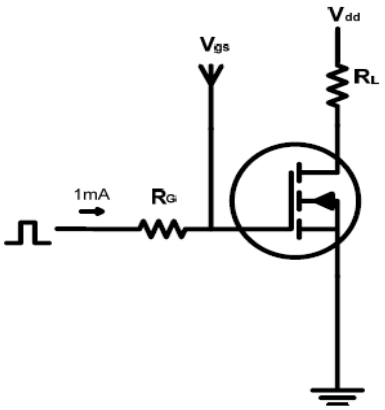
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	6	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	24	A	
V_{sd}	Diode Forward Voltage	—	0.86	1.4	V	I_S=6A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	589	—	ns	T_J = 25°C, I_F =6A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	3.7	—	μC	

Test circuits and Waveforms

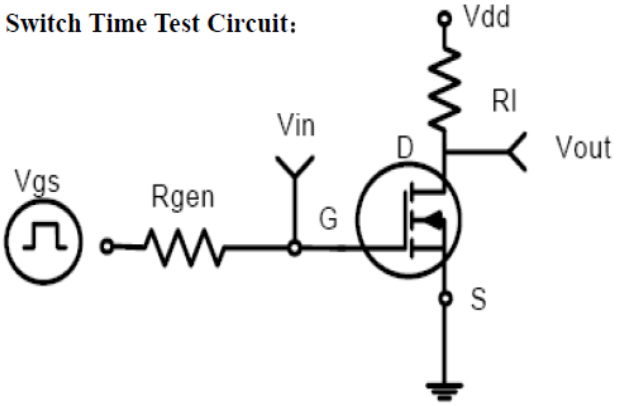
EAS test circuits:



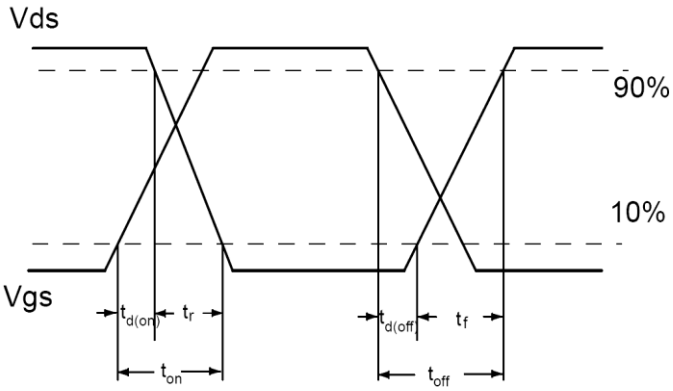
Gate charge test circuit:



Switch Time Test Circuit:



Switch Waveforms:



Notes:

①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical electrical and thermal characteristics

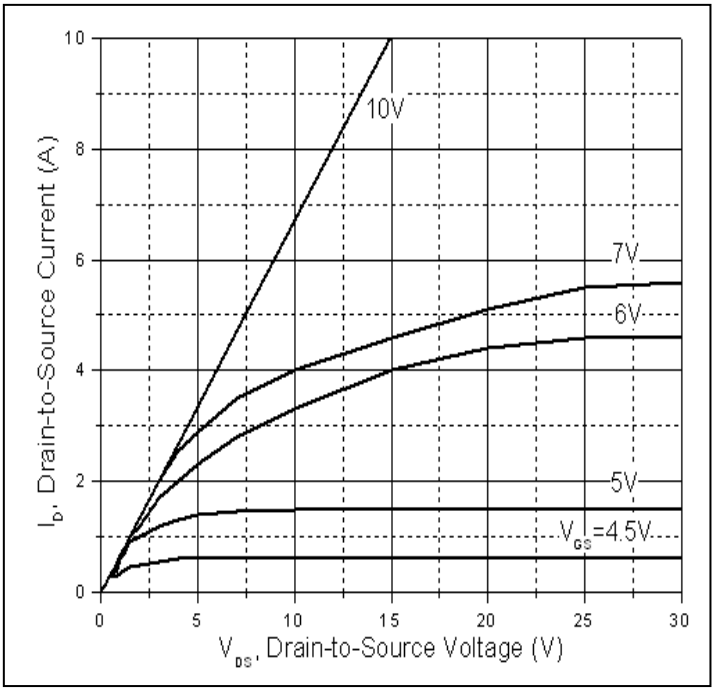


Figure 1: Typical Output Characteristics

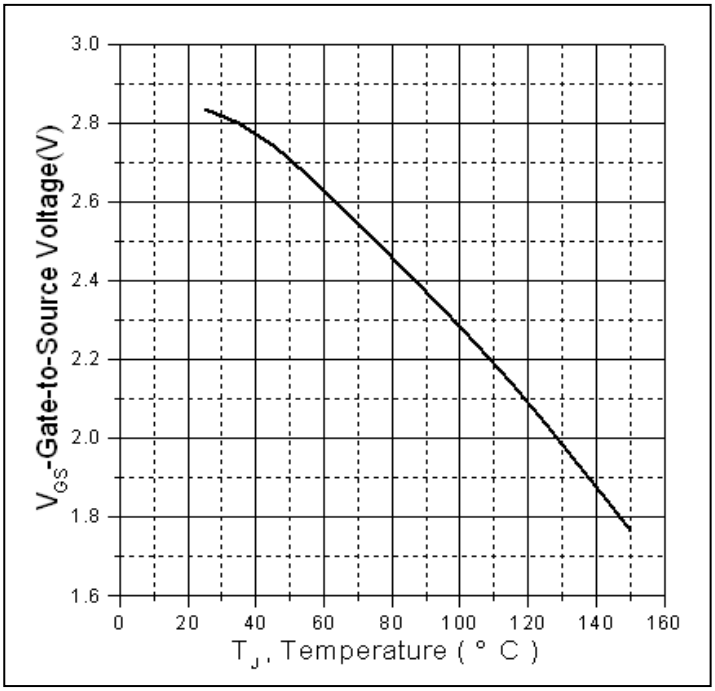


Figure 2. Gate to source cut-off voltage

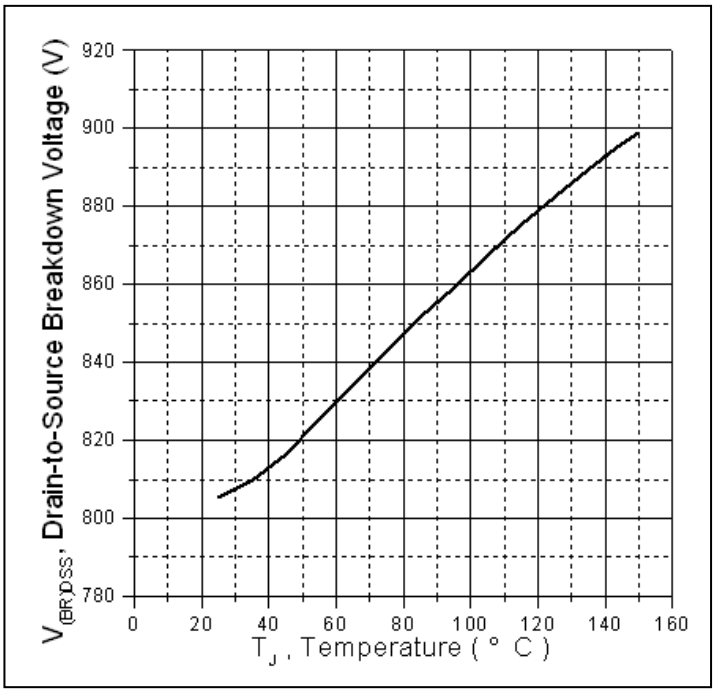


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

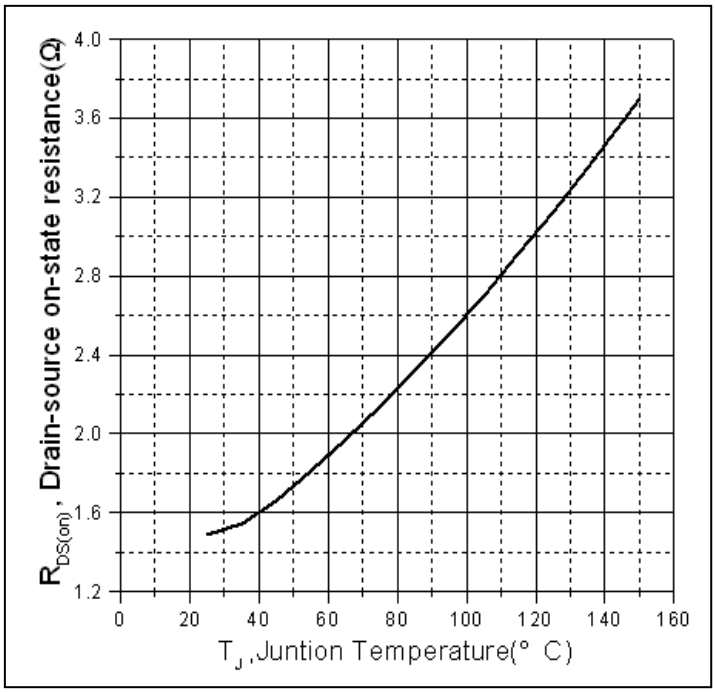


Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

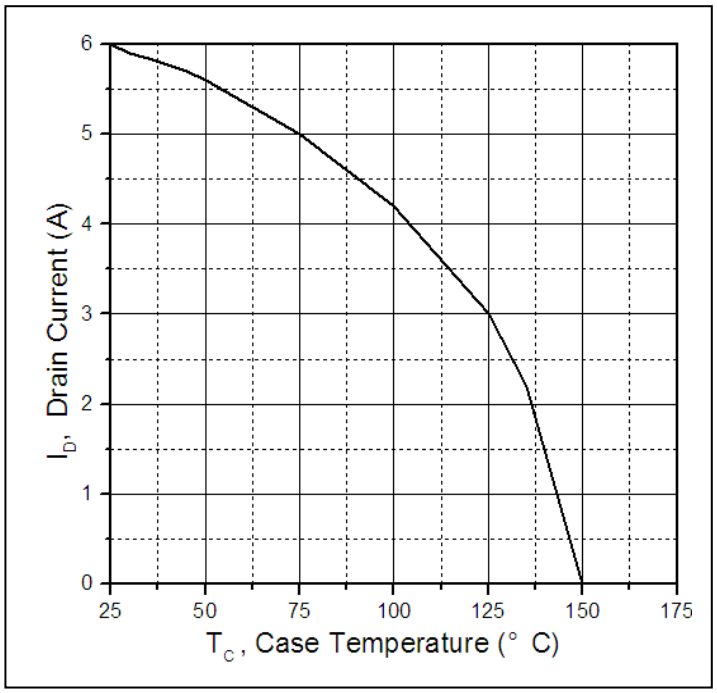


Figure 5. Maximum Drain Current Vs. Case Temperature

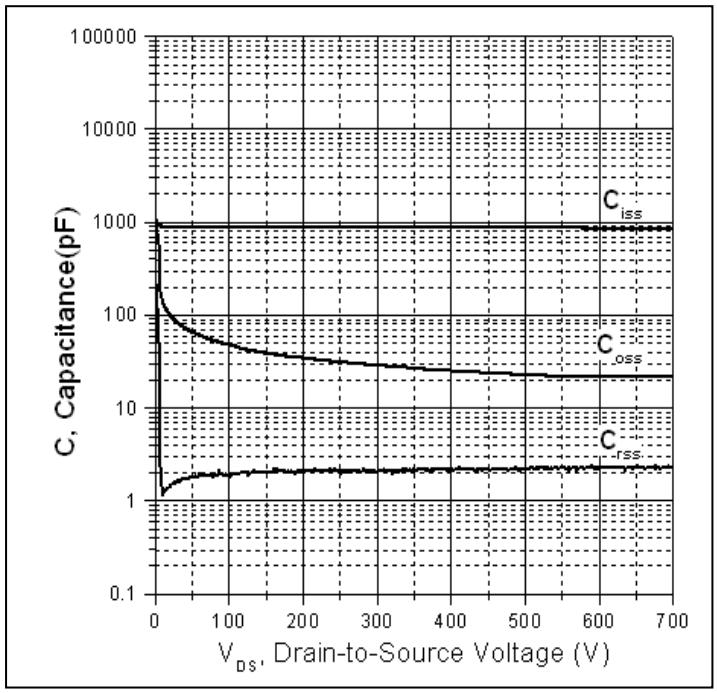


Figure 6.Typical Capacitance Vs. Drain-to-Source Voltage

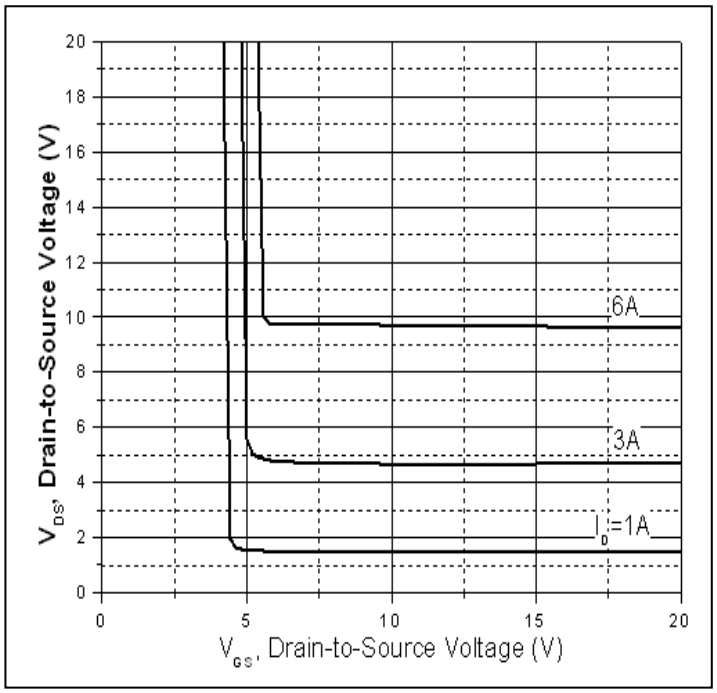


Figure7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

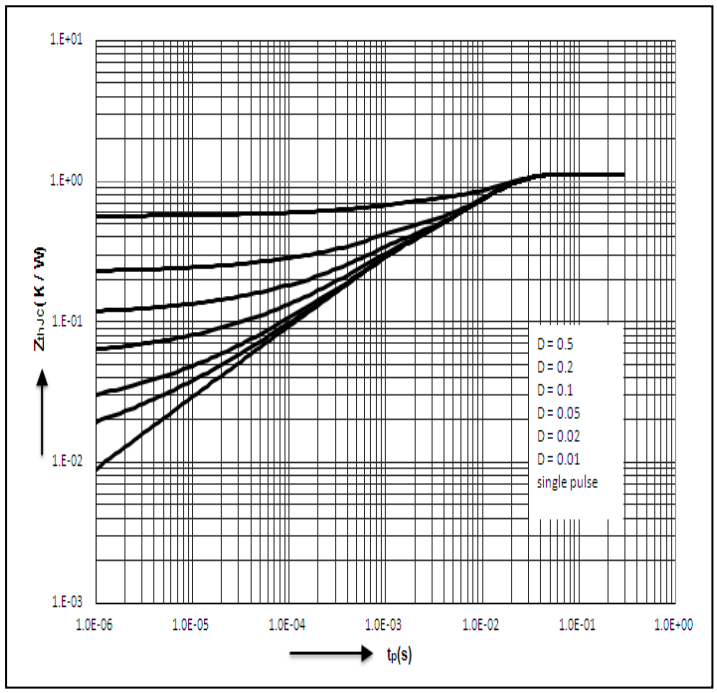
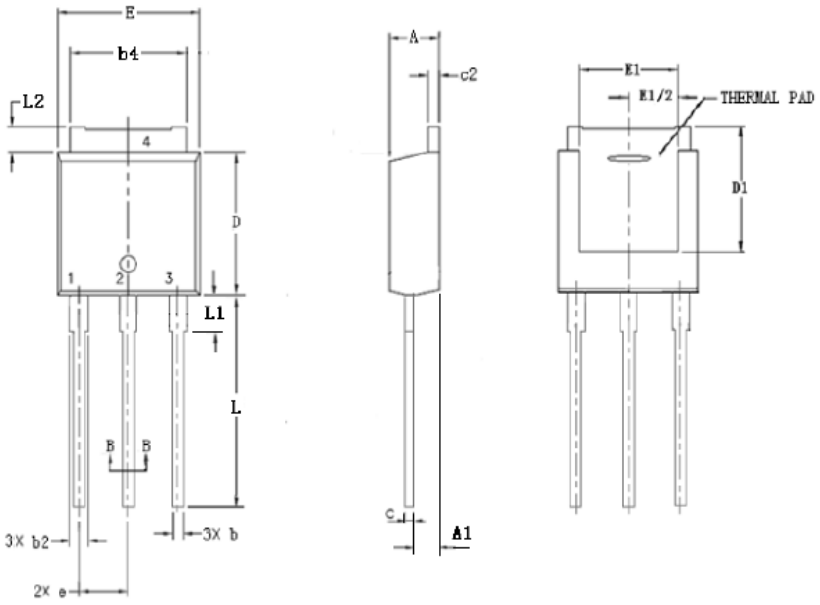


Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data：

TO-251 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.220	-	2.420	0.087	-	0.095
A1	0.890	-	1.140	0.035	-	0.045
b	0.550	-	0.670	0.022	-	0.026
b1	0.550	-	0.650	0.022	-	0.026
b2	0.760	-	0.960	0.030	-	0.038
b4	5.200	-	5.400	0.205	-	0.213
c	0.460	-	0.570	0.018	-	0.022
c1	0.450	-	0.550	0.018	-	0.022
c2	0.450	-	0.550	0.018	-	0.022
D	5.950	-	6.250	0.234	-	0.246
D1	4.200	-	4.500	0.165	-	0.177
E	6.400	-	6.700	0.252	-	0.264
E1	4.900	-	5.000	0.193	-	0.197
e	2.28BSC			0.090BSC		
L	8.900	-	9.650	0.350	-	0.380
L1	1.900	-	2.290	0.075	-	0.090
L2	0.500	-	0.800	0.020	-	0.031

Ordering and Marking Information

Device Marking: SSF6N70G

Package (Available)

TO-251（IPAK）

Operating Temperature Range

C : -55 to 150 ºC

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	75	40	3000	5	15000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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