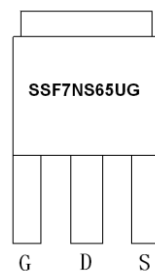
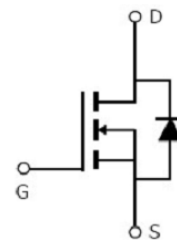


**Main Product Characteristics:**

$V_{DSS}$	650V
$R_{DS(on)}$	0.65Ω (typ.)
$I_D$	7A ①


**TO-251 (IPAK)**

**Marking and pin Assignment**

**Schematic diagram**
**Features and Benefits:**

- High dv/dt and avalanche capabilities
- 100% avalanche tested
- Low input capacitance and gate charge
- Low gate input resistance


**Description:**

The SSF7NS65UG series MOSFETs is a new technology, which combines an innovative super junction technology and advance process. This new technology achieves low Rdson, energy saving, high reliability and uniformity, superior power density and space saving.

**Absolute max Rating:**

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7 ①	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	5①	
$I_{DM}$	Pulsed Drain Current ②	28	
$P_D @ TC = 25^\circ C$	Power Dissipation ③	42	W
	Linear Derating Factor	0.33	W/°C
$V_{DS}$	Drain-Source Voltage	650	V
$V_{GS}$	Gate-to-Source Voltage	± 30	V
$E_{AS}$	Single Pulse Avalanche Energy @ L=100mH	480	mJ
$I_{AS}$	Avalanche Current @ L=100mH	3.1	A
$T_J T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +150	°C

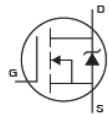
## Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	3.0	$^{\circ}C/W$
$R_{\theta JA}$	Junction-to-ambient ( $t \leq 10s$ ) ④	—	62	$^{\circ}C/W$

## Electrical Characterizes @ $T_A=25^{\circ}C$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	650	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.65	0.75	$\Omega$	$V_{GS}=10V, I_D = 1A$ $T_J = 125^{\circ}C$
		—	1.38	—		
		—	0.77	0.85	$\Omega$	$V_{GS}=10V, I_D = 4.8A$ $T_J = 125^{\circ}C$
		—	2.0	—		
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	$V_{DS} = V_{GS}, I_D = 250\mu A$ $T_J = 125^{\circ}C$
		—	2.2	—		
$I_{DSS}$	Drain-to-Source leakage current	—	—	1	$\mu A$	$V_{DS} = 650V, V_{GS} = 0V$ $T_J = 125^{\circ}C$
		—	—	50		
$I_{GSS}$	Gate-to-Source forward leakage	—	—	100	nA	$V_{GS} = 30V$ $V_{GS} = -30V$
		—	—	-100		
$Q_g$	Total gate charge	—	13	—	nC	$I_D = 5A,$ $V_{DS}=200V,$ $V_{GS} = 10V$
$Q_{gs}$	Gate-to-Source charge	—	2.6	—		
$Q_{gd}$	Gate-to-Drain("Miller") charge	—	3.1	—		
$t_{d(on)}$	Turn-on delay time	—	9.6	—	ns	$V_{GS}=10V, V_{DS} = 400V,$ $R_{GEN}=10.2\Omega, I_D = 2.2A$
$t_r$	Rise time	—	6	—		
$t_{d(off)}$	Turn-Off delay time	—	26	—		
$t_f$	Fall time	—	10	—		
$C_{iss}$	Input capacitance	—	500	—	pF	$V_{GS} = 0V$ $V_{DS} = 100V$ $f = 1MHz$
$C_{oss}$	Output capacitance	—	24	—		
$C_{rss}$	Reverse transfer capacitance	—	3	—		

## Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	7 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode)	—	—	28	A	
$V_{SD}$	Diode Forward Voltage	—	0.85	1.2	V	$I_S=4.8A, V_{GS}=0V$
$t_{rr}$	Reverse Recovery Time	—	111	—	nS	$T_J = 25^{\circ}C, I_F = 2.2A,$
$Q_{rr}$	Reverse Recovery Charge	—	639	—	nC	$di/dt = 100A/\mu s$

## Test circuits and Waveforms

**EAS Test Circuit:**

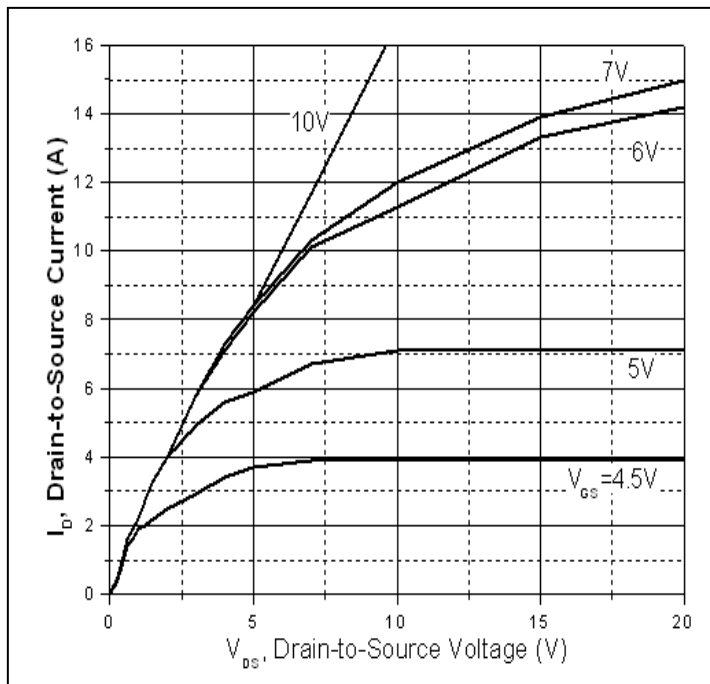
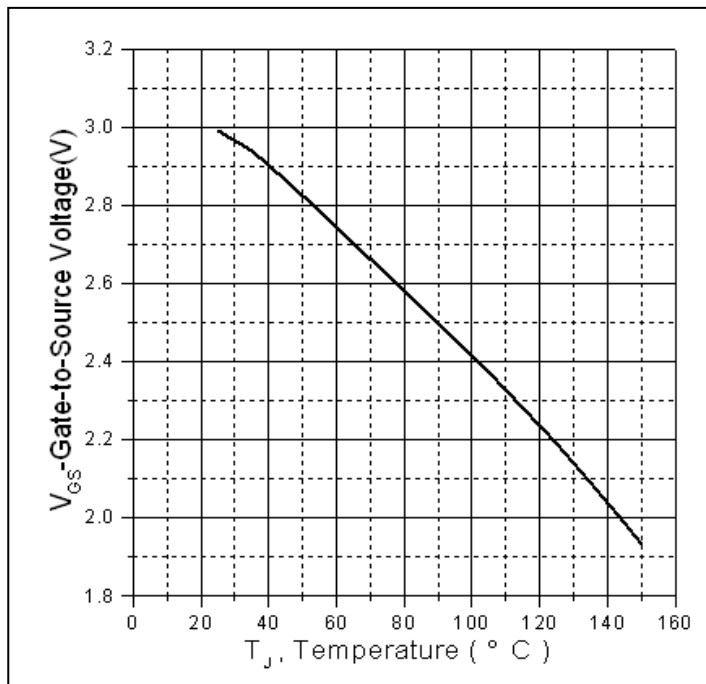
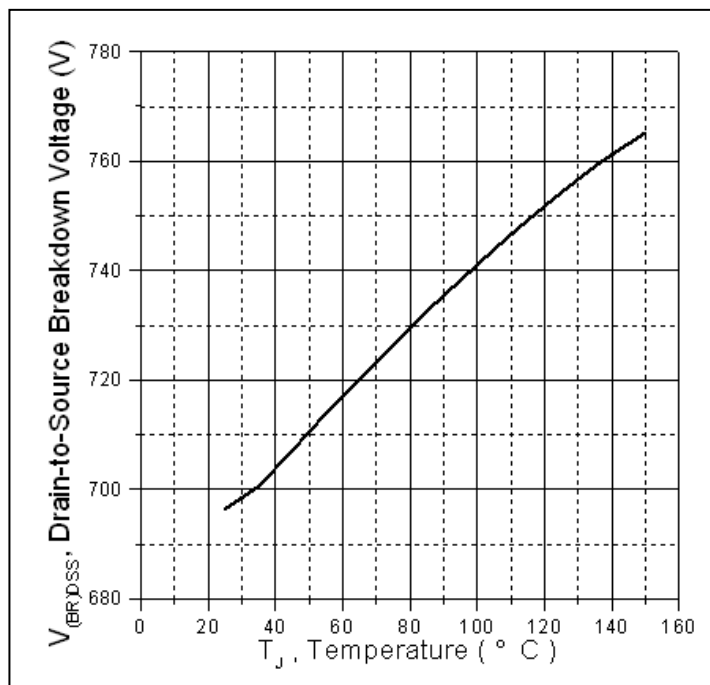
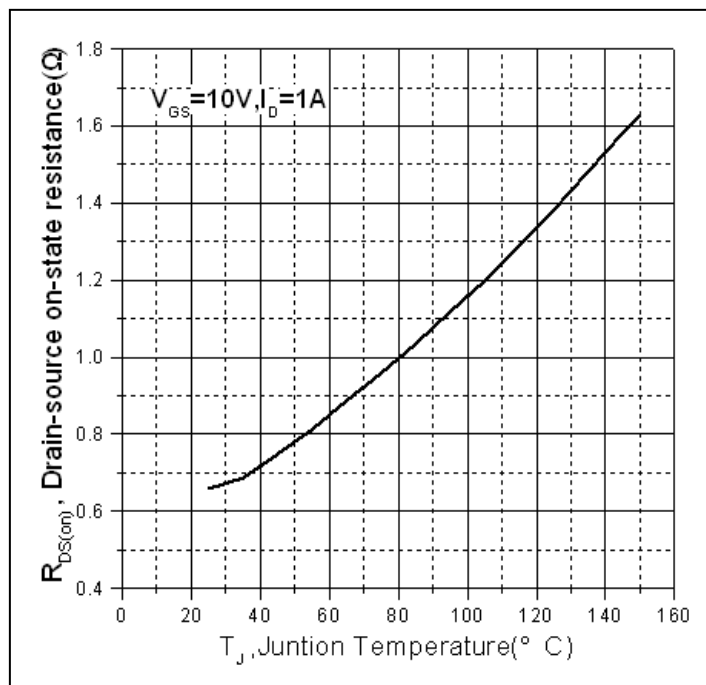
**Gate charge test circuit:**

**Switching Time Test Circuit:**

**Switching Waveforms:**


### Notes:

- ① Calculated continuous current based on maximum allowable junction temperature.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of  $R_{\theta JA}$  is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with  $T_A = 25^\circ\text{C}$

**Typical electrical and thermal characteristics**

**Figure 1: Typical Output Characteristics**

**Figure 2. Gate to source cut-off voltage**

**Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature**

**Figure 4: Normalized On-Resistance Vs. Case Temperature**

Typical electrical and thermal characteristics

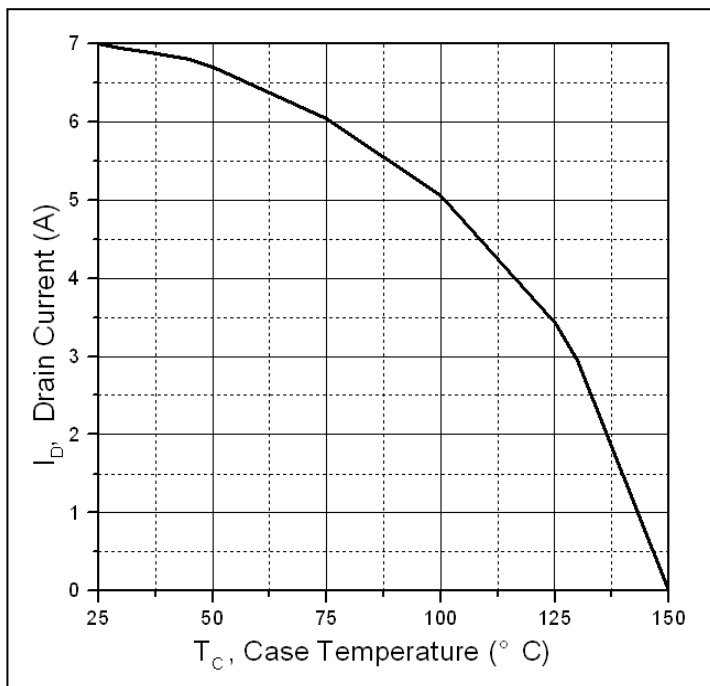


Figure 5. Maximum Drain Current Vs. Case Temperature

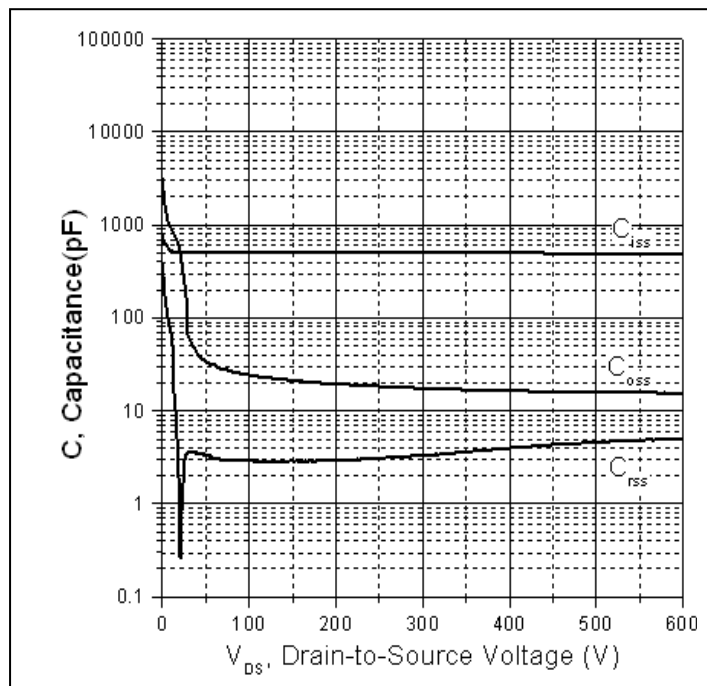


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

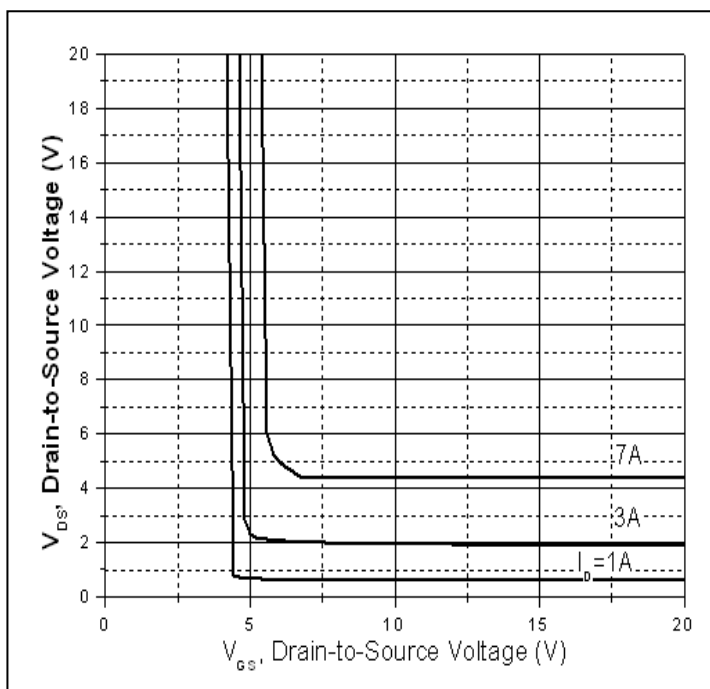


Figure 7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

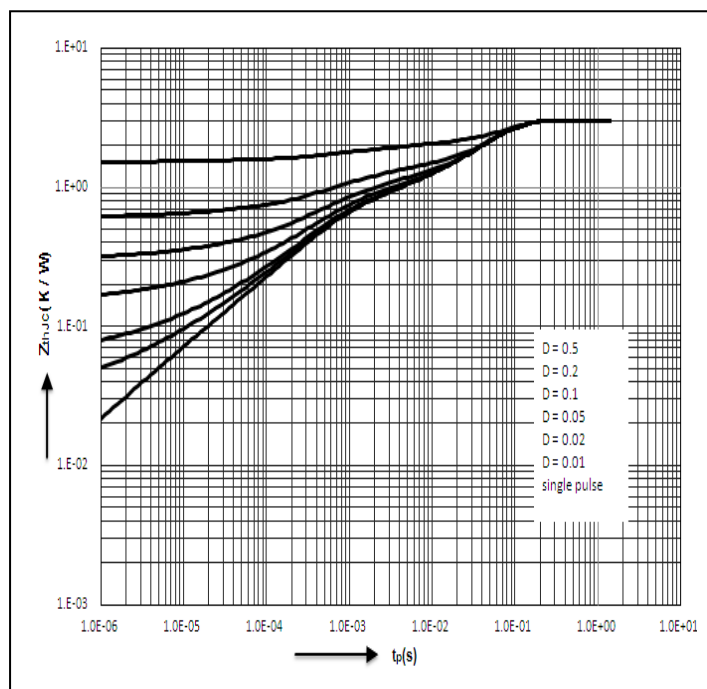


Figure 8. Maximum Effective Transient Thermal Impedance, Junction-to-Case



**Ordering and Marking Information**
**Device Marking: SSF7NS65UG**

**Package (Available)**  
**TO-251(IPAK)**  
**Operating Temperature Range**  
**C : -55 to 150 °C**

**Devices per Unit**

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-251	75	48	3600	5	18000

**Reliability Test Program**

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to $150^{\circ}\text{C}$ @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ @ 100% of Max $V_{GSS}$	168 hours 500 hours 1000 hours	3 lots x 77 devices

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**Technical Support:**

Technical@silikron.com

**Suzhou Silikron Semiconductor Corp.**

11A, 428 Xinglong Street, Suzhou Industrial Park, P.R.China

**TEL:** (86-512) 62560688

**FAX:** (86-512) 65160705

**E-mail:** Sales@silikron.com