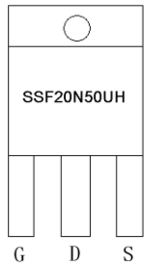
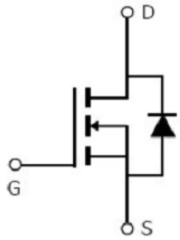
Main Product Characteristics

V_{DSS}	500V
$R_{DS}(on)$	0.2Ω (typ.)
I_D	20A ①

TO-247



Marking and Pin Assignment



Schematic Diagram

Features and Benefits

- Advanced Process Technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery

Description

These N-Channel enhancement mode power field effect transistors are produced using silikron proprietary MOSFET technology. This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switch mode power supplies.

Absolute Max Rating

Symbol	Parameter	Max.	Units
I_D @ TC = 25°C	Continuous Drain Current, V_{GS} @ 10V	20 ①	A
I_D @ TC = 100°C	Continuous Drain Current, V_{GS} @ 10V	12.6 ①	
I_{DM}	Pulsed Drain Current ②	80	
P_D @TC = 25°C	Power Dissipation ③	250	W
	Linear Derating Factor	2.0	W/°C
V_{DS}	Drain-Source Voltage	500	V
V_{GS}	Gate-to-Source Voltage	± 30	V
E_{AS}	Single Pulse Avalanche Energy @ L=6.5mH	1433	mJ
I_{AS}	Avalanche Current @ L=6.5mH	21	A
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to +150	°C

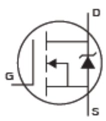
Thermal Resistance

Symbol	Characteristics	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case ③	—	0.5	℃/W
$R_{\theta JA}$	Junction-to-ambient (t ≤ 10s) ④	—	50	℃/W

Electrical Characteristics @T_A=25℃ unless otherwise specified

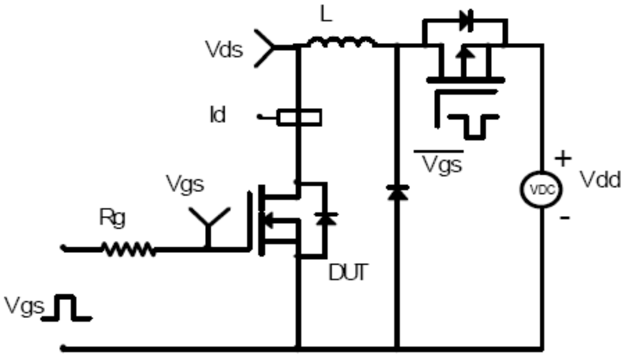
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source breakdown voltage	500	—	—	V	V_{GS} = 0V, I_D = 250μA
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	0.2	0.27	Ω	V_{GS}=10V,I_D = 10A
		—	0.47	—		T_J = 125°C
$V_{GS(th)}$	Gate threshold voltage	2	—	4	V	V_{DS} = V_{GS}, I_D = 250μA
		—	1.4	—		T_J = 125°C
I_{DSS}	Drain-to-Source leakage current	—	—	1	μA	V_{DS} = 500V,V_{GS} = 0V
		—	—	50		T_J = 125°C
I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS} = 30V
		—	—	-100		V_{GS} = -30V
Q_g	Total gate charge	—	48	—	nC	I_D = 20A,
Q_{gs}	Gate-to-Source charge	—	16	—		V_{DS}=400V,
Q_{gd}	Gate-to-Drain("Miller") charge	—	13	—		V_{GS} = 10V
$t_{d(on)}$	Turn-on delay time	—	18	—	ns	V_{GS}=10V, V_{DS} =250V, R_{GEN}=3.9Ω, R_L=12Ω
t_r	Rise time	—	64	—		
$t_{d(off)}$	Turn-Off delay time	—	51	—		
t_f	Fall time	—	49	—		
C_{iss}	Input capacitance	—	2778	—	pF	V_{GS} = 0V
C_{oss}	Output capacitance	—	350	—		V_{DS} = 25V
C_{rss}	Reverse transfer capacitance	—	3.1	—		f = 1MHz

Source-Drain Ratings and Characteristics

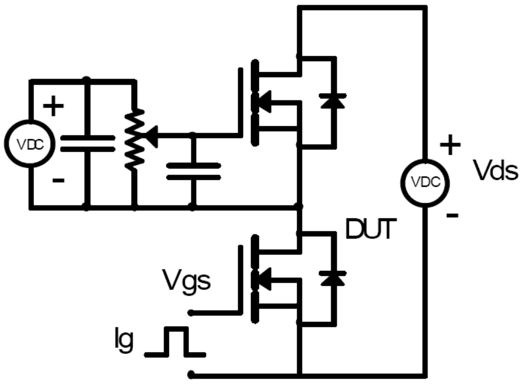
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	20 ①	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode)	—	—	80	A	
V_{SD}	Diode Forward Voltage	—	1.0	1.4	V	I_S=20A, V_{GS}=0V
t_{rr}	Reverse Recovery Time	—	570	—	nS	T_J = 25°C, I_F =20A, di/dt = 100A/μs
Q_{rr}	Reverse Recovery Charge	—	7.35	—	μC	

Test circuits and Waveforms

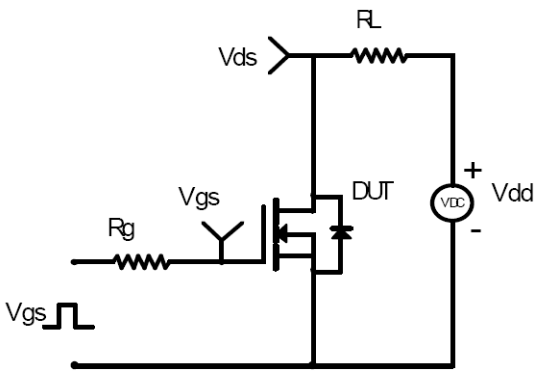
EAS Test Circuit



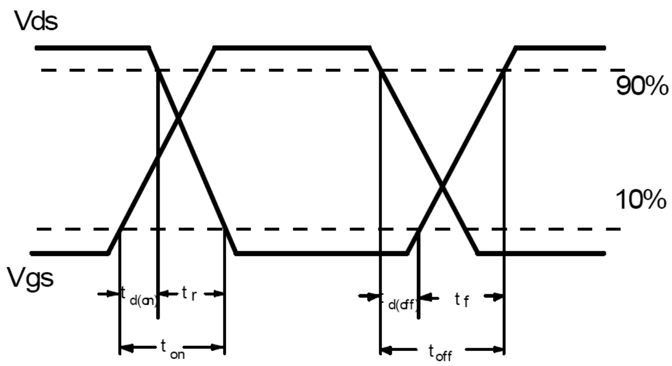
Gate charge test circuit



Switching Time Test Circuit



Switching Waveforms



Notes:

①Calculated continuous current based on maximum allowable junction temperature.

②Repetitive rating; pulse width limited by max. junction temperature.

③The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.

④The value of $R_{\theta JA}$ is measured with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with TA =25°C

Typical electrical and thermal characteristics

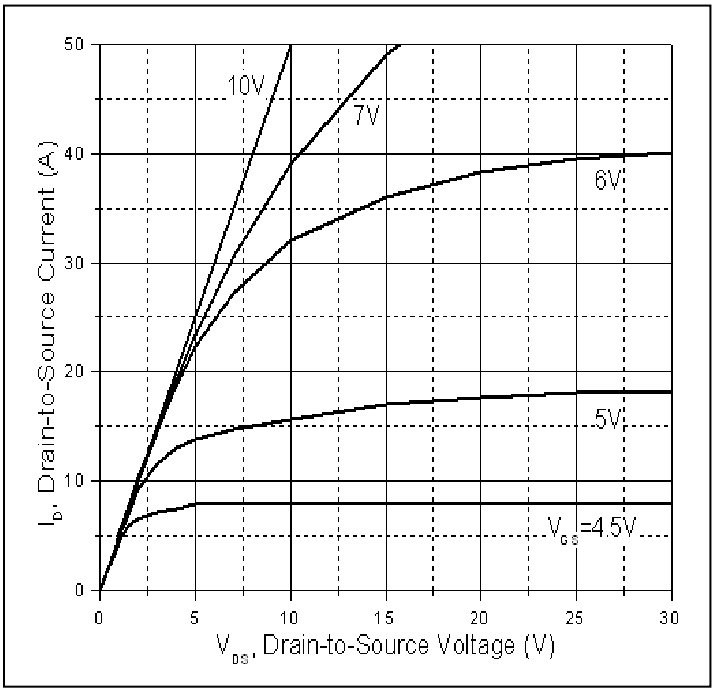


Figure 1.Typical Output Characteristics

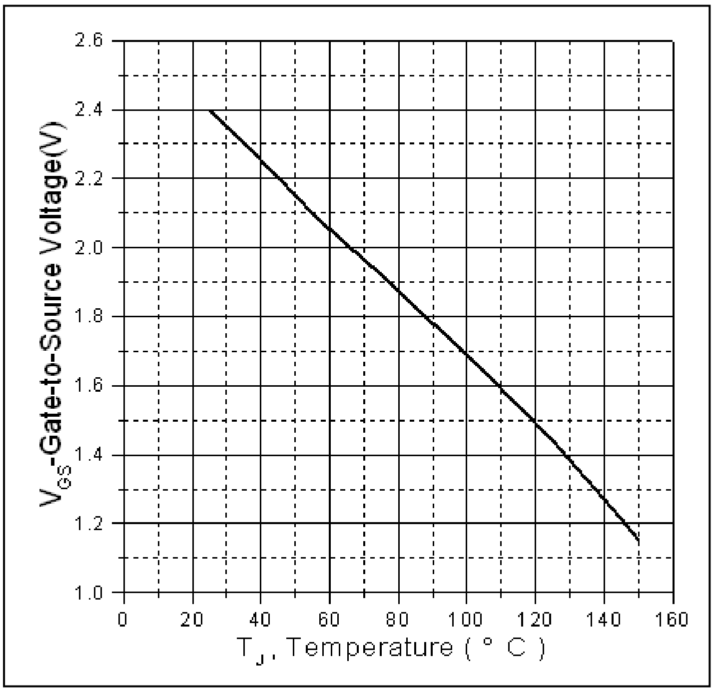


Figure 2. Gate to source cut-off voltage

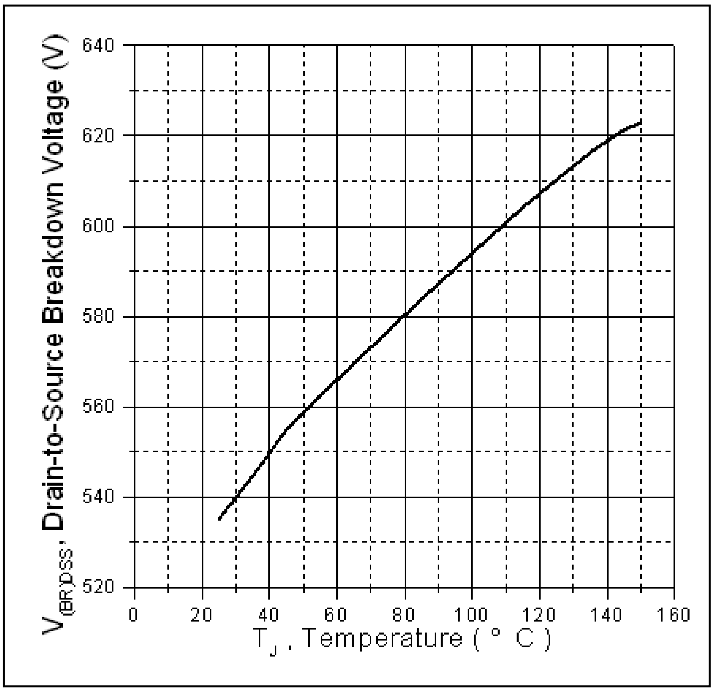


Figure 3. Drain-to-Source Breakdown Voltage Vs. Case Temperature

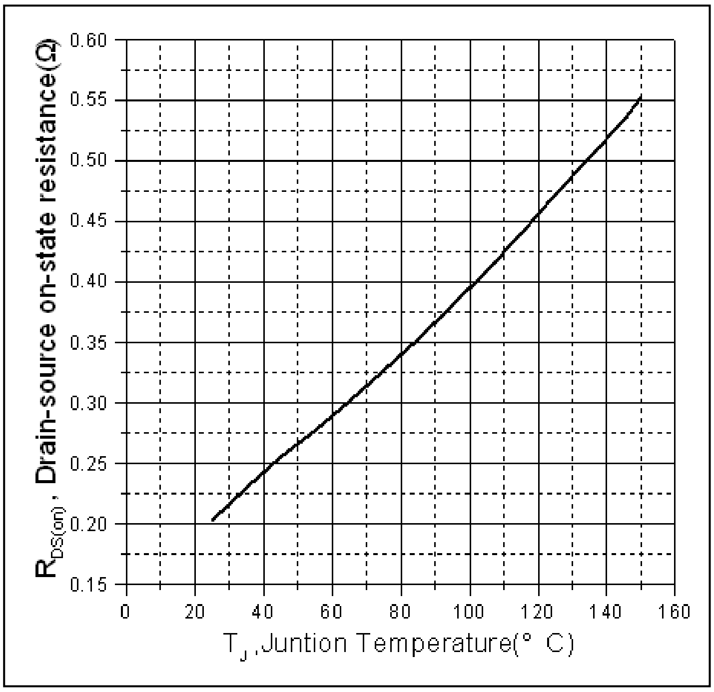


Figure 4.Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

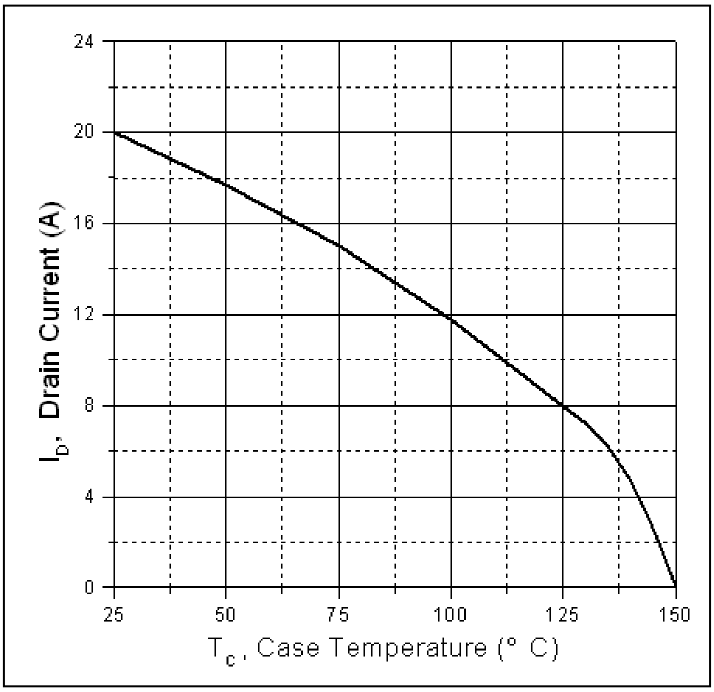


Figure 5. Maximum Drain Current Vs. Case Temperature

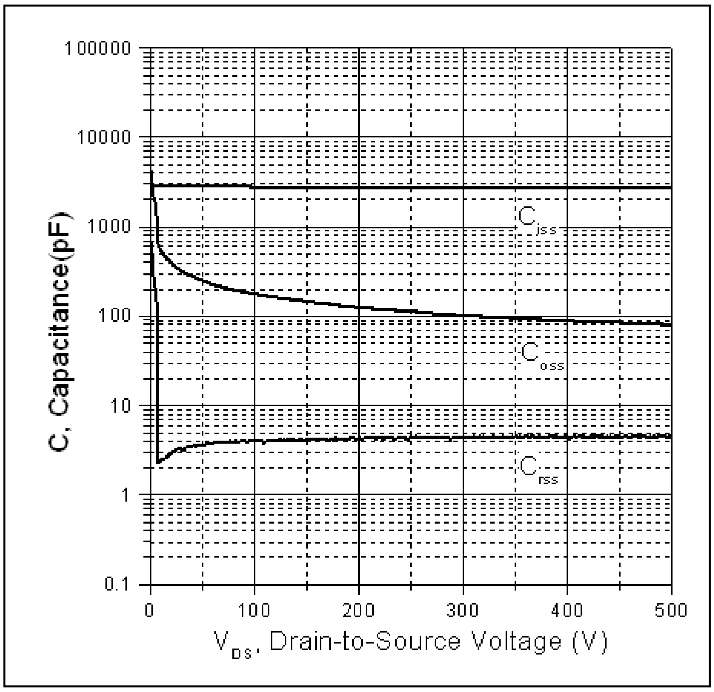


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

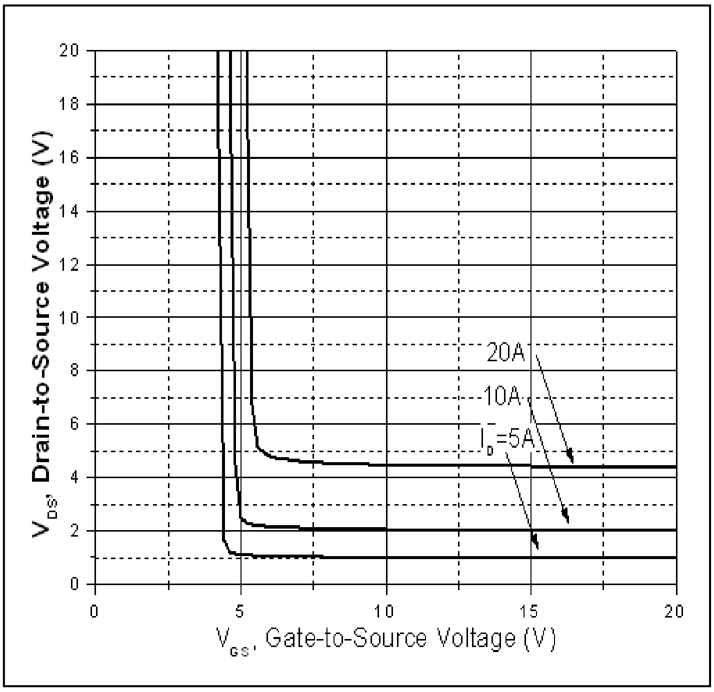


Figure7. Drain-to-Source Voltage Vs. Gate-to-Source Voltage

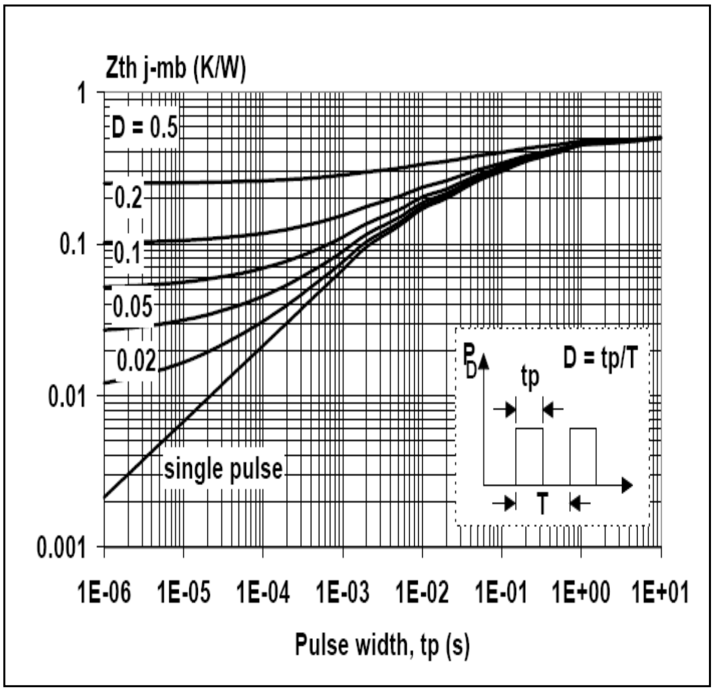
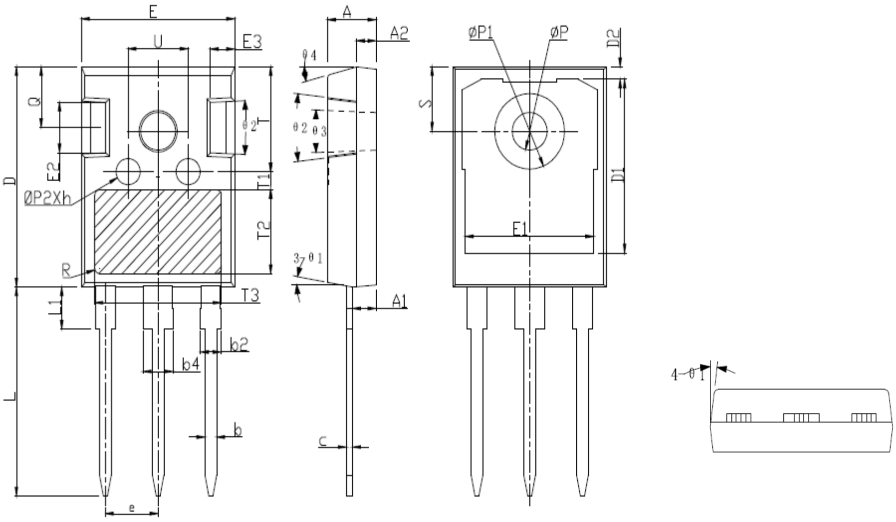


Figure8. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:

TO247 PACKAGE OUTLINE DIMENSION



Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.900	5.000	5.100	0.193	0.197	0.201
A1	2.310	2.410	2.510	0.091	0.095	0.099
A2	1.900	2.000	2.100	0.075	0.079	0.083
b	1.160	1.210	1.260	0.046	0.048	0.050
b2	1.960	2.010	2.060	0.077	0.079	0.081
b4	2.960	3.010	3.060	0.117	0.119	0.120
c	0.590	0.610	0.660	0.023	0.024	0.026
D	20.900	21.000	21.100	0.823	0.827	0.831
D1	16.250	16.550	16.850	0.640	0.652	0.663
D2	1.050	1.200	1.350	0.041	0.047	0.053
E	15.700	15.800	15.900	0.618	0.622	0.626
E1	13.100	13.300	13.500	0.516	0.524	0.531
E2	4.900	5.000	5.100	0.193	0.197	0.201
E3	2.400	2.500	2.600	0.094	0.098	0.102
e	5.44BSC			0.214BSC		
h	0.050	0.100	0.150	0.002	0.004	0.006
L	19.800	19.920	20.100	0.780	0.784	0.791
L1	-	-	4.300	-	-	0.169
ΦP	3.500	3.600	3.700	0.138	0.142	0.146
ΦP1	-	-	7.300	-	-	0.287
ΦP2	2.400	2.500	2.600	0.094	0.098	0.102
Q	5.600	5.800	6.000	0.220	0.228	0.236
S	6.15BSC			0.242BSC		
R	0.50BSC			0.020BSC		
T	9.800	-	10.200	0.386	-	0.402
T1	1.65REF			0.065REF		
T2	8.00REF			0.315REF		
T3	12.80REF			0.504REF		
U	6.000	-	6.400	0.236	-	0.252
θ1	6°	7°	8°	6°	7°	8°
θ2	4°	5°	6°	4°	5°	6°
θ3	1°	-	1.5°	1°	-	1.5°
θ4	14°	15°	16°	14°	15°	16°

Ordering and Marking Information

Device Marking: SSF20N50UH

Package (Available)

TO-247

Operating Temperature Range

C : -55 to 150 °C

Devices per Unit

Package Type	Units/ Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
TO-247	30	11	330	6	1980

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	T_j=125℃ to 150℃ @ 80% of Max V_{DSS}/V_{CES}/VR	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	T_j=150℃ @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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