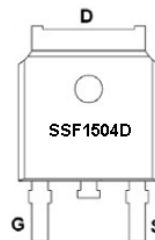
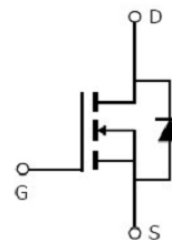


Main Product Characteristics:

V_{DSS}	170V(typ)
$R_{DS(on)}$	0.3Ω(typ)
I_D	6A


DPAK

Marking and pin Assignment

Schematic diagram
Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature


Description:

It utilizes the latest trench processing techniques to achieve the high cell density and reduces the on-resistance with high repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in power switching application and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	6	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	4	
I_{DM}	Pulsed Drain Current②	20	
$P_D @ TC = 25^\circ C$	Power Dissipation③	24	W
	Linear Derating Factor	0.16	W/°C
V_{DS}	Drain-Source Voltage	150	V
V_{GS}	Gate-to-Source Voltage	± 20	V
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C

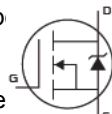
Thermal Resistance

Symbol	Characterizes	Typ.	Max.	Units
R _{θJC}	Junction-to-case ^③	—	6.25	°C/W
R _{θJA}	Junction-to-Ambient (t ≤ 10s) ^④	—	100	°C/W
	Junction-to-Ambient (PCB mounted, steady-state) ^④	—	71	°C/W

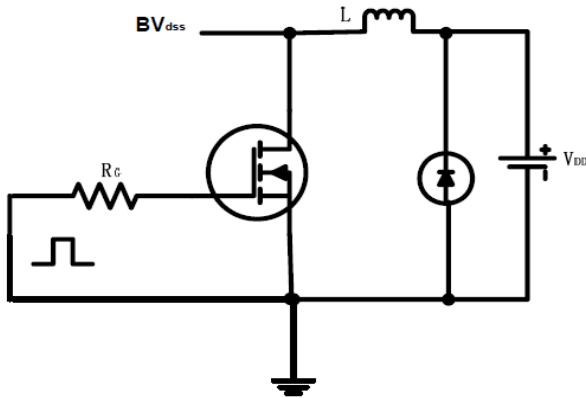
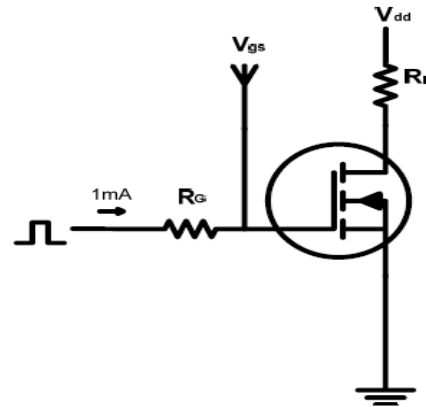
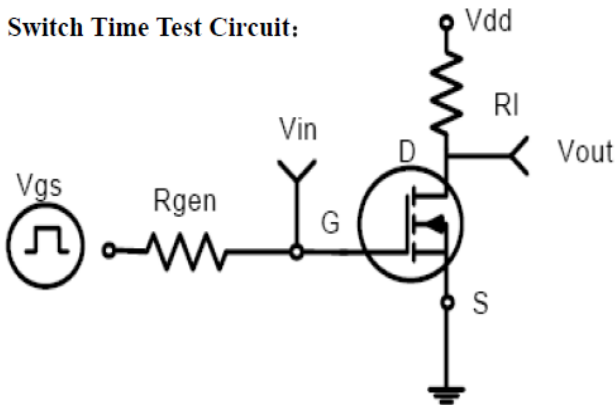
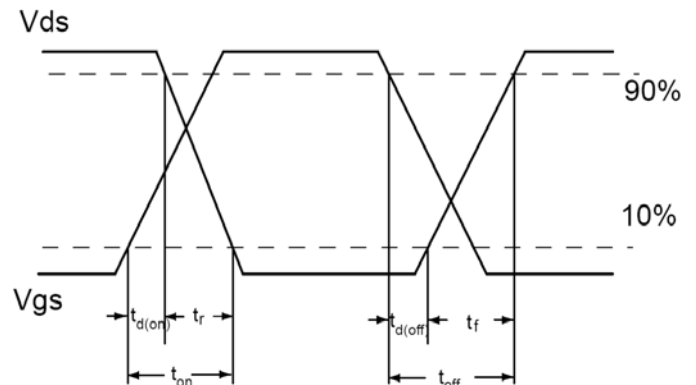
Electrical Characterizes @T_A=25°C unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source breakdown voltage	150	170		V	V _{GS} = 0V, I _D = 250μA
R _{DSS(on)}	Static Drain-to-Source on-resistance	—	0.3	0.35	Ω	V _{GS} =10V, I _D = 3A T _J = 125°C
		—	0.7	—		
V _{GS(th)}	Gate threshold voltage	2	—	4	V	V _{DS} = V _{GS} , I _D = 250μA T _J = 125°C
		—	2.8	—		
I _{DSS}	Drain-to-Source leakage current	—	—	1	μA	V _{DS} = 150, V _{GS} =10V T _J = 125°C
		—	—	50		
I _{GSS}	Gate-to-Source forward leakage			100	nA	V _{GS} = 20V
	Gate-to-Source reverse leakage	-100	-			V _{GS} = -20V
Q _g	Total gate charge		20		nC	I _D = 6A V _{DD} =120V V _{GS} = 10V
Q _{gs}	Gate-to-Source charge		4			
Q _{gd}	Gate-to-Drain("Miller") charge		7			
t _{d(on)}	Turn-on delay time		17		ns	V _{GS} =10V, V _{DD} =24.6V, R _L =8.2Ω, R _{GEN} =2.55Ω I _D =3.00A
t _r	Rise time		32			
t _{d(off)}	Turn-Off delay time		80			
t _f	Fall time		36			
C _{iss}	Input capacitance		759		pF	V _{GS} = 0V V _{DS} = 25V f = 800KHz
C _{oss}	Output capacitance		94			
C _{rss}	Reverse transfer capacitance		53			

Source-Drain Ratings and Characteristics

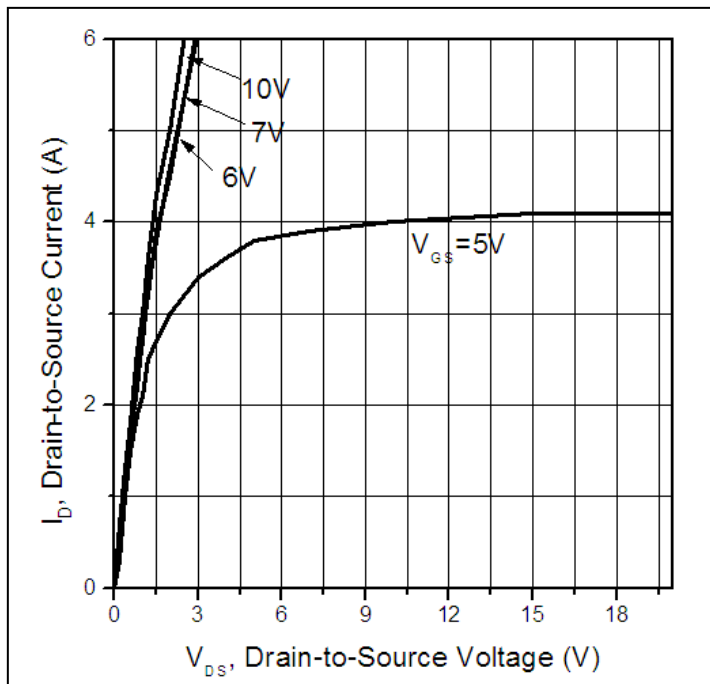
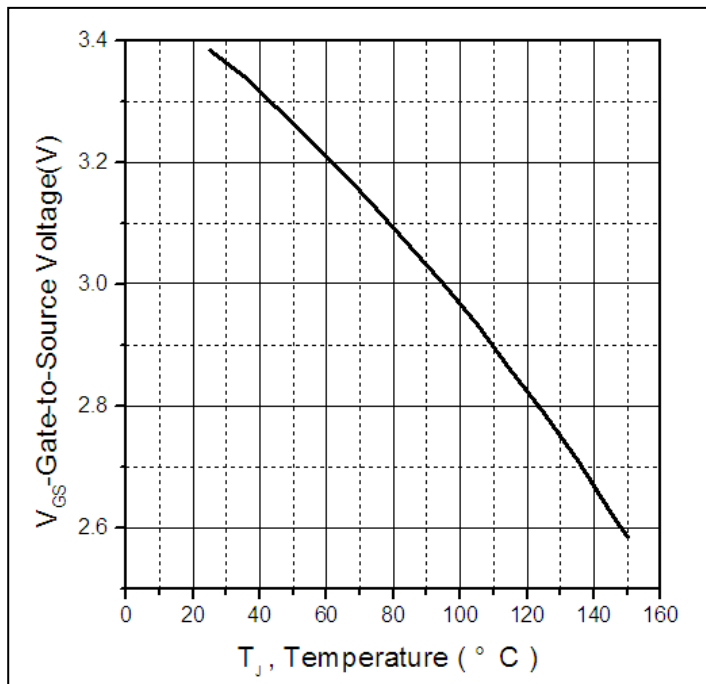
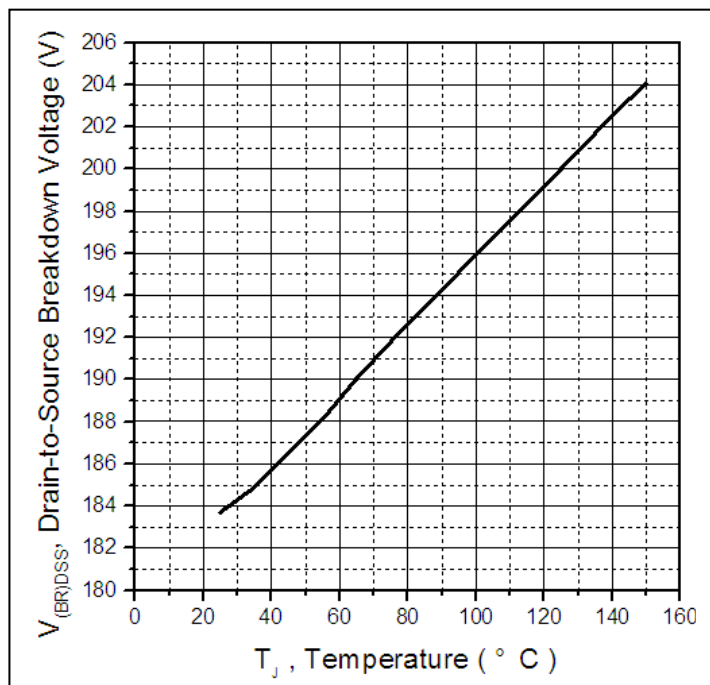
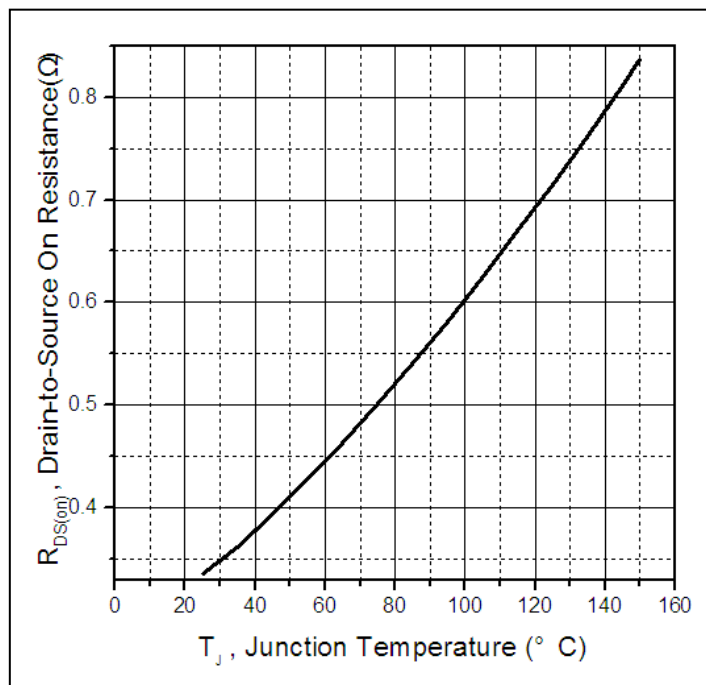
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	6	A	MOSFET symb showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode)	—	—	24	A	
V _{SD}	Diode Forward Voltage		0.82	1.5	V	I _S =6.00A, V _{GS} =0V, T _J = 25°C
t _{rr}	Reverse Recovery Time		90		ns	T _J = 25°C, I _F = 6.00A, di/dt =
Q _{rr}	Reverse Recovery Charge		105		nC	25.0A/μs

Test circuits and Waveforms

EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:


Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ C$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)} = 175^\circ C$.
- ⑥ The maximum current rating is limited by bond-wires.

Typical electrical and thermal characteristics

Figure 1: Typical Output Characteristics

Figure 2. Gate to source cut-off voltage

Figure 3. Drain-to-Source Breakdown Voltage vs. Temperature

Figure 4: Normalized On-Resistance Vs. Case Temperature

Typical electrical and thermal characteristics

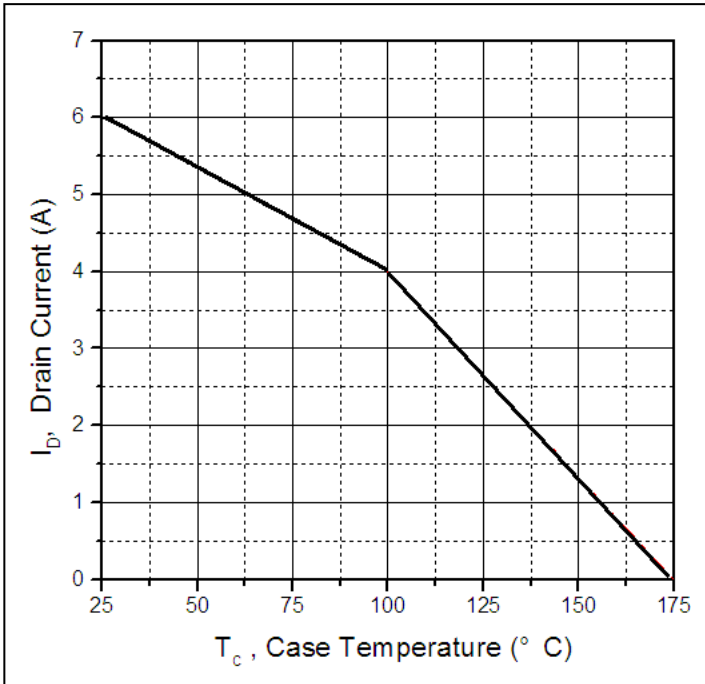


Figure 5. Maximum Drain Current Vs. Case Temperature

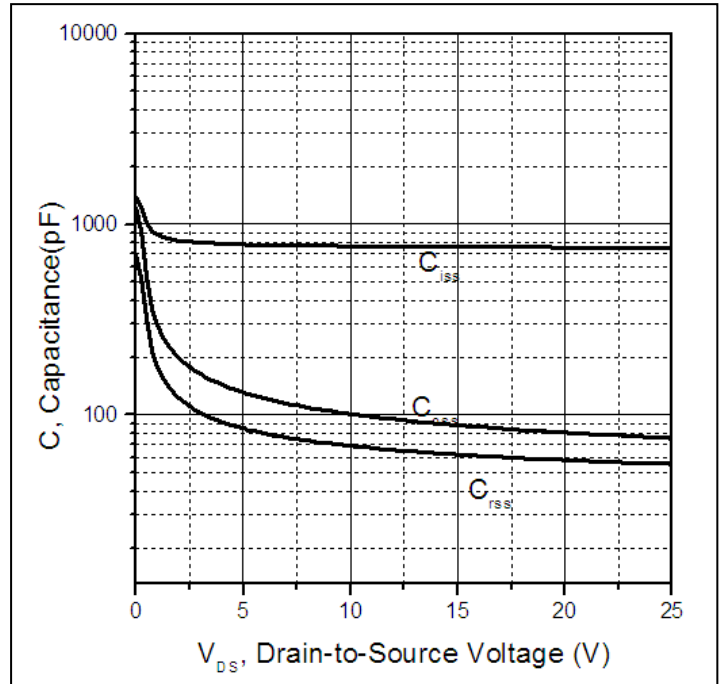


Figure 6. Typical Capacitance Vs. Drain-to-Source Voltage

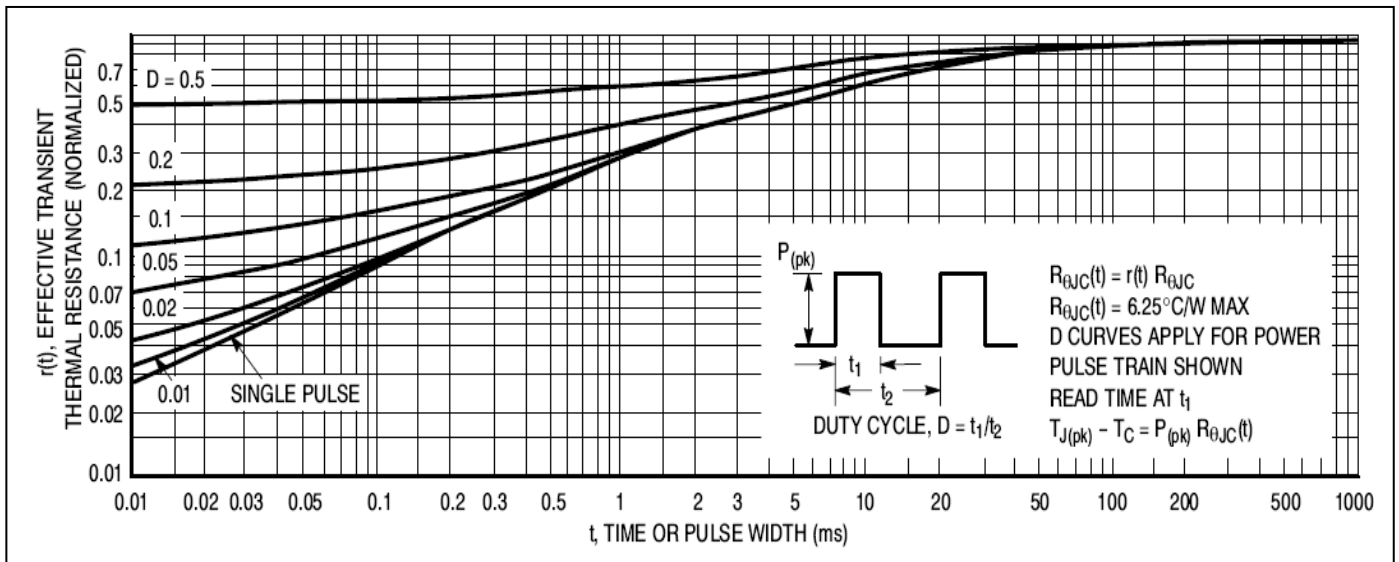
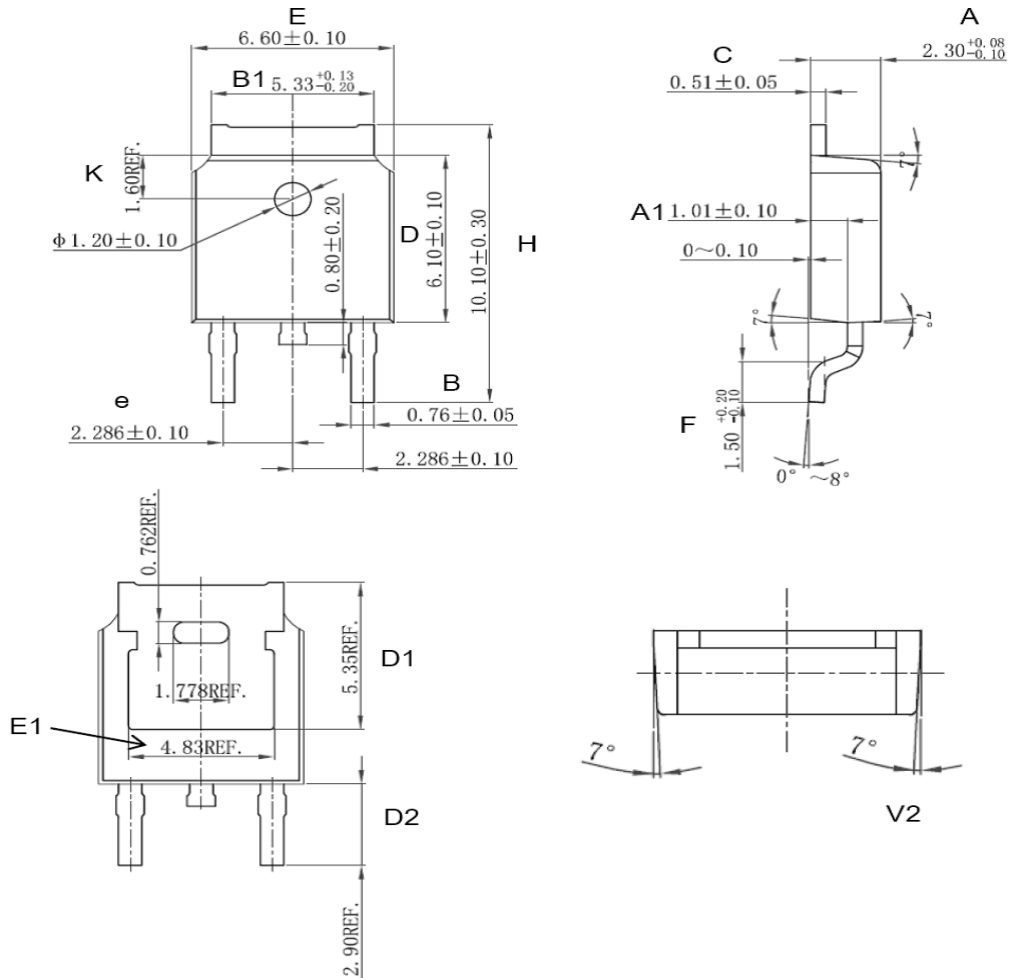


Figure 7. Maximum Effective Transient Thermal Impedance, Junction-to-Case

Mechanical Data:
DPAK PACKAGE OUTLINE DIMENSION_CD


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	2.200	2.300	2.380	0.087	0.091	0.094
A1	0.910	1.010	1.110	0.036	0.040	0.044
B	0.710	0.760	0.810	0.028	0.030	0.032
B1	5.130	5.330	5.460	0.202	0.210	0.215
C	0.460	0.510	0.560	0.018	0.020	0.022
D	6.000	6.100	6.200	0.236	0.240	0.244
D1	5.350 (REF)			0.211 (REF)		
D2	2.900 (REF)			0.114 (REF)		
E	6.500	6.600	6.700	0.256	0.260	0.264
E1	4.83 (REF)			0.190 (REF)		
e	2.186	2.286	2.386	0.086	0.090	0.094
H	9.800	10.100	10.400	0.386	0.398	0.409
F	1.400	1.500	1.700	0.055	0.059	0.067
K	1.600 (REF)			0.063 (REF)		
V2	8° (REF)			8° (REF)		

Ordering and Marking Information
Device Marking: SSF1504D

Package (Available)
DPAK
Operating Temperature Range
C : -55 to 175 °C

Devices per Unit

Package Type	Units/Tube	Tubes/Inner Box	Units/Inner Box	Inner Boxes/Carton Box	Units/Carton Box
DPAK	80	50	4000	10	40000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=125^{\circ}\text{C}$ to 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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