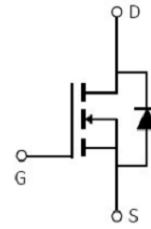
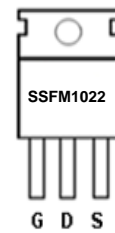


Main Product Characteristics:

V_{DSS}	100V
$R_{DS(on)}$	19mohm
I_D	40A


Features and Benefits:

- Advanced trench MOSFET process technology
- Special designed for PWM, load switching and general purpose applications
- Ultra low on-resistance with low gate charge
- Fast switching and reverse body recovery
- 175°C operating temperature

TO220

 Marking and pin
Assignment

Schematic diagram


Description:

It utilizes the latest FRRMOS (fast reverse recovery MOS) trench processing techniques to achieve extremely low on resistance, fast switching speed and short reverse recovery time. These features combine to make this design an extremely efficient and reliable device for use in PWM, load switching and a wide variety of other applications

Absolute max Rating:

Symbol	Parameter	Max.	Units
$I_D @ TC = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	40	A
$I_D @ TC = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ ①	36	
IDM	Pulsed Drain Current②	160	
ISM	Pulsed Source Current (Body Diode)②	160	
$PD @ TC = 25^\circ C$	Power Dissipation③	3.2	W
$PD @ TC = 100^\circ C$	Power Dissipation③	2	W
VDS	Drain-Source Voltage	100	V
VGS	Gate-to-Source Voltage	± 25	V
EAS	Single Pulse Avalanche Energy @ $L=0.1mH$ ②	42	mJ
IAR	Avalanche Current @ $L=0.1mH$ ②	29	A
$T_J \quad T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	$^\circ C$

Thermal Resistance

Symbol	Characterizes	Value	Unit
$R_{\theta JC}$	Junction-to-case③	16	$^\circ C/W$
$R_{\theta JA}$	Junction-to-ambient ($t \leq 10s$) ④	32	$^\circ C/W$
	Junction-to-Ambient (PCB mounted, steady-state) ④	60	$^\circ C/W$

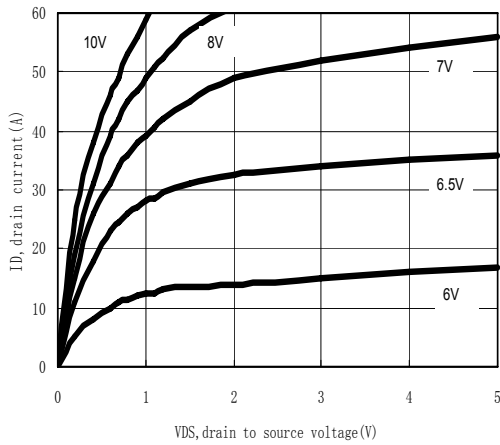
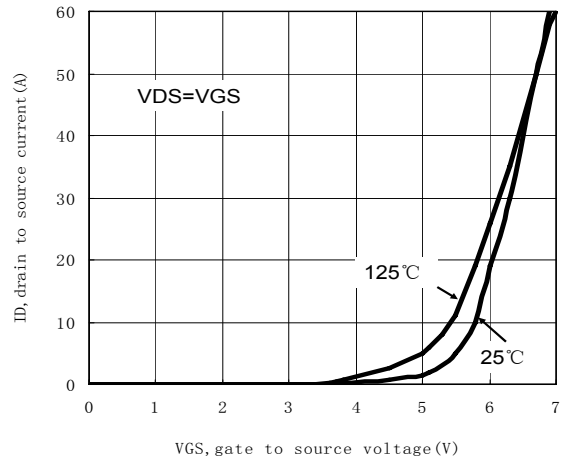
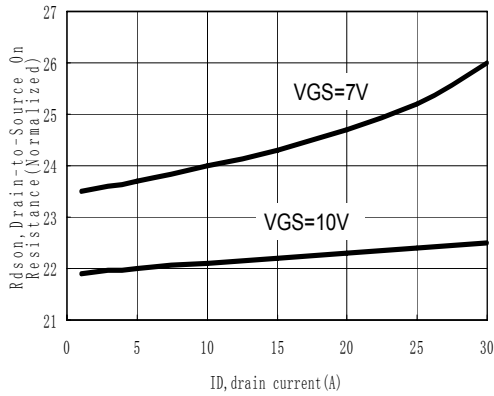
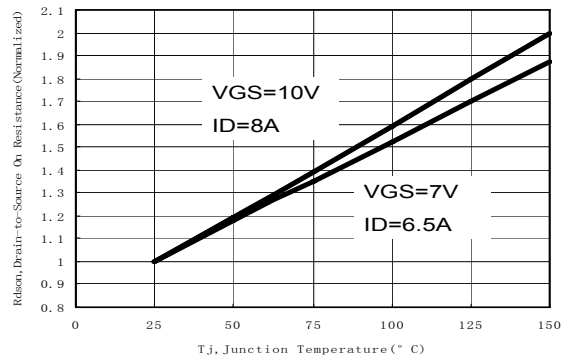
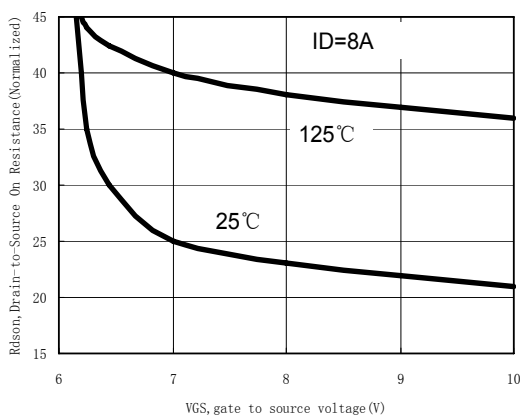
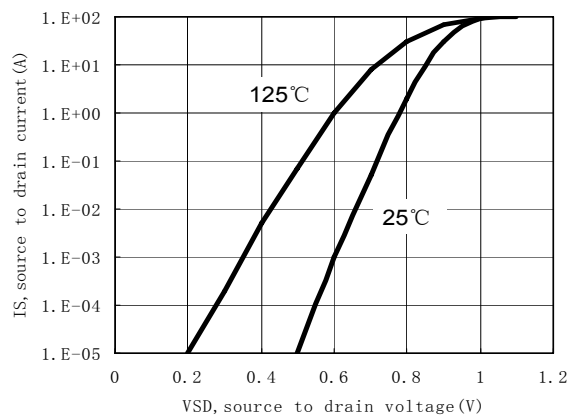
Electrical Characterizes @ $T_A=25^{\circ}\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max	Units	Conditions
BVDSS	Drain-to-Source breakdown voltage	100	—	—	V	VGS = 0V, ID = 250 μ A
RDS(on)	Static Drain-to-Source on-resistance	—	19	22	m Ω	VGS = 10V, ID = 8A
VGS(th)	Gate threshold voltage	2	—	4	V	VDS = VGS, ID = 250 μ A
IDSS	Drain-to-Source leakage current	—	—	10	μ A	VDS = 100V, VGS = 0V
		—	—	50		VDS = 100V, VGS = 0V, TJ = 55 $^{\circ}$ C
IGSS	Gate-to-Source forward leakage	—	—	100	nA	VGS = 25V
	Gate-to-Source reverse leakage	-100	—	—		VGS = -25V
Qg	Total gate charge	—	26.4	35	nC	VGS=10V, VDS=50V, ID=8A
Qgs	Gate-to-Source charge	—	9.18	15		
Qgd	Gate-to-Drain("Miller") charge	—	6.91	10		
Qg(th)	Gate charge at shreshold	—	5.78	8		
Vplateau	gate plateau voltage	—	5.48	8	V	
td(on)	Turn-on delay time	—	10.6	—	ns	VGS=10V, VDS=50V, RL=6 Ω , RGEN=3 Ω
tr	Rise time	—	3.8	—		
td(off)	Turn-Off delay time	—	16	—		
tf	Fall time	—	6	—		
Ciss	Input capacitance	—	1596	—	pF	VGS=0V, VDS=50V, f=1MHz
Coss	Output capacitance	—	249	—		
Crss	Reverse transfer capacitance	—	77	—		
Rg	Gate resistance	—	6	—	Ω	Vgs=0V, Vds=0V, f=1MHz

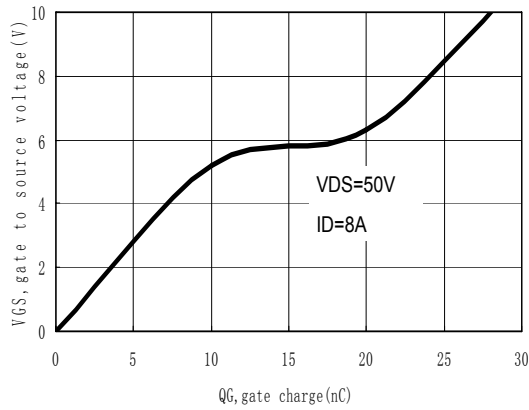
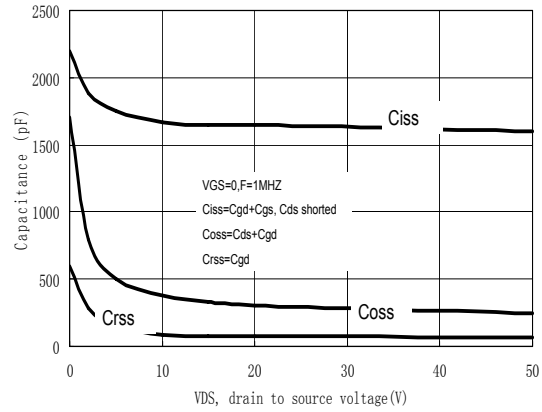
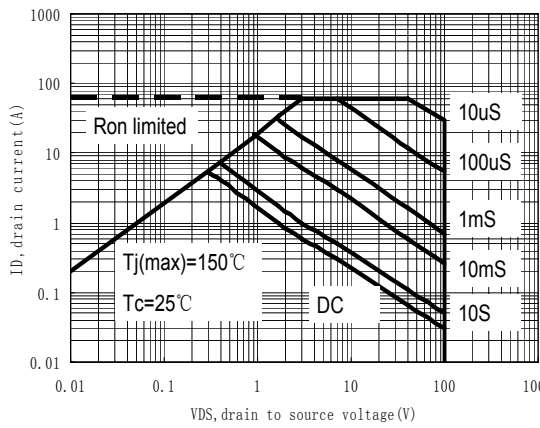
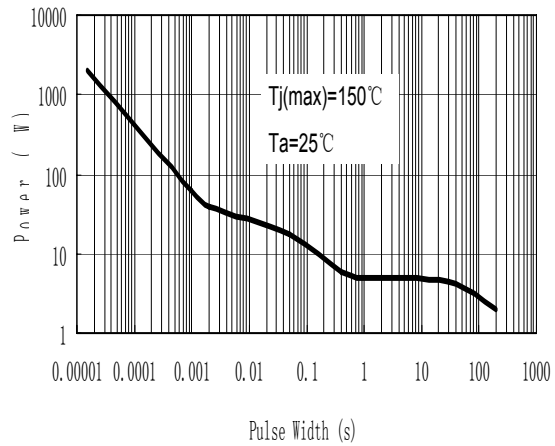
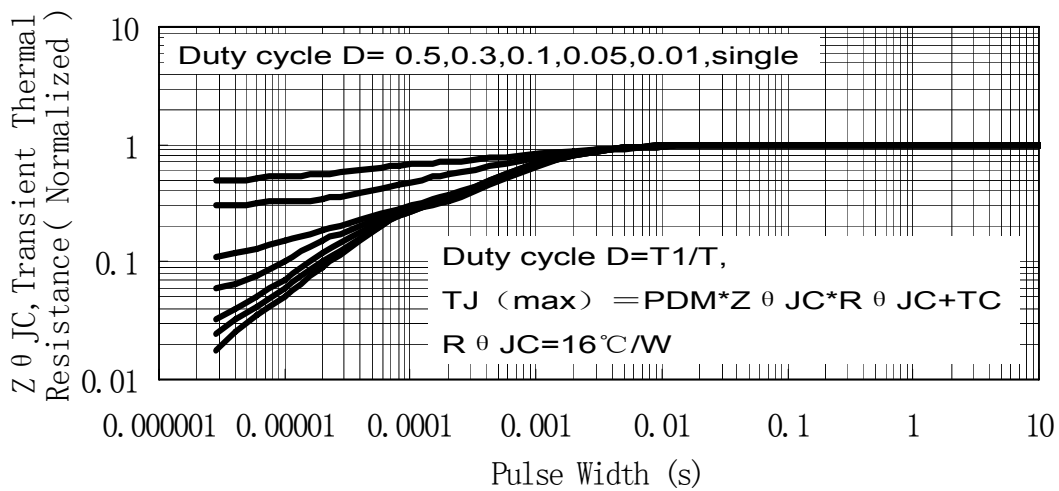
Source-Drain Ratings and Characteristics

Symbol	Parameter	Min.	Typ.	Max	Units	Conditions
IS	Maximum Body-Diode Continuous Current			40	A	
VSD	Diode Forward Voltage	—	0.65	1	V	IS=1A, VGS=0V
trr	Reverse Recovery Time	—	32	—	ns	IF=8A, dI/dt=100A/ μ s
Qrr	Reverse Recovery Charge	—	48	—	nC	
ton	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by LS+LD)				

Typical electrical and thermal characteristics


Figure 1: Typical Output Characteristics

Figure 2: Typical Transfer Characteristics

Figure 3: On-Resistance vs. Drain Current and Gate Voltage

Figure 4: On-Resistance vs. Junction Temperature

Figure 5: On-Resistance vs. Gate-Source Voltage

Figure 6: Body-Diode Characteristics

Typical electrical and thermal characteristics


Figure 7: Gate-Charge Characteristics Figure

8: Capacitance Characteristics

Figure 9: Maximum Forward Biased Safe Operating Area(Ⓢ)

Figure 10: Single Pulse Power Rating Junction-to-Ambient (Ⓢ)

Figure 11: Normalized Maximum Transient Thermal Impedance (Ⓢ)

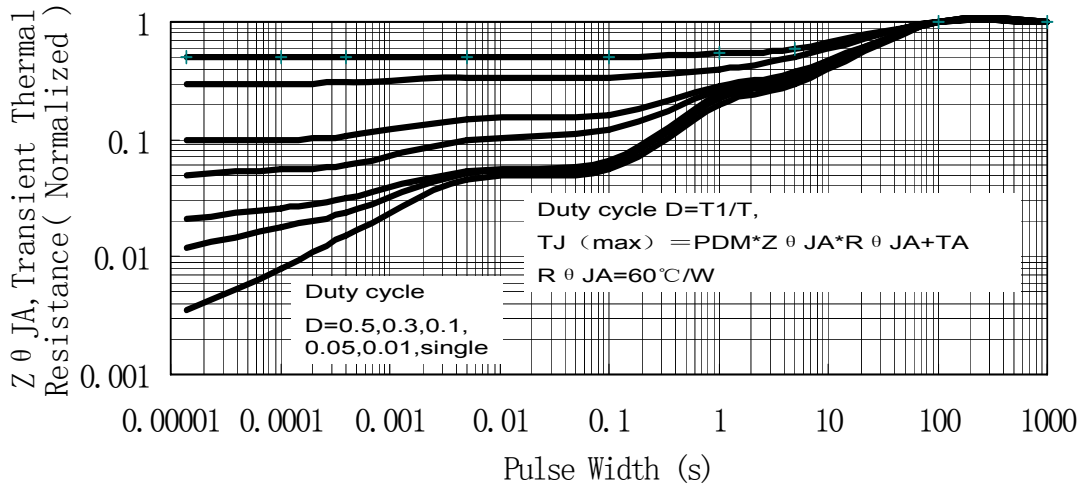
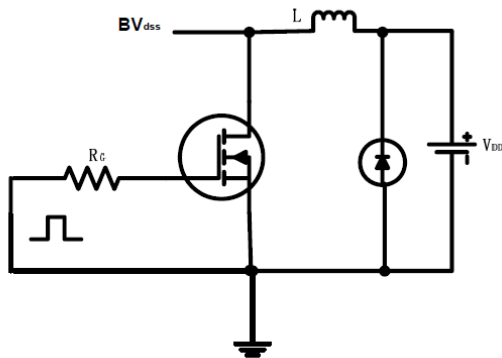
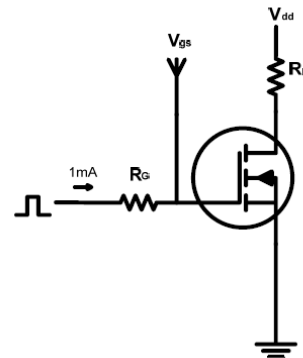
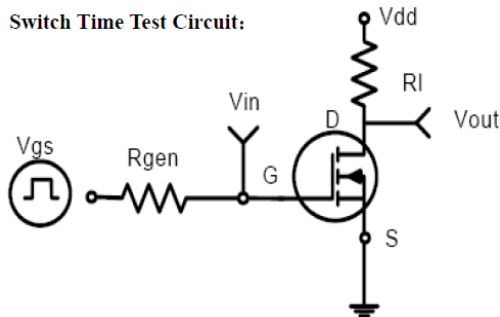
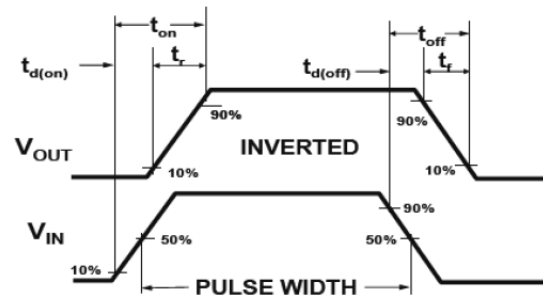
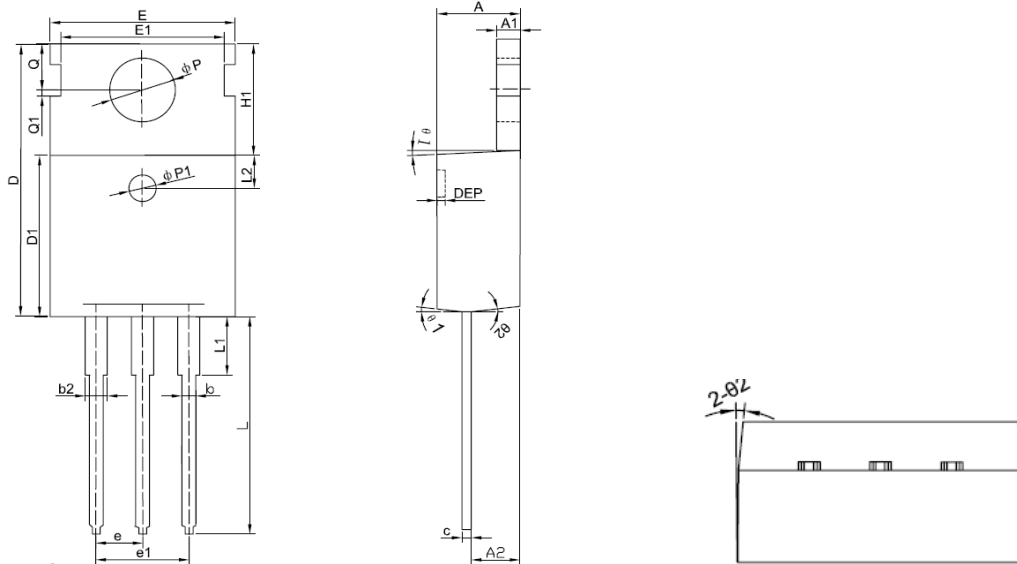


Figure 12: Normalized Maximum Transient Thermal Impedance (°C)

EAS test circuits:

Gate charge test circuit:

Switch Time Test Circuit:

Switch Waveforms:


Notes:

- ① The maximum current rating is limited by bond-wires.
- ② Repetitive rating; pulse width limited by max. junction temperature.
- ③ The power dissipation PD is based on max. junction temperature, using junction-to-case thermal resistance.
- ④ The value of $R_{\theta JA}$ is measured with the device mounted on 1in 2 FR-4 board with 2oz. Copper, in a still air environment with $T_A = 25^\circ\text{C}$
- ⑤ These curves are based on the junction-to-case thermal impedance which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_J(\text{MAX}) = 175^\circ\text{C}$.

Mechanical Data:
TO220 PACKAGE OUTLINE DIMENSION


Symbol	Dimension In Millimeters			Dimension In Inches		
	Min	Nom	Max	Min	Nom	Max
A	4.400	4.550	4.700	0.173	0.179	0.185
A1	1.270	1.300	1.330	0.050	0.051	0.052
A2	2.590	2.690	2.790	0.102	0.106	0.110
b	0.770	-	0.900	0.030	-	0.035
b2	1.230	-	1.360	0.048	-	0.054
c	0.480	0.500	0.520	0.019	0.020	0.020
D	15.100	15.400	15.700	-	0.606	-
D1	9.000	9.100	9.200	0.354	0.358	0.362
DEP	0.050	0.285	0.520	0.002	0.011	0.020
E	10.060	10.160	10.260	0.396	0.400	0.404
E1	-	8.700	-	-	0.343	-
$\Phi P1$	1.400	1.500	1.600	0.055	0.059	0.063
e	2.54BSC			0.1BSC		
e1	5.08BSC			0.2BSC		
H1	6.100	6.300	6.500	0.240	0.248	0.256
L	12.750	12.960	13.170	0.502	0.510	0.519
L1	-	-	3.950	-	-	0.156
L2	1.85REF			0.073REF		
ΦP	3.570	3.600	3.630	0.141	0.142	0.143
Q	2.730	2.800	2.870	0.107	0.110	0.113
Q1	-	0.200	-	-	0.008	-
$\square 1$	5°	7°	9°	5°	7°	9°
$\square 2$	1°	3°	5°	1°	3°	5°

Ordering and Marking Information
Device Marking: SSFM1022
Package (Available)
TO220
Operating Temperature Range
C : -55 to 175 °C
Devices per Unit

Package Type	Units/ Tube	Tubes/ Inner Box	Units/ Inner Box	Inner Boxes/ Carton Box	Units/ Carton Box
TO220	50	20	1000	6	6000

Reliability Test Program

Test Item	Conditions	Duration	Sample Size
High Temperature Reverse Bias(HTRB)	$T_j=150^{\circ}\text{C}$ or 175°C @ 80% of Max $V_{DSS}/V_{CES}/V_R$	168 hours 500 hours 1000 hours	3 lots x 77 devices
High Temperature Gate Bias(HTGB)	$T_j=150^{\circ}\text{C}$ or 175°C @ 100% of Max V_{GSS}	168 hours 500 hours 1000 hours	3 lots x 77 devices

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