

FML-G13S/FML-G14S

Super Fast Rectifiers

VOLTAGE RANGE: 300~400 V

CURRENT: 5.0 A



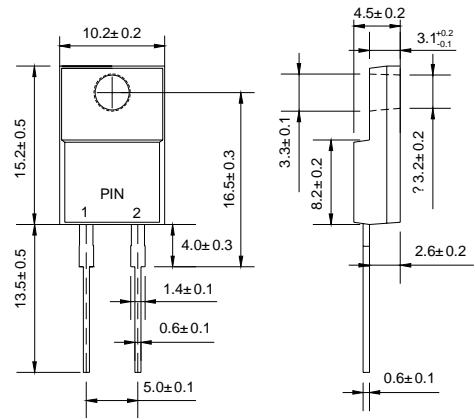
ITO-220AC

Features

- ◇ Metal-Semiconductor junction with guard ring
- ◇ Epitaxial construction
- ◇ Low forward voltage drop, low switching losses
- ◇ High surge capability
- ◇ For use in low voltage, high frequency inverters free wheeling, and polarity protection applications
- ◇ The plastic material carries U/L recognition 94V-0

Mechanical Data

- ◇ Case: JEDEC ITO-220AC
- ◇ Polarity: As marked
- ◇ Weight: 0.056 ounces, 1.587 gram
- ◇ Mounting position: Any



Dimensions in millimeters

MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

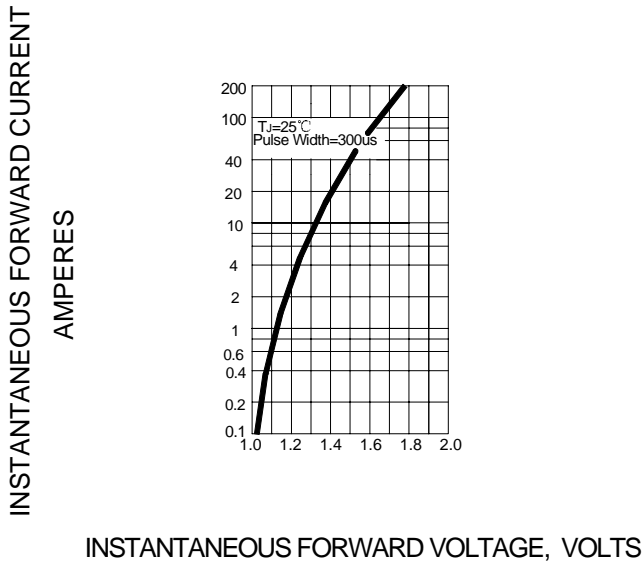
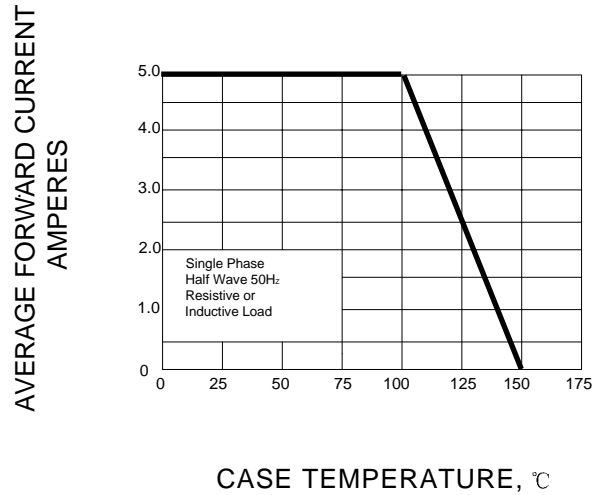
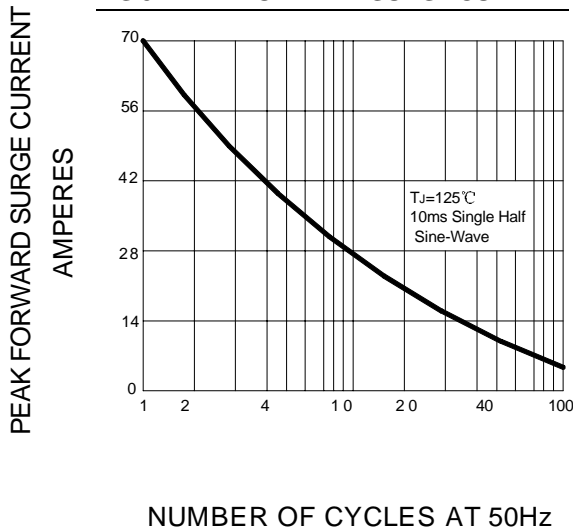
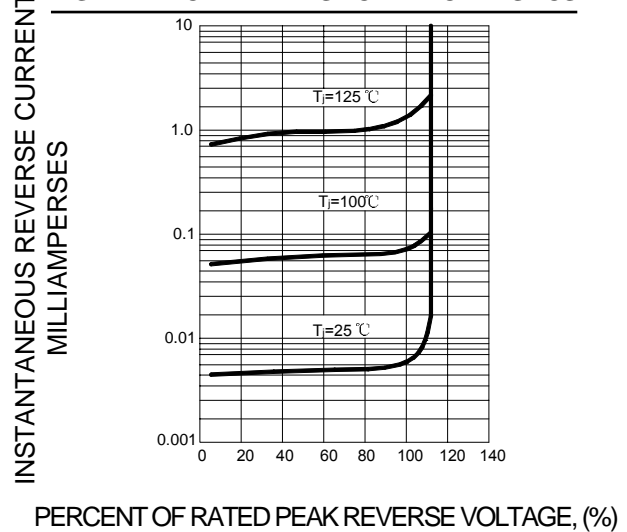
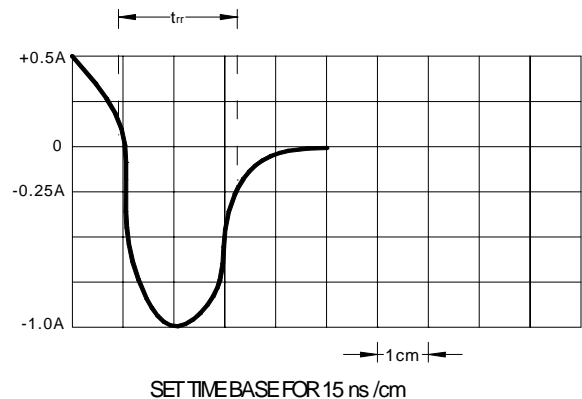
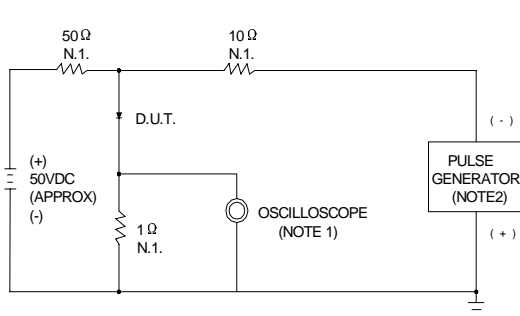
Ratings at 25°C ambient temperature unless otherwise specified.

Single phase, half wave, 50 Hz, resistive or inductive load. For capacitive load, derate by 20%.

		FML- G13S	FML- G14S	UNITS
Maximum recurrent peak reverse voltage	V_{RRM}	300	400	V
Maximum RMS voltage	V_{RMS}	210	280	V
Maximum DC blocking voltage	V_{DC}	300	400	V
Maximum average forward rectified current @ $T_C=100^\circ\text{C}$	$I_{F(AV)}$	5.0		A
Peak forward surge current 10ms single half-sine-wave superimposed on rated load	I_{FSM}	70		A
Maximum instantaneous forward voltage ($I_F=5.0A$)	V_F	1.3		V
Maximum reverse current @ $T_J=25^\circ\text{C}$ at rated DC blocking voltage @ $T_J=100^\circ\text{C}$	I_R	0.1 0.2		mA
Maximum reverse recovery time (Note1)	t_{rr}	35		ns
Typical thermal resistance (Note2)	$R_{\theta JC}$	4.0		$^\circ\text{C}/\text{W}$
Operating junction temperature range	T_J	- 55 ---- + 150		$^\circ\text{C}$
Storage temperature range	T_{STG}	- 55 ---- + 150		$^\circ\text{C}$

NOTE: 1. Measured with $I_F=0.5A$, $I_R=1A$, $I_{rr}=0.25A$.
2. Thermal resistance junction to case.

Ratings AND Characteristic Curves

FIG.1 – TYPICAL FORWARD CHARACTERISTIC

FIG.2– FORWARD DERATING CURVE

FIG.3– PEAK FORWARD SURGE CURRENT

FIG.4 – TYPICAL REVERSE CHARACTERISTICS

FIG.5 – REVERSE RECOVERY TIME CHARACTERISTIC AND TEST CIRCUIT DIAGRAM


NOTES:1.RISE TIME=7ns MAX. INPUT IMPEDANCE=1M Ω , 22pF
 2.RISE TIME=10ns MAX. SOURCE IMPEDANCE=50 Ω