Shenzhen Tuofeng Semiconductor Technology Co., Ltd

8810

Common-Drain Dual N-Channel Enhancement Mode Field Effect Transistor

General Description

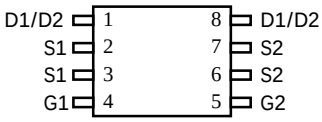
The 8810 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 1.8V. This device is suitable for use as a load switch or in PWM applications. It is ESD protected.

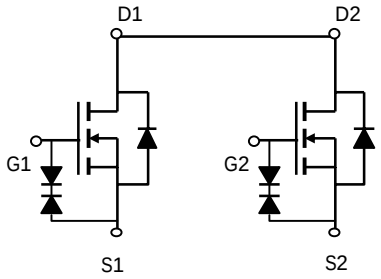
Standard Product 8810 is Pb-free (meets ROHS & Sony 259 specifications). 8810 is electrically identical.

Features

V_{DS} (V) = 20V
I_D = 6A (V_{GS} = 4.5V)
$R_{DS(ON)}$ < 22mΩ (V_{GS} = 4.5V)
$R_{DS(ON)}$ < 30mΩ (V_{GS} = 2.5V)
ESD Rating: 2000V HBM

TSSOP-8
Top View





Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	20	V
Gate-Source Voltage		V_{GS}	±8	V
Continuous Drain Current [A]	T_A=25°C	I_D	6	A
Pulsed Drain Current [B]		I_{DM}	30	
Power Dissipation [A]	T_A=25°C	P_D	1.5	W
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 150	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	64	83	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		89	120	°C/W
Maximum Junction-to-Lead [C]	Steady-State	$R_{\theta JL}$	53	70	°C/W

Electrical Characteristics (T =25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250μA, V_{GS}=0V	20			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=16V, V_{GS}=0V			1	μA
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}=±12V			±15	μA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250μA	0.5	0.6	1	V
$I_{D(ON)}$	On state drain current	V_{GS}=4.5V, V_{DS}=5V	30			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=4.5V, I_D=6A		20	22	mΩ
		V_{GS}=2.5V, I_D=5.5A		28	30	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=6A		29		S
V_{SD}	Diode Forward Voltage	I_S=1.5A,V_{GS} =0V			1.2	V
I_S	Maximum Body-Diode Continuous Current				2.5	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=10V, f=1MHz		1160		pF
C_{oss}	Output Capacitance			187		pF
C_{rss}	Reverse Transfer Capacitance			146		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.5		Ω
SWITCHING PARAMETERS						
Q_g	Total Gate Charge	V_{GS}=4.5V, V_{DS}=10V, I_D=7A		16		nC
Q_{gs}	Gate Source Charge			0.8		nC
Q_{gd}	Gate Drain Charge			3.8		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=5V, V_{DS}=10V, R_L=1.35Ω, R_{GEN}=3Ω		6.2		ns
t_r	Turn-On Rise Time			12.7		ns
$t_{D(off)}$	Turn-Off DelayTime			51.7		ns
t_f	Turn-Off Fall Time			16		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=7A, dI/dt=100A/μs		17.7		ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=7A, dI/dt=100A/μs		6.7		nC

A: The value of $R_{\theta JA}$ is measured with the device mounted on 1in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A =25°C. The value in any given application depends on the user's specific board design. The current rating is based on the t≤ 10s thermal resistance rating.

B: Repetitive rating, pulse width limited by junction temperature.

C. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to lead $R_{\theta JL}$ and lead to ambient.

D. The static characteristics in Figures 1 to 6,12,14 are obtained using 80μs pulses, duty cycle 0.5% max.

E. These tests are performed with the device mounted on 1 in^2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

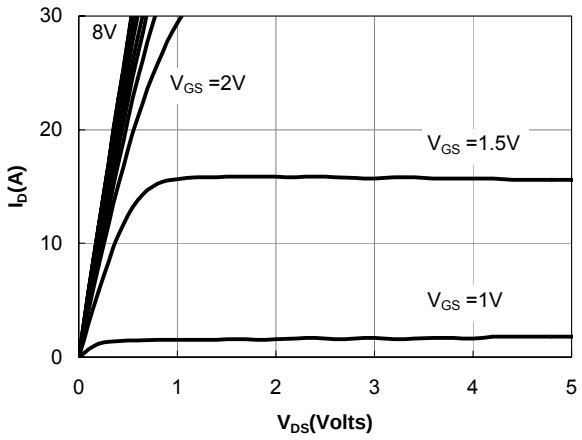


Figure 1: On-Regions Characteristics

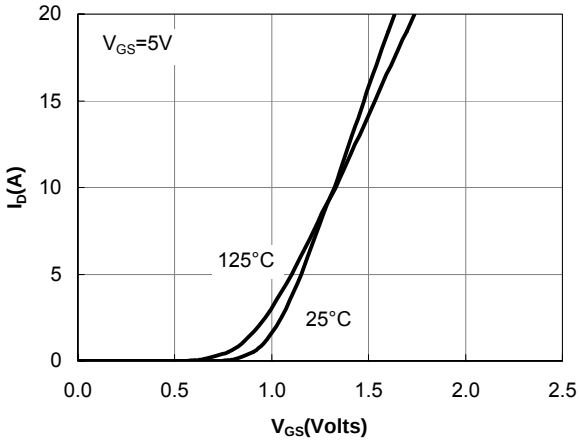


Figure 2: Transfer Characteristics

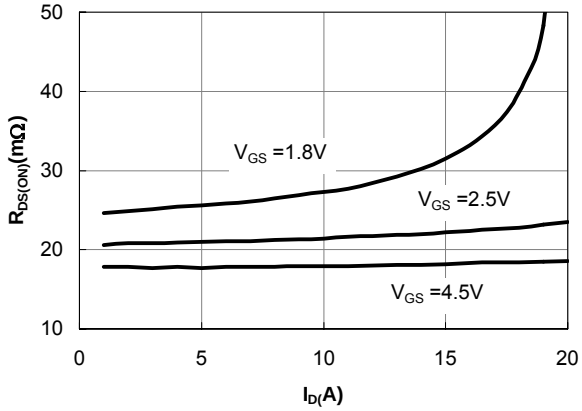


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

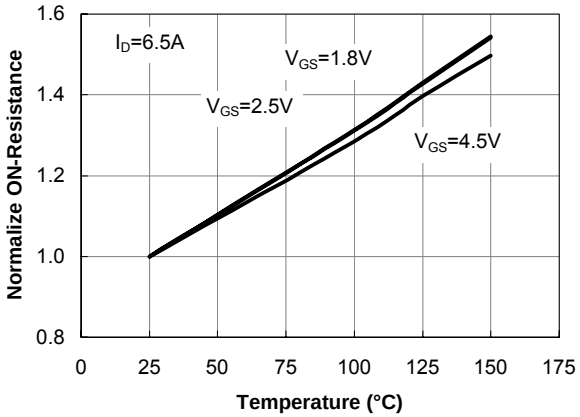


Figure 4: On-Resistance vs. Junction Temperature

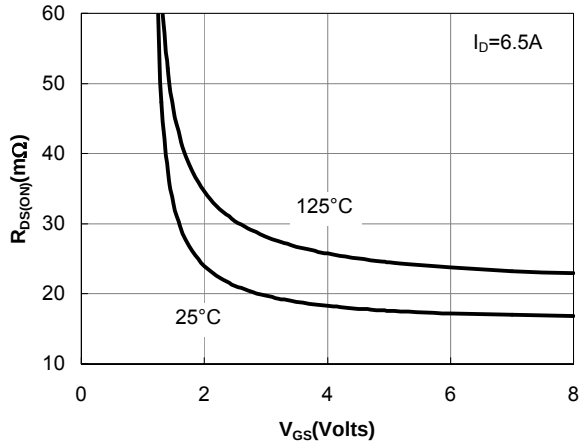


Figure 5: On-Resistance vs. Gate-Source Voltage

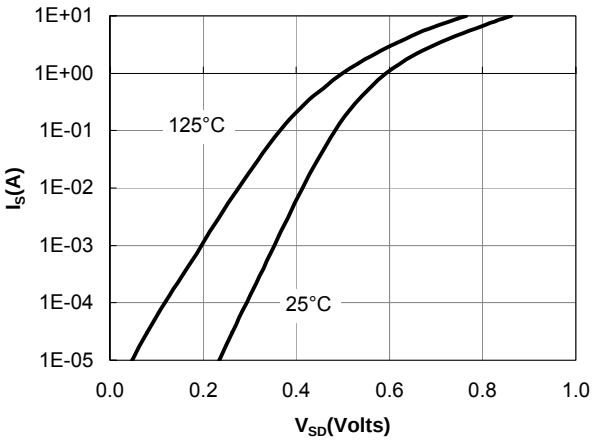


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

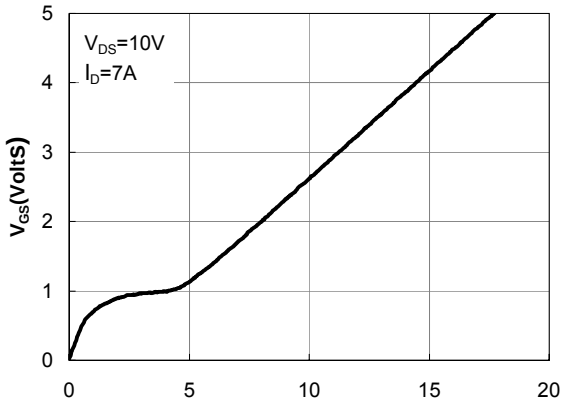


Figure 7: Gate-Charge Characteristics

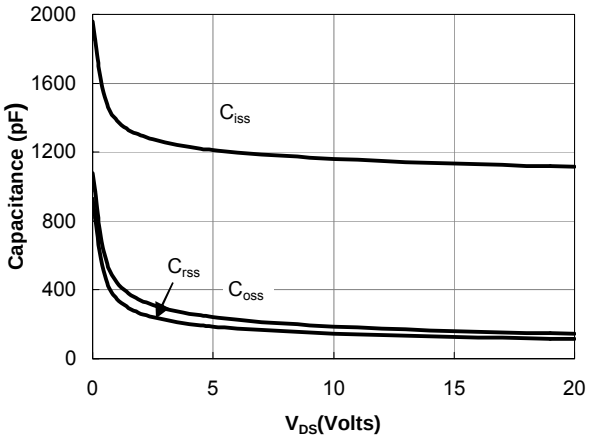


Figure 8: Capacitance Characteristics

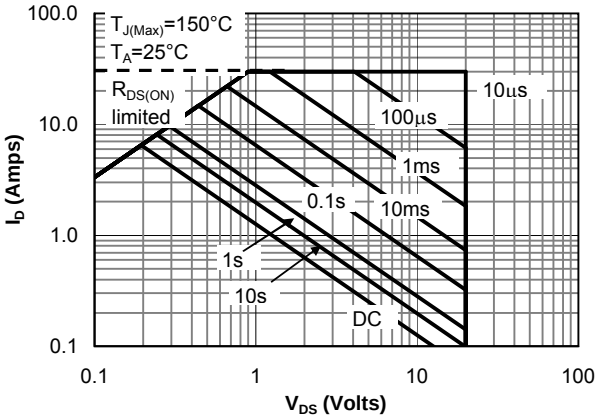


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

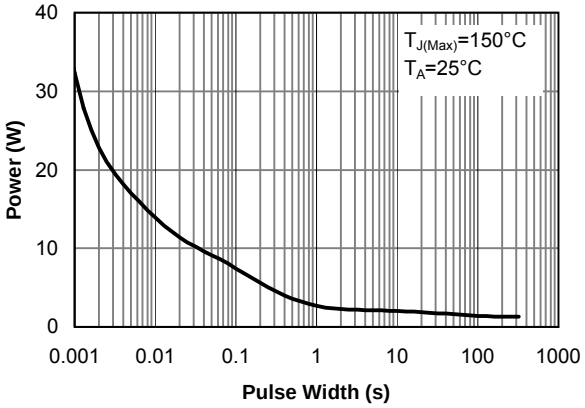


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

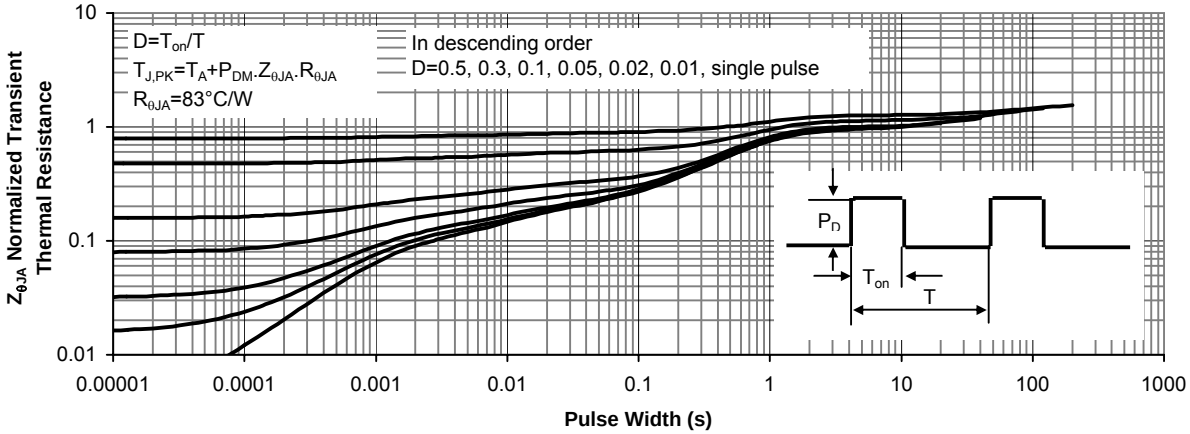


Figure 11: Normalized Maximum Transient Thermal Impedance