

High Voltage NPN Power Transistors (3A, 1500V)

FEATURES

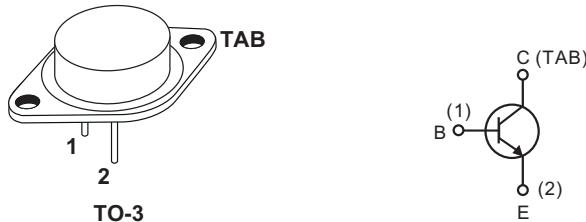
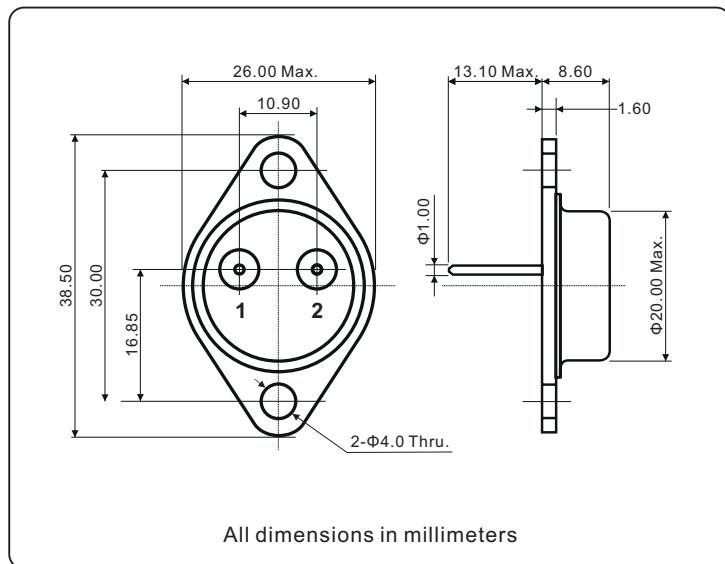
- High V_{CES} breakdown voltage.
 - High collector peak current
 - High reliability

DESCRIPTION

The **2SD649** is a silicon epitaxial-base mesa NPN transistor mounted in JEDEC TO-3 metal case.

APPLICATIONS

- Designed for line-operated horizontal deflection output



ABSOLUTE MAXIMUM RATINGS (T_C = 25°C unless otherwise specified)

SYMBOL	PARAMETER	VALUE	UNIT
V_{CBO}	Collector to base voltage	1500	V
V_{CES}	Collector to emitter voltage ($V_{BE} = 0$)	1500	
V_{EBO}	Emitter to base voltage ($I_C = 0$)	5	
I_C	Collector current	3	A
I_{CP}	Collector peak current	5	
P_C	Total power dissipation ($T_C \leq 90^\circ\text{C}$)	35	W
T_j	Junction temperature	130	$^\circ\text{C}$
T_{stg}	Storage temperature	-65 to 130	
T_L	Maximum lead temperature for soldering purposes : 1/8" from case for 5 seconds	275	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
◎ OFF CHARACTERISTICS					
I_{CBO}	Collector cutoff current	$V_{CB} = 750\text{V}, I_E = 0$		100	μA
		$V_{CB} = 1500\text{V}, I_E = 0$		1.0	mA
I_{EBO}	Emitter cutoff current	$V_{EB} = 5\text{V}, I_C = 0$		1.0	
$V_{(BR)EBO}$	Emitter to base breakdown voltage	$I_C = 0, I_E = 10\text{mA}$	5		V
$V_{CE(\text{sat})}$	Collector to emitter saturation voltage	$I_C = 3\text{A}, I_B = 1\text{A}$		7.0	
$V_{BE(\text{sat})}$	Base to emitter saturation voltage	$I_C = 3\text{A}, I_B = 1\text{A}$		1.5	
h_{FE}	DC current gain	$I_C = 3\text{A}, V_{CE} = 10\text{V}$	4	12	

INDUCTIVE SWITCHING TIMES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
t_s	Storage time	$I_C = 3\text{A}, L_B = 20\mu\text{H}, I_{Bend} = 1\text{A}$	$T_C = 25^\circ\text{C}$	13		μs
t_f	Fall time	$I_C = 3\text{A}, L_B = 20\mu\text{H}, I_{Bend} = 1\text{A}$		$T_C = 25^\circ\text{C}$	1.0	

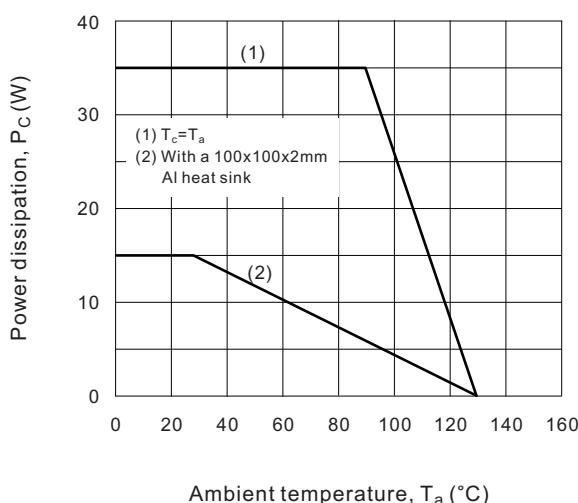
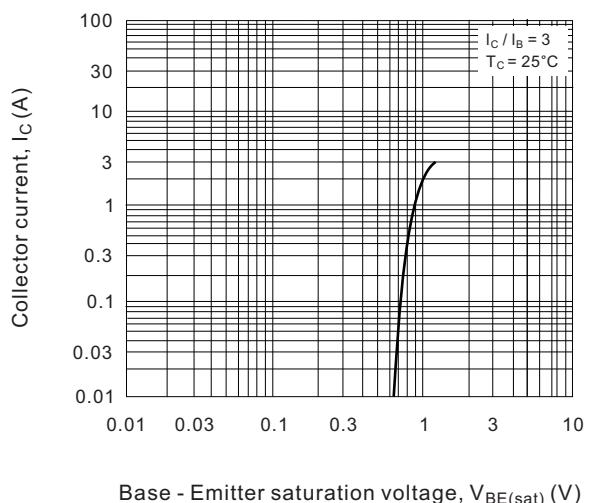
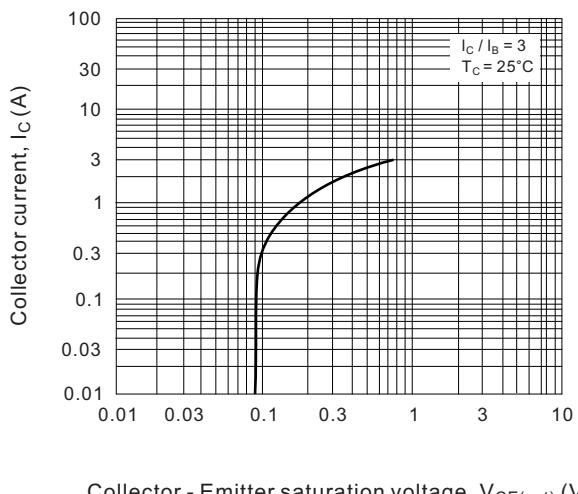
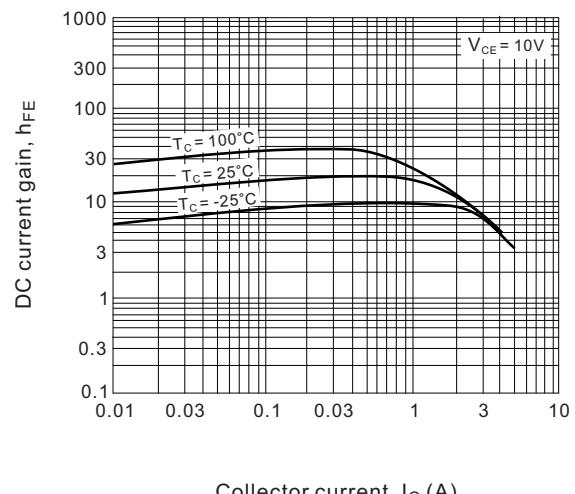
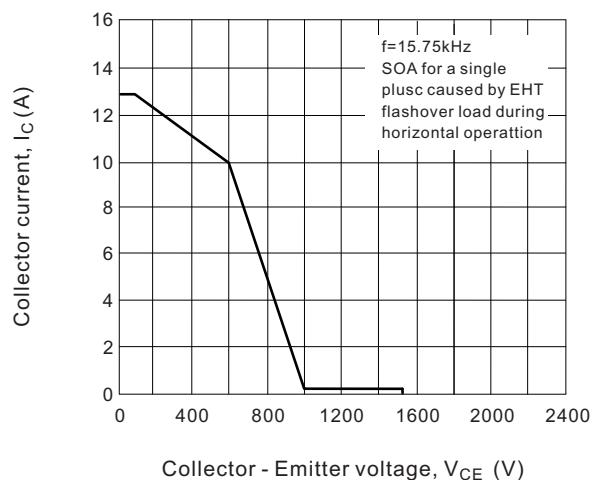
Fig.1 Power dissipation vs. ambient temperature

Fig.2 Base-Emitter saturation voltage


Fig.3 Collector-Emitter saturation voltage

Fig.4 DC current gain

Collector - Emitter saturation voltage, $V_{CE(sat)}$ (V)

Collector current, I_C (A)

Fig.5 Safe operation area

Fig.6 Thermal resistance (from junction to tab)
