

**Sensitive Gate Triacs
Silicon Bidirectional Thyristors**

**TRIACS
8 AMPERES RMS
600 VOLTS**

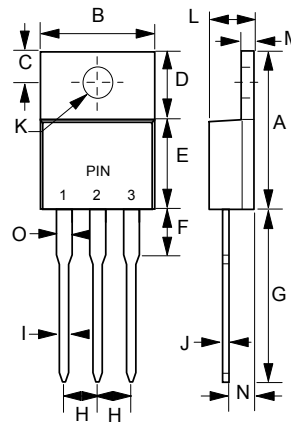
FEATURES

- Sensitive Gate Allows Triggering by Microcontrollers and other Logic Circuits
- Uniform Gate Trigger Currents in Three Quadrants; Q1, Q2, and Q3
- High Immunity to dv/dt - 25 V/ μ s Minimum at 110°C
- High Commutating di/dt - 8.0 A/ms Minimum at 110°C
- Maximum Values of IGT, VGT and IH Specified for Ease of Design
- On-State Current Rating of 8 Amperes RMS at 70°C
- High Surge Current Capability - 70 Amperes
- Blocking Voltage to 800 Volts
- Rugged, Economical TO220AB Package
- Pb-Free Package

MECHANICAL DATA

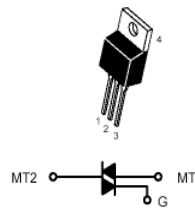
- Case: Molded plastic
- Weight: 0.07 ounces, 2.0 grams

TO-220AB



TO-220AB		
DIM.	MIN.	MAX.
A	14.22	15.88
B	9.65	10.67
C	2.54	3.43
D	5.84	6.86
E	8.26	9.28
F	-	6.35
G	12.70	14.73
H	2.29	2.79
I	0.51	1.14
J	0.40	0.67
K	3.53 \varnothing	4.09 \varnothing
L	3.56	4.83
M	1.14	1.40
N	2.03	2.92
O	1.17	1.37

All Dimensions in millimeter



PIN ASSIGNMENT	
1	Main Terminal 1
2	Main Terminal 2
3	Gate
4	Main Terminal 2

MAXIMUM RATINGS (Tj= 25°C unless otherwise noticed)

Rating	Symbol	Value	Unit
Peak Repetitive Off- State Voltage (1) (Tj= -40 to 110°C, Sine Wave, 50 to 60 Hz; Gate Open)	V _{DRM} , V _{VRRM}	600	Volts
On-State RMS Current (Full Cycle Sine Wave 50 to 60 Hz, Tc =70°C)	I _{T(RMS)}	8.0	Amp
Peak Non-Repetitive Surge Current (One Full Cycle Sine Wave, 60 Hz, Tj= 25°C)	I _{TSM}	70	Amps
Circuit Fusing Consideration (t = 8.3 ms)	I ² t	20	A ² s
Peak Gate Power (Tc = 70°C, Tp ≤1.0 us)	P _{GM}	16	Watt
Average Gate Power (Tc = 70°C, t = 8.3 ms)	P _{G(AV)}	0.35	Watt
Operating Junction Temperature Range	T _J	-40 to +110	°C
Storage Temperature Range	T _{stg}	-40 to +150	°C

Notice: (1) V_{DRM} and V_{VRRM} for all types can be applied on a continuous basis. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

REV. 7, Dec-2010, KTXC08

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance - Junction to Case - Junction to Ambient	RthJC RthJA	2.2 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 10 Seconds	TL	260	°C

ELECTRICAL CHARACTERISTICS (T_J=25°C unless otherwise noted; Electrical apply in both directions)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Peak Repetitive Forward or Reverse Blocking Current (V _D =Rated V _{DRM} , V _{RRM} ; Gate Open)	T _J =25°C	I _{DRM}	----	----	10	µA
	T _J =110°C	I _{RRM}	----	----	2.0	mA

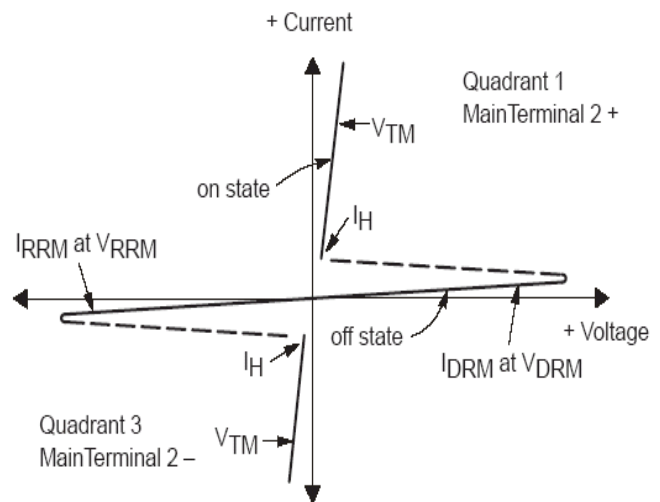
ON CHARACTERISTICS

Peak On-State Voltage (I _{TM} =± 11A Peak @T _p ≤ 2.0 ms, Duty Cycle ≤ 2%)	V _{TM}	----	----	1.85	Volts
Gate Trigger Current (V _D = 12V; R _L = 100 Ohms)	I _{GT1}	----	2.0	5.0	mA
	I _{GT2}	----	3.0	5.0	
	I _{GT3}	----	3.0	5.0	
Gate Trigger Voltage (V _D = 12 V; R _L =100 Ohms)	V _{GT1}	0.45	0.62	1.5	Volts
	V _{GT2}	0.45	0.60	1.5	
	V _{GT3}	0.45	0.65	1.5	
Latching Current (V _D = 24 V, I _G = 5 mA)	I _{L1}	----	5.0	15	mA
	I _{L2}	----	10	20	
	I _{L3}	----	5.0	15	
Holding Current (V _D = 12 V, Initiating Current = ± 150 mA, Gate Open)	I _H	----	3.0	10	mA

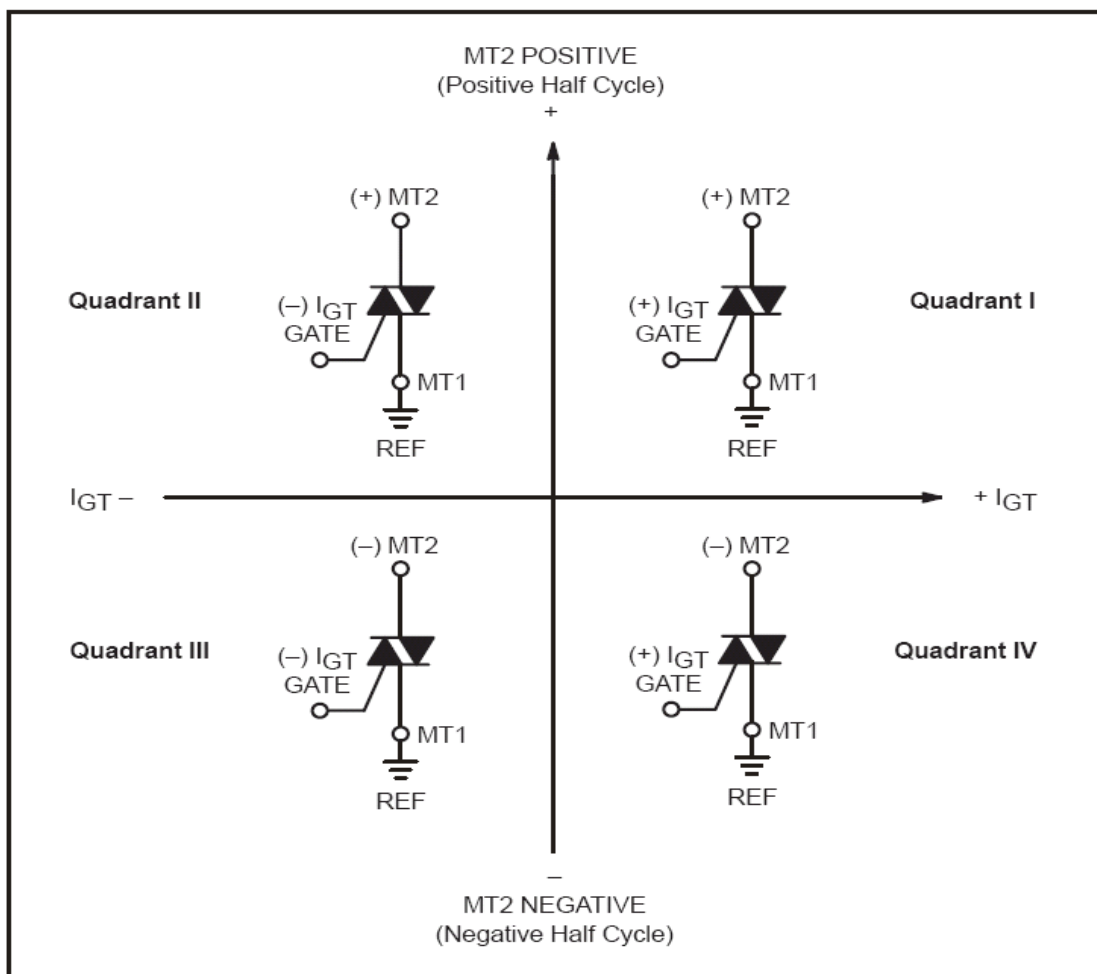
DYNAMIC CHARACTERISTICS

Critical Rate of Rise of Off-State Voltage (V _D = Rated V _{DRM} , Exponential Waveform, R _{GK} =510 Ohms, T _J =110°C)	dv/dt	25	75	----	V/µs
Rate of Change of Commutating Current (V _D = 400 V, I _{TM} = 3.5A, Commutating dv/dt = 10 V/µs, Gate Open, T _J = 110°C, f = 500 Hz, C _s = 0.01 µF, R _s = 15 Ohms)	di/dt(c)	8.0	10	----	A/ms

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I_{DRM}	Peak Forward Blocking Current
V_{RRM}	Peak Repetitive Reverse Off State Voltage
I_{RRM}	Peak Reverse Blocking Current
V_{TM}	Maximum On State Voltage
I_H	Holding Current



Quadrant Definitions



All polarities are referenced to MT1

Whith in -phase signal (using standard AC lines) quadrants I and III are used

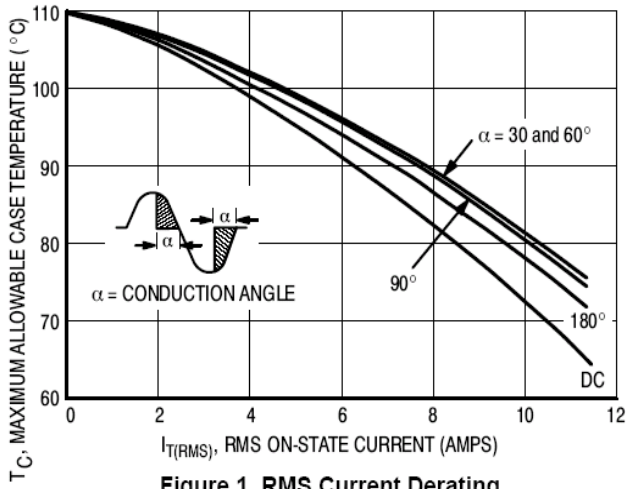


Figure 1. RMS Current Derating

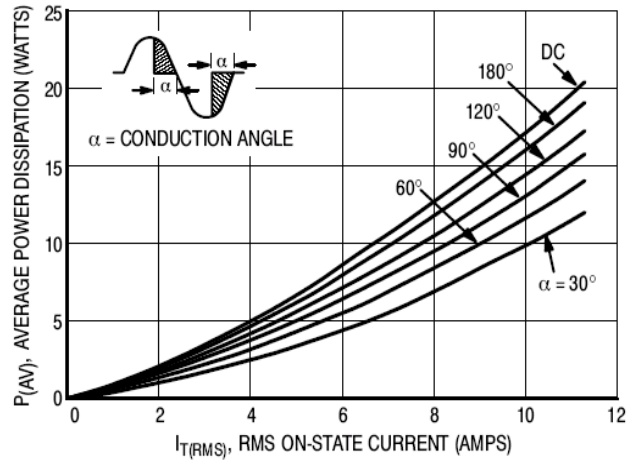


Figure 2. Maximum On-State Power Dissipation

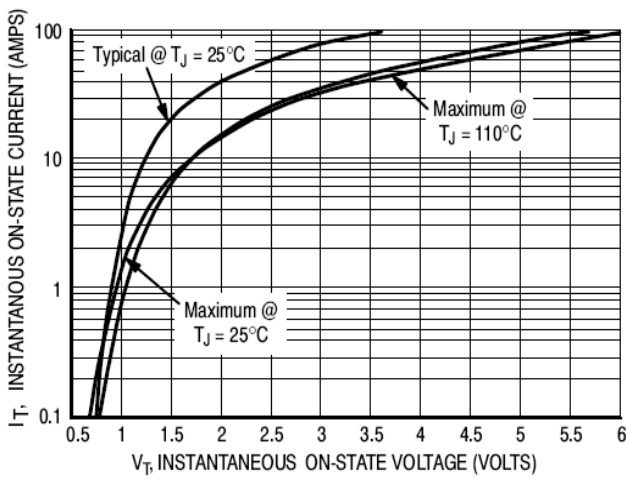


Figure 3. On-State Characteristics

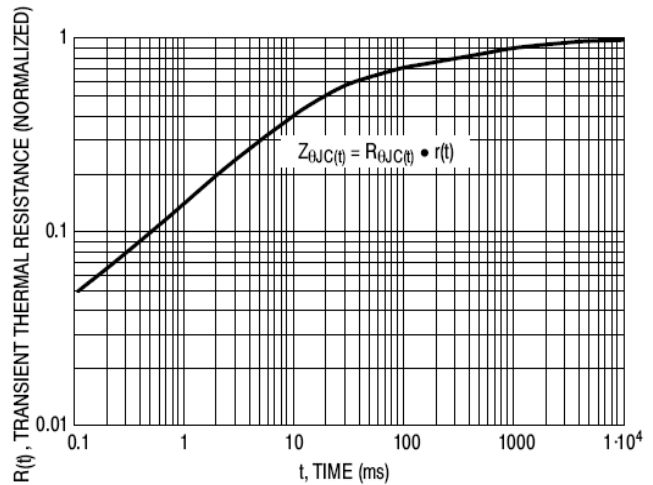


Figure 4. Transient Thermal Response

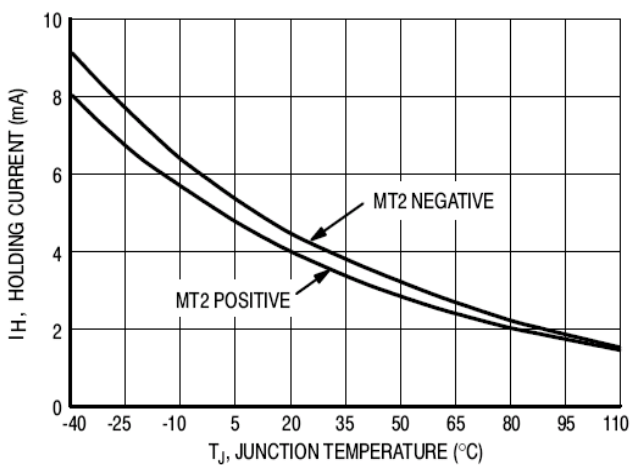


Figure 5. Typical Holding Current Versus Junction Temperature

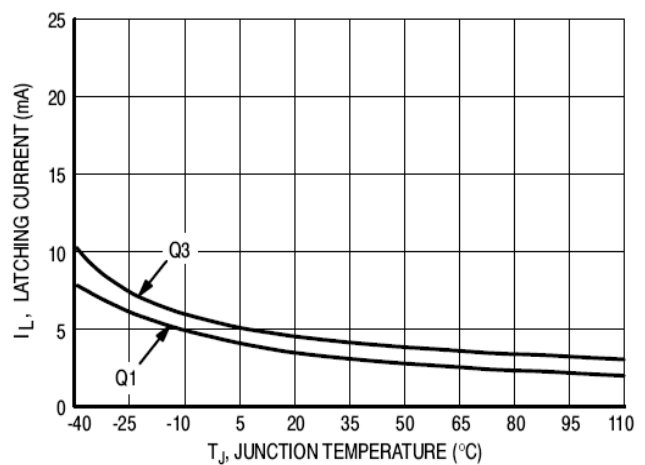


Figure 6. Typical Latching Current Versus Junction Temperature

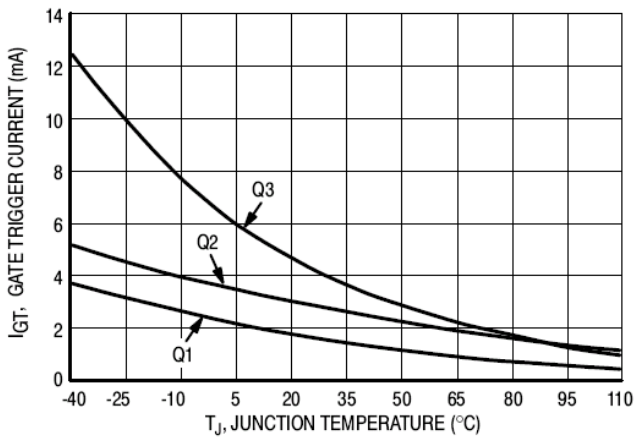


Figure 7. Typical Gate Trigger Current Versus Junction Temperature

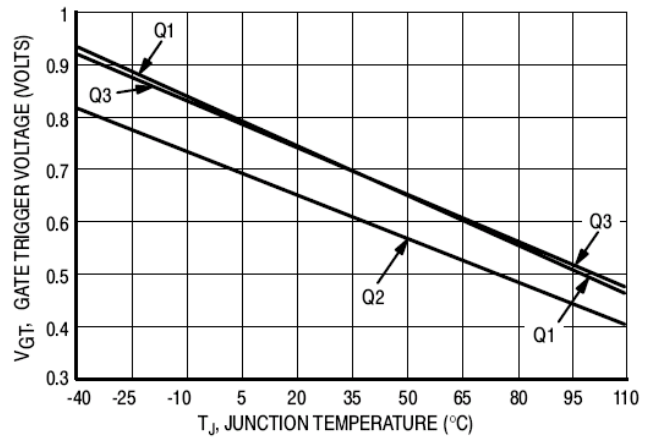


Figure 8. Typical Gate Trigger Voltage Versus Junction Temperature

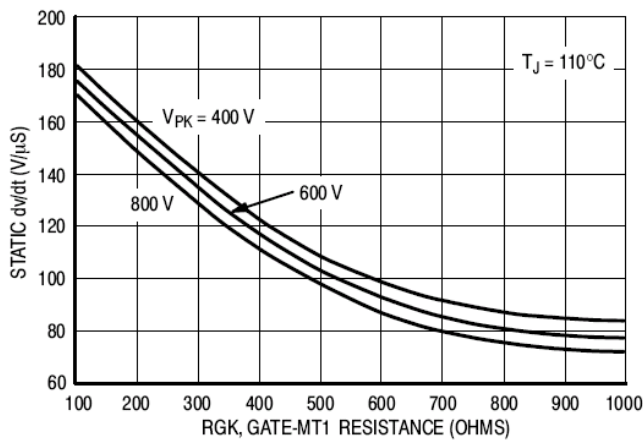


Figure 9. Typical Exponential Static dv/dt Versus Gate-MT1 Resistance, MT2(+)

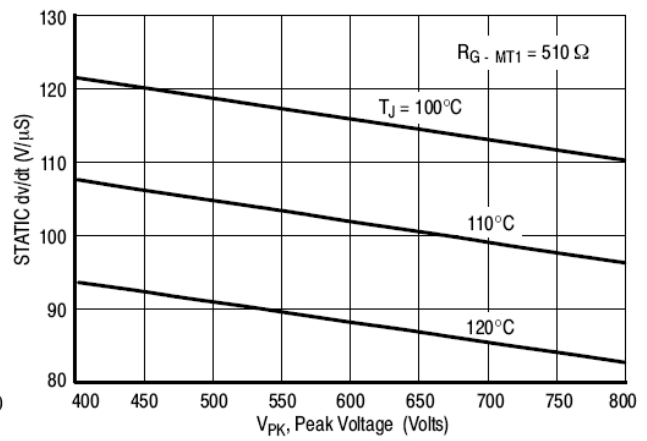


Figure 10. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(+)

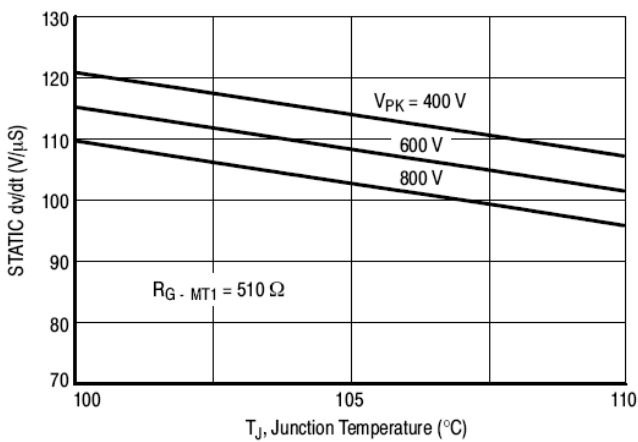


Figure 11. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(+)

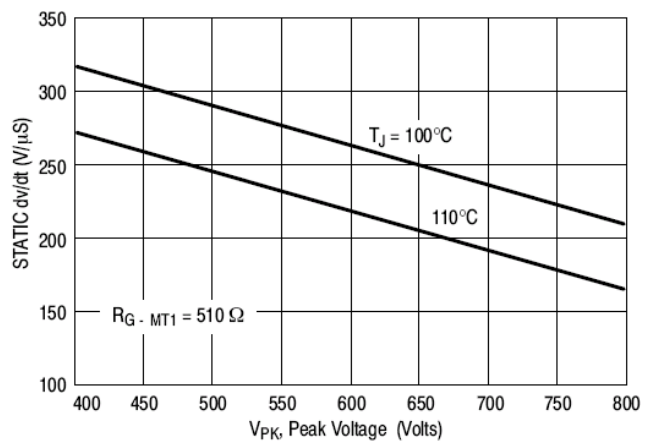


Figure 12. Typical Exponential Static dv/dt Versus Peak Voltage, MT2(-)

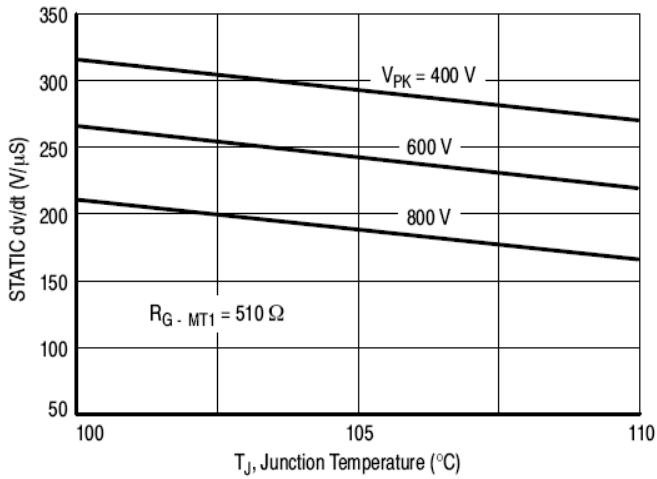


Figure 13. Typical Exponential Static dv/dt Versus Junction Temperature, MT2(-)

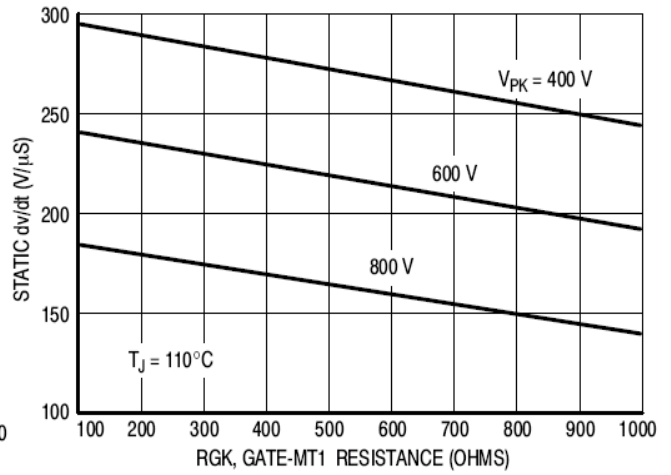


Figure 14. Typical Exponential Static dv/dt Versus Gate-MT1 Resistance, MT2(-)

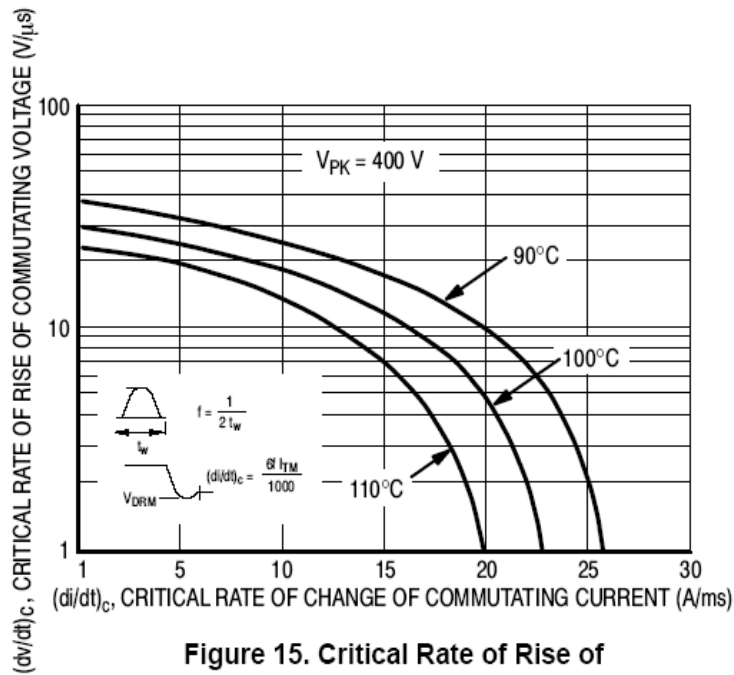


Figure 15. Critical Rate of Rise of Commutating Voltage

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