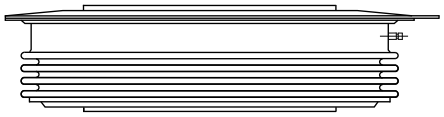
Phase Control Thyristors (Hockey PUK Version), 3370A

FEATURES

- Center amplifying gate
- Metal case with ceramic insulator
- International standard case Nell's DX-type Capsule
- Compliant to RoHS
- Low on-state and switching losses
- Designed and qualified for industrial level



Nell's DX-type Capsule

TYPICAL APPLICATIONS

- DC and AC motor controls
- Controlled DC power supplies
- AC controllers

PRODUCT SUMMARY	
$I_{T(AV)}$	3370A

MAJOR RATINGS AND CHARACTERISTICS			
PARAMETER	**TEST CONDITIONS**	**VALUES**	**UNIT**
$I_{T(AV)}$	Double side cooled, single phase, 50Hz, 180° half-sine wave	3370	A
	T_{hs}	70	°C
$I_{T(RMS)}$		12100	A
	T_{hs}	25	°C
I_{TSM}	50 HZ	49000	kA
	60 HZ	51300	
I^2t	50 HZ	12005	kA^2s
	60 HZ	10922	
V_{DRM}/V_{RRM}		1200 to 1600	V
T_q	Typical	200	μs
T_J		-40 to 125	°C

ELECTRICAL SPECIFICATIONS

VOLTAGE RATINGS				
TYPE NUMBER	**VOLTAGE CODE**	**V_{DRM}/V_{RRM}, MAXIMUM REPETITIVE PEAK AND OFF-STATE VOLTAGE V**	**V_{RSM}, MAXIMUM NON-REPETITIVE PEAK REVERSE VOLTAGE V**	**I_{DRM}/I_{RRM}, MAXIMUM AT $T_J = T_J$ MAXIMUM mA**
3370PTxxDX0	12	1200	1300	200
	14	1400	1500	
	16	1600	1700	

FORWARD CONDUCTION						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**			**VALUES**	**UNIT**
Maximum average current at heatsink temperature	$I_{T(AV)}$	180° conduction, half sine wave double side (single side) cooled			3370	A
					70	°C
Maximum RMS on-state current	$I_{T(RMS)}$	DC at 25°C heatsink temperature double side cooled			12800	A
Maximum peak, one cycle non-reptitive surge current	I_{TSM}	t = 10ms	No voltage reapplied	Sinusoidal half wave, initial $T_J = T_J$ maximum	49000	A
		t = 8.3ms			51300	
		t = 10ms	100%V_{RRM} reapplied		41160	
		t = 8.3ms			43090	
Maximum I^2t for fusing	I^2t	t = 10ms	No voltage reapplied		12005	kA^2s
		t = 8.3ms			10922	
		t = 10ms	100%V_{RRM} reapplied		8471	
		t = 8.3ms			7706	
Maximum $I^2\sqrt{t}$ for fusing	$I^2\sqrt{t}$	t = 0.1 to 10 ms, no voltage reapplied			120050	$kA^2\sqrt{s}$
Maximum threshold voltage	$V_{T(TO)}$	I_T = 4200A~12500A, $T_J = T_J$ maximum			0.94	V
Maximum on-state slope resistance	r_t				0.066	mΩ
Maximum on-state voltage	V_{TM}	I_{pk} =4000A, $T_J = T_J$ maximum, t_p = 10 ms sine pulse			1.20	V
Maximum holding current	I_H	T_J = 25°C, anode supply 12V resistive load			600	mA
Typical latching current	I_L				1500	

SWITCHING			
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Maximum non-repetitive rate of rise of turned-on current	dI/dt	I_{TM} = 4000A, $V_D \le 80\%\ V_{DRM}$, I_{FG} = 2A, t_r = 0.3μs, $T_J = T_J$ maximum, f = 50Hz	200	A/μs
Maximum delay time (Gate turn-on delay time)	t_d	V_D = 0.4 V_{DRM}, I_{FG} = 2A, t_r = 0.3μs, T_J = 25°C	2.0	μs
Typical turn-on time	t_g	I_{TM} = 4000A, $T_J = T_J$ maximum, dI/dt = -12.5 A/μs. V_R = 100V, dV/dt = 50 V/μs, $V_D \le 0.67$, V_{DRM}	200	
Reverse recovery charge (Typical)	Q_{rr}	I_{TM} = 4000A, $T_J = T_J$ maximum, V_R = 100V, di/dt = -12.5 A/μs	2800	μC

BLOCKING				
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**VALUES**	**UNIT**
Minimum critical rate of rise of off-state voltage	dV/dt	$T_J = T_J$ maximum, linear to 67% rated V_{DRM}	1000	V/μs
Maximum peak reverse and off-state leakage current	I_{RRM}, I_{DRM},	$T_J = T_J$ maximum, rated V_{DRM}/V_{RRM} applied	200	mA

TRIGGERING

PARAMETER	SYMBOL	TEST CONDITIONS		VALUES TYP.	VALUES MAX.	UNIT
Maximum peak gate power	P_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		25		W
Maximum average gate power	$P_{G(AV)}$	$T_J = T_J$ maximum, f = 50 Hz, d% = 50		5		W
Maximum peak positive gate current	I_{GM}	$T_J = T_J$ maximum, $t_p \leq 5$ ms		10		A
Maximum peak positive gate voltage	$+V_{GM}$	$T_J = T_J$ maximum, $t_p \leq 5$ ms		12		V
Maximum peak negative gate voltage	$-V_{GM}$			10		V
DC gate current required to trigger	I_{GT}	T_J = -40°C	Maximum required gate current/voltage are the lowest value which will trigger all units 12V anode to cathode applied	200	500	mA
		T_J = 25°C		100	250	mA
		T_J = 125°C		50	150	mA
DC gate voltage required to trigger	V_{GT}	T_J = -40°C		2.5	4	V
		T_J = 25°C		1.8	3	V
		T_J = 125°C		1.1	2	V
DC gate current not to trigger	I_{GD}	$T_J = T_J$ maximum	Maximum gate current/ voltage not to trigger is the maximum value which will not trigger any unit with rated V_{DRM} anode to cathode applied	10		mA
DC gate voltage not to trigger	V_{GD}			0.25		V

THERMAL AND MECHANICAL SPECIFICATIONS

PARAMETER	SYMBOL	TEST CONDITIONS	VALUES	UNIT
Maximum operating junction temperature range	T_J		-40 to 125	°C
Maximum storage temperature range	T_{stg}		-40 to 150	°C
Maximum thermal resistance, junction to heatsink	$R_{th(J\text{-}hs)}$	DC operation single side cooled	0.020	K/W
		DC operation double side cooled	0.010	K/W
Maximum thermal resistance, case to heatsink	$R_{th(C\text{-}hs)}$	DC operation single side cooled	0.006	K/W
		DC operation double side cooled	0.003	K/W
Mounting force, ±10%			50000 (5100)	N (kg)
Approximate weight			930	g
Case style		Nell's DX-type Capsule		

△ R_{thJC} CONDUCTION

CONDUCTION ANGEL	SINUSOIDAL CONDUCTION		RECTANGULAR CONDUCTION		TEST CONDUCTIONS	UNITS
	SINGLE SIDE	DOUBLE SIDE	SINGLE SIDE	DOUBLE SIDE		
180°	0.003	0.003	0.002	0.002	$T_J = T_J$ maximum	K/W
120°	0.004	0.004	0.004	0.004		
90°	0.005	0.005	0.005	0.005		
60°	0.007	0.007	0.007	0.007		
30°	0.012	0.012	0.012	0.012		

Note

• The table above shows the increment of thermal resistance $R_{thJ\text{-}hs}$ when devices operate at different conduction angles than DC

Fig.1 Current ratings characteristics

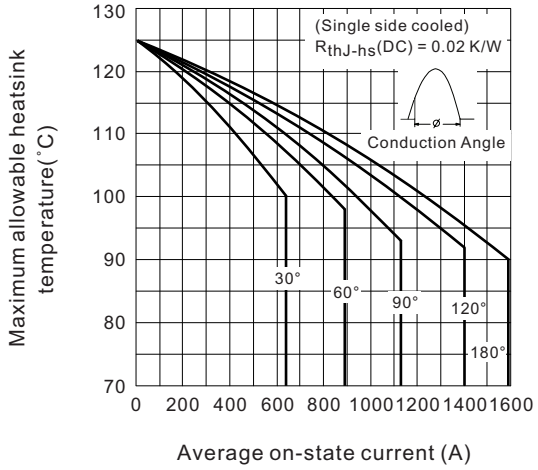


Fig.2 Current ratings characteristics

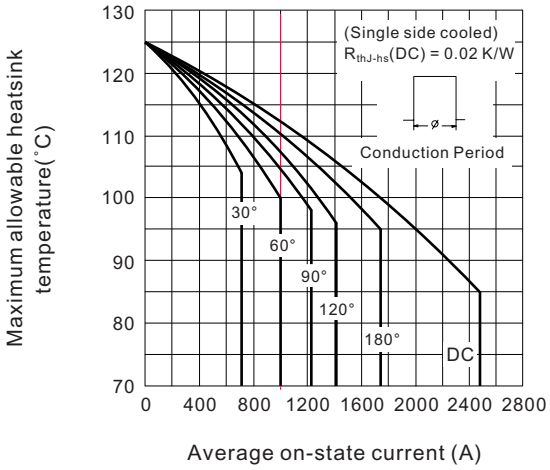


Fig.3 Current ratings characteristics

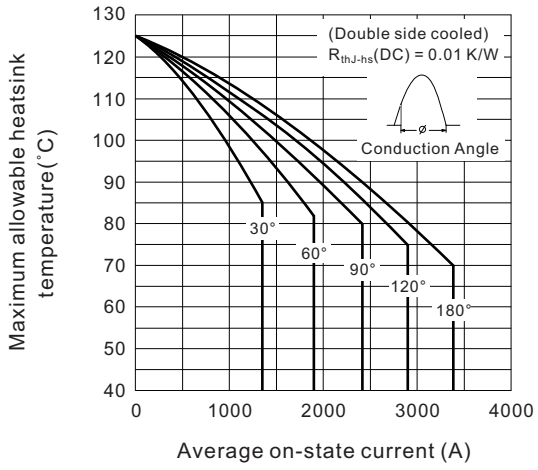


Fig.4 Current ratings characteristics

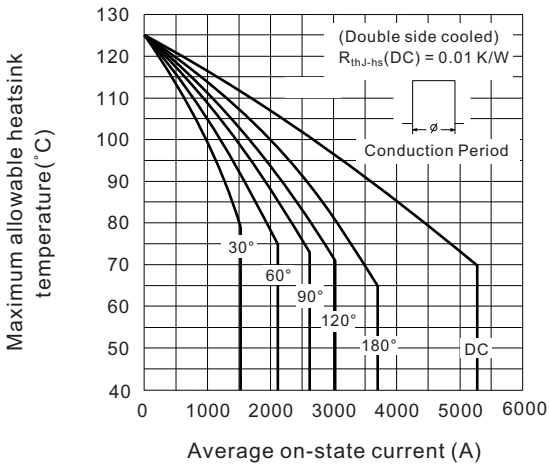


Fig.5 On-state power loss characteristics

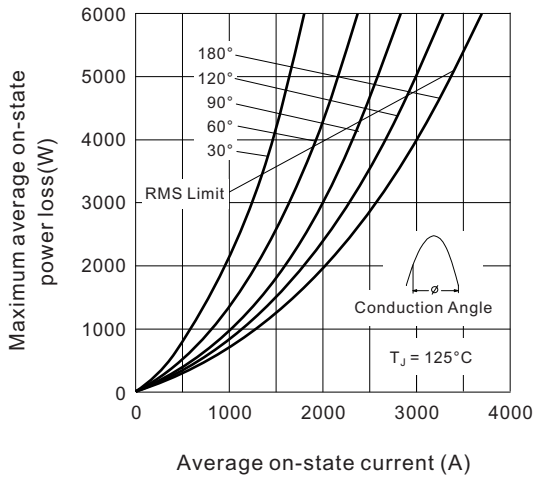


Fig.6 On-state power loss characteristics

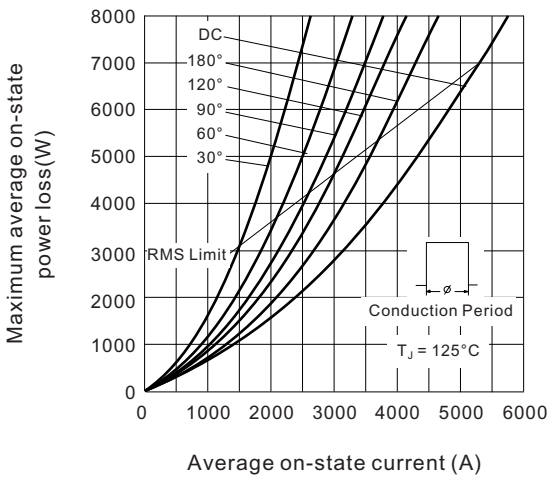


Fig.7 Maximum non-repetitive surge current single and double side cooled

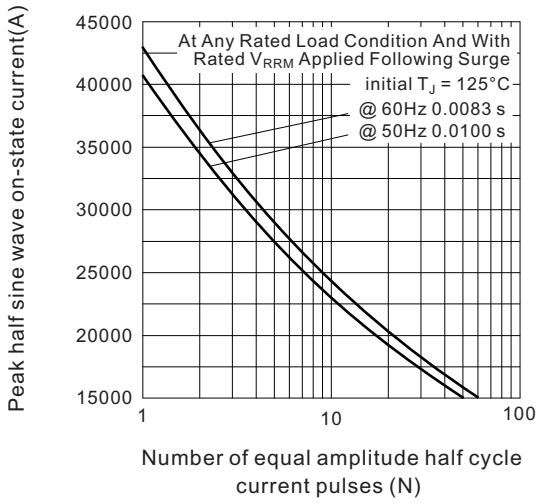


Fig.8 Maximum non-repetitive surge current single and double side cooled

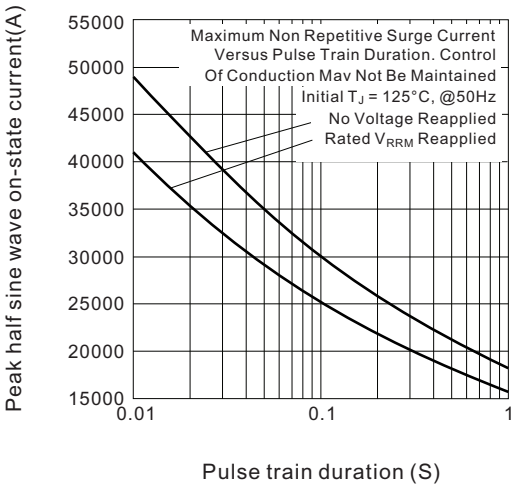


Fig.9 Maximum on-state voltage drop characteristcs

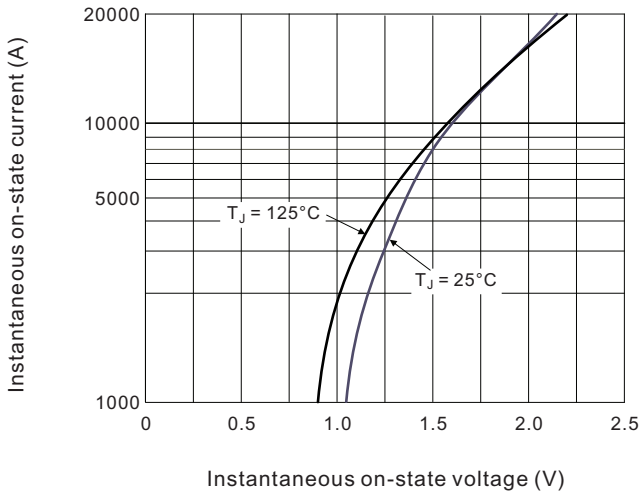


Fig.10 Thermal Impedance $Z_{th(J\text{-}hs)}$ characteristics

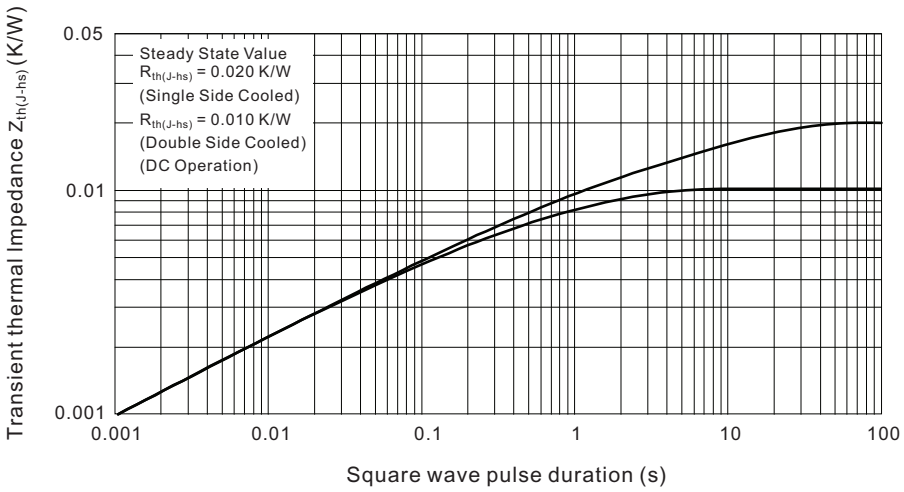


Fig.11 Gate trigger characteristics

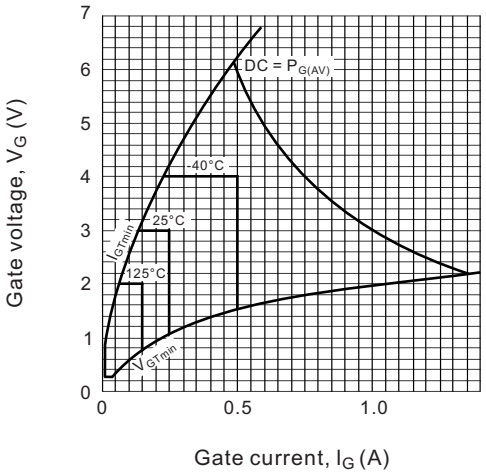
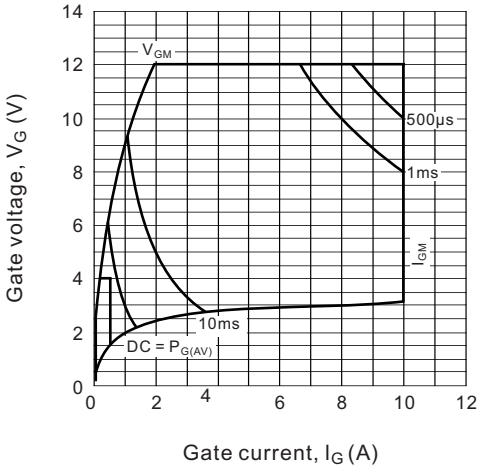


Fig.12 Gate trigger characteristics



ORDERING INFORMATION TABLE

Device code

3370	PT	16	DX	0
①	②	③	④	⑤

1 - Maximum average on-state current $I_{T(AV)}$, 3370 for 3370A

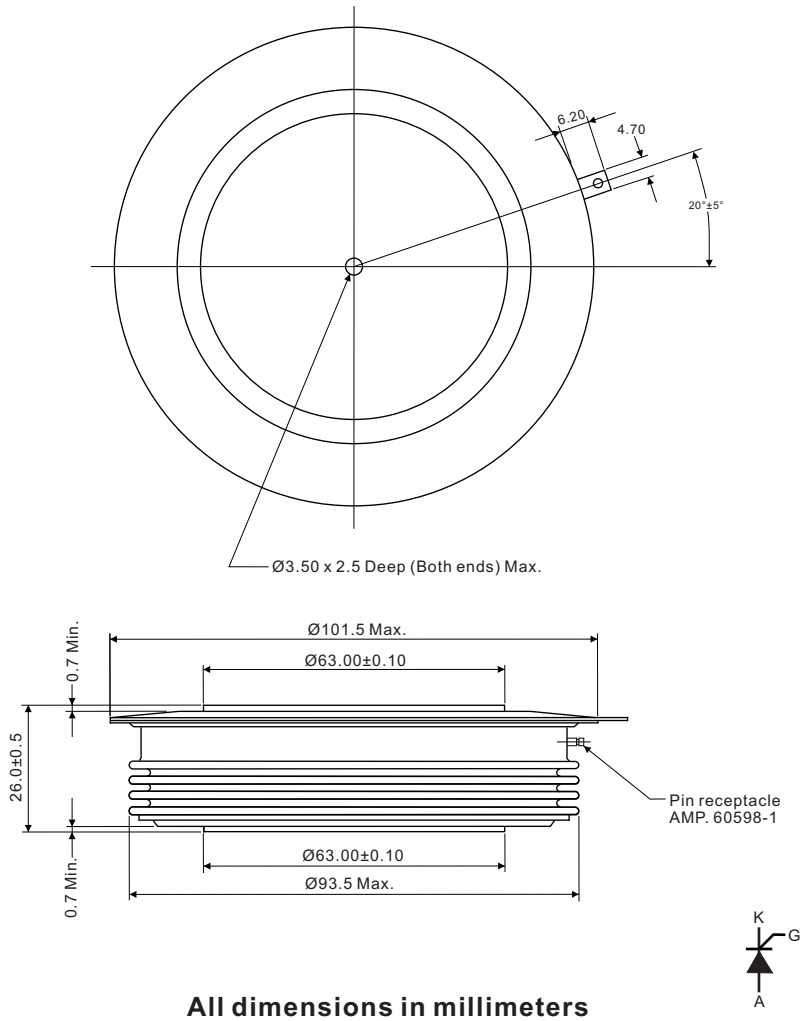
2 - PT = Phase control thyristor

3 - Voltage code, cold × 100 = V_{RRM}/V_{RRM}

4 - DX = Nell's DX-type Capsule

5 - Terminal type, "0" for eyelet

NELL'S DX-type Capsule



All dimensions in millimeters