

MS13N50

500V N-Channel MOSFET

Description

The MS13N50 is a N-channel enhancement-mode MOSFET, providing the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness. The TO-220 package is universally preferred for all commercial-industrial applications

Features

- Originative New Design
- Very Low Intrinsic Capacitances
- Excellent Switching Characteristics
- 100% EAS Test
- Extended Safe Operating Area
- RoHS compliant package

Application

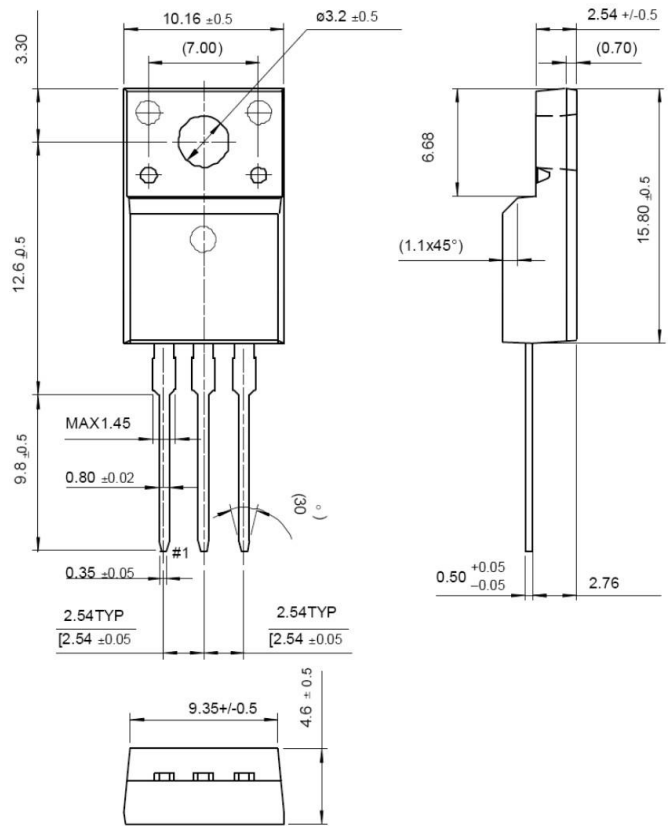
- Electronic lamp ballasts
- based on half bridge topology
- PFC (Power Factor Correction)
- SMPS (Switched Mode Power Supplies)

Packing & Order Information

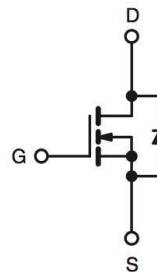
50/Tube ; 1,000/Box



RoHS
COMPLIANT



Graphic symbol



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage	500	V
V _{GS}	Gate-Source Voltage	±30	V
I _D	Drain Current -Continuous (TC=25°C)	13	A
	Drain Current -Continuous (TC=100°C)	8	A
I _{DM}	Drain Current -Pulsed	52	A
E _{AS}	Avalanche Energy	803	mJ
E _{AR}	Repetitive Avalanche Energy	19.5	mJ
P _D	Power Dissipation (TC=25°C)	195	W
	Power Dissipation (TC=100°C)	1.56	W/°C

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Absolute Maximum Ratings (Tc=25°C unless otherwise specified)

Symbol	Parameter	Value	Unit
T_J/T_{STG}	Operating Junction and Storage Temperature	-55 to +175	°C

Note:

1. Pulse width limited by maximum junction temperature
2. Duty cycle $\leq 1\%$

Thermal Resistance Characteristics

Symbol	Parameter	Typ.	Max.	Units
R_{thjc}	Typical thermal resistance	--	0.64	°C/W
$R_{\theta JA}$		--	62.5	

Static Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 250\mu\text{A}$	500	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	$I_D = 250\mu\text{A}$, Referenced to 25°C	--	0.50	--	V/°C
V_{GS}	$V_{DS} = V_{GS}, I_D = 250\mu\text{A}$	2.0		4.0	V
G_{FS}	$V_{DS} = 40\text{ V}, I_D = 6.5\text{ A}$			15	S
I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 400\text{ V}, V_{GS} = 0\text{ V}, T_J = 125^\circ\text{C}$	--	--	1 10	μA
I_{GSS}	$V_{GS} = \pm 30$	--	--	± 100	nA
* $R_{DS(ON)}$	$V_{GS} = -10\text{ V}, I_D = 6.5\text{ A}$	--	3.8	4.8	Ω

Dynamic Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
Q_g	$V_{DS} = 400\text{ V}, I_D = 13\text{ A},$ $V_{GS} = 10\text{ V}$	--	43	56	nC
Q_{gs}		--	7.5	10	nC
Q_{gd}		--	18.5	24	nC
$t_{d(on)}$	$V_{DS} = 250\text{ V}, I_D = 13\text{ A},$ $R_G = 25\ \Omega$	--	25	57.5	ns
t_r		--	100	220	ns
$t_{d(off)}$		--	130	273	ns
t_f		--	100	220	ns
C_{ISS}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	--	1580	2054	pF
C_{OSS}		--	180	234	pF
C_{RSS}		--	20	28	pF

Source-Drain Diode Characteristics

Symbol	Test Conditions	Min	Typ.	Max.	Units
I_S		--	--	13	A
I_{SM}		--	--	52	

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V_{SD}	$I_F = I_S, V_{GS} = 0$	--	--	1.4	V
t_{rr}	$I_F = I_S, diF/dt=100A/\mu s$	--	410	--	ns
Q_{rr}		--	4.5	--	μC

Notes:

1. Repeativity rating : pulse width limited by junction temperature
2. $L=9.5mH, I_{AS}=13A, V_{DD}=50V, R_G=25\Omega, \text{Starting } T_J=25^\circ C$
3. $I_{SD} \leq 13A, di/dt \leq 200A/\mu s, V_{DD} \leq BVDSS, \text{Starting } T_J = 25^\circ C$
4. Pulse Test : Pulse Width $\leq 300\mu s, \text{Duty Cycle} \leq 2\%$
5. Essentially independent of operating temperature.

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Characteristics Curve

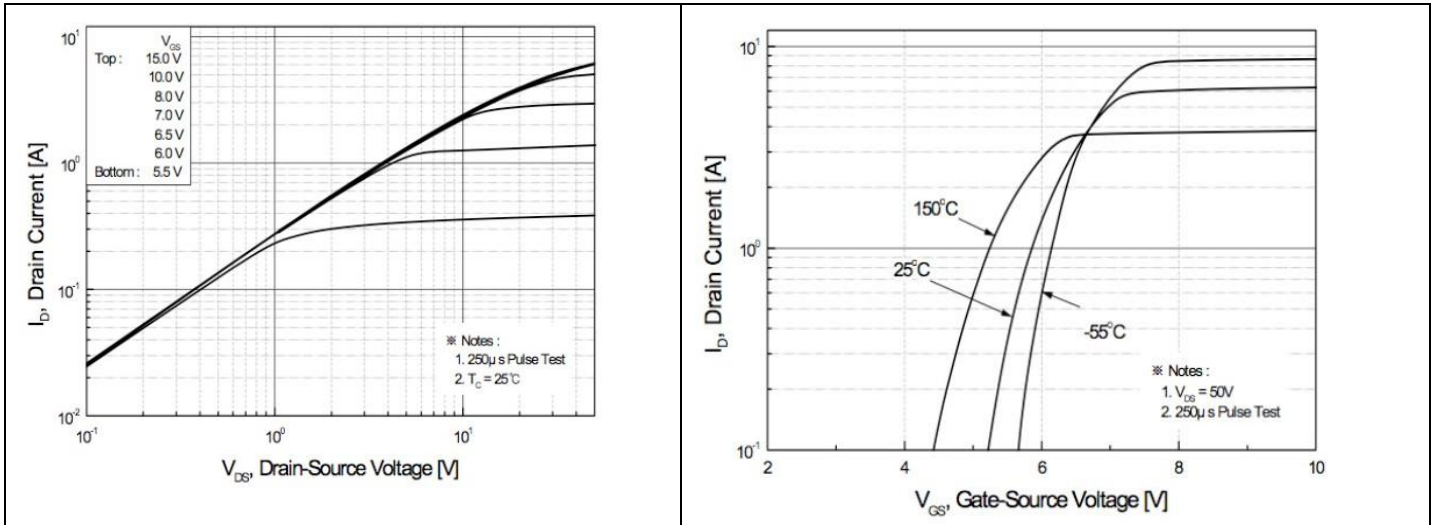


FIG.1-ON REGION CHARACTERISTICS

FIG.2-TRANSFER CHARACTERISTICS

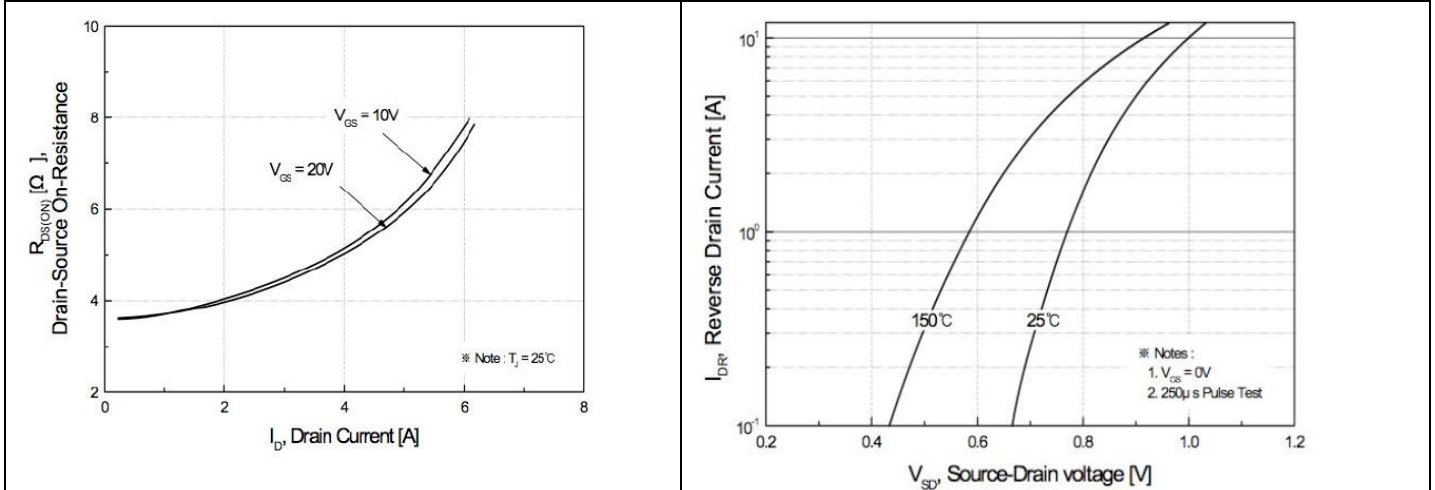


FIG.3-ON RESISTANCE VARIATION VS DRAIN CURRENT AND GATE VOLTAGE

FIG.4-BODY DIODE FORWARD VOLTAGE VARIATION WITH SOURCE CURRENT AND TEMPERATURE

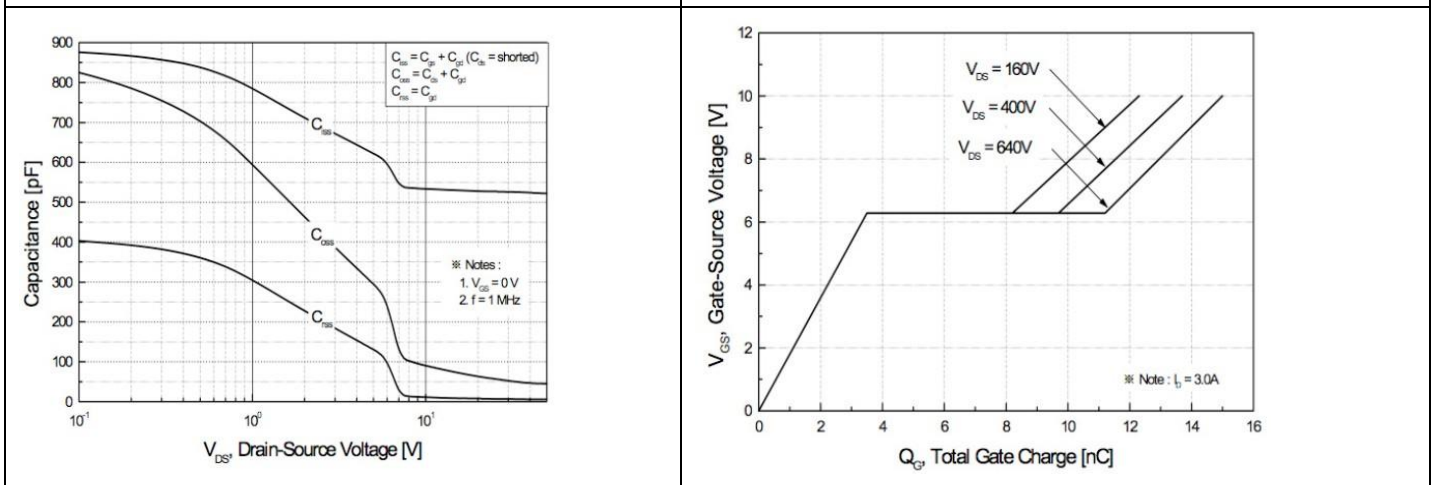


FIG.5-CAPACITANCE CHARACTERISTICS

FIG.6-GATE CHARGE CHARACTERISTICS

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■ Characteristics Curve

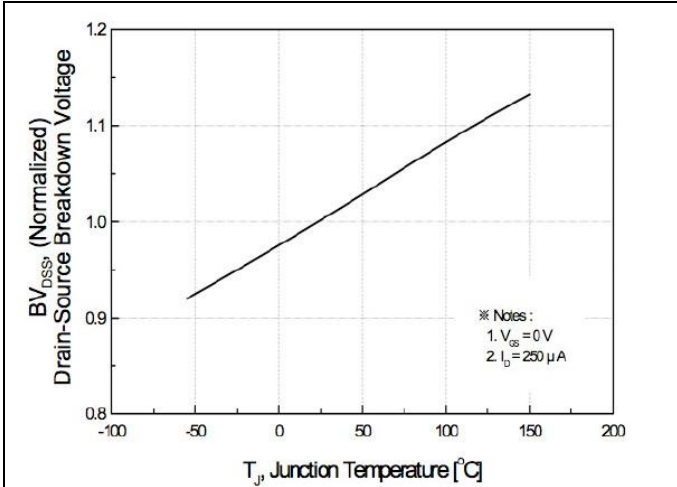


FIG.7-BREAKDOWN VOLTAGE VARIATION VS TEMPERATURE

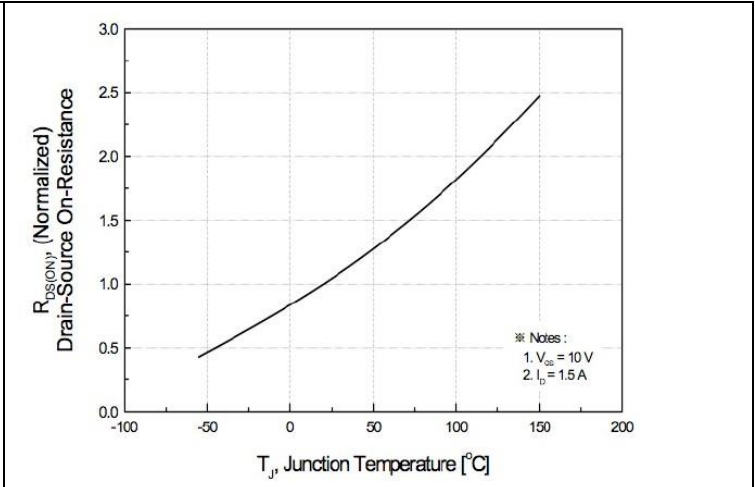


FIG.8-ON-RESISTANCE VARIATION VS TEMPERATURE

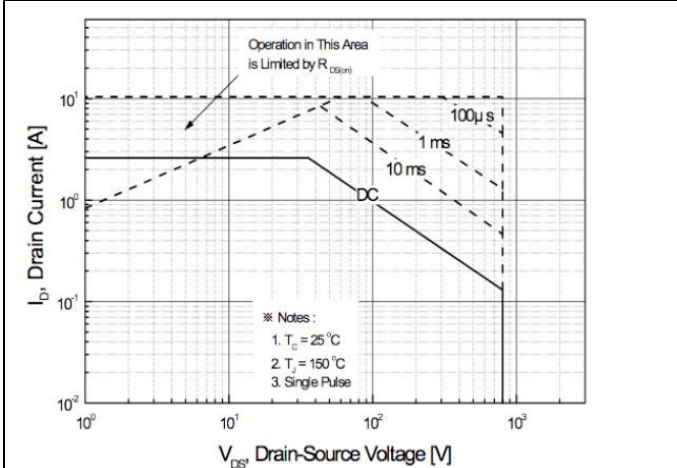


FIG.9-MAXIMUM SAFE OPERATING AREA

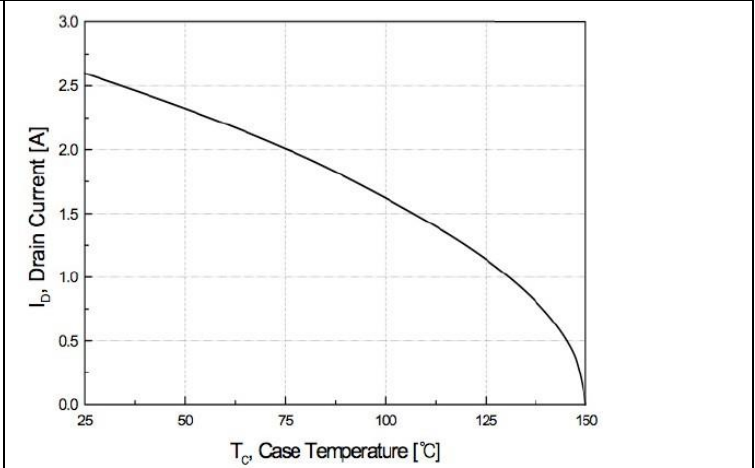


FIG.10-MAXIMUM DRAIN CURRENT VS CASE TEMPERATURE

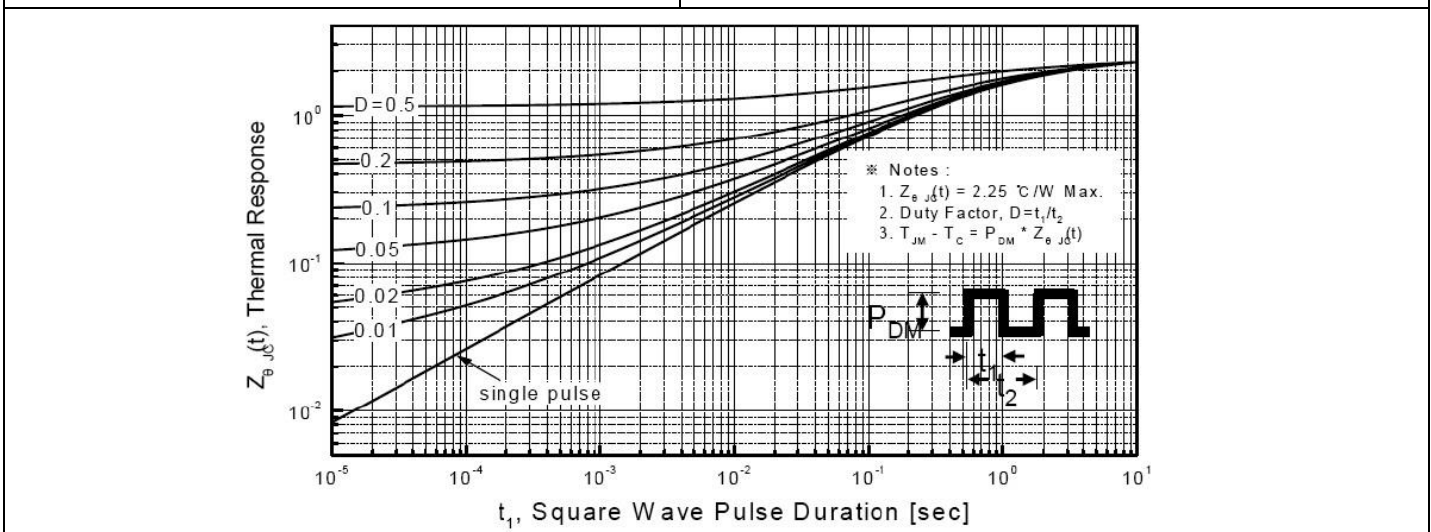


FIG.11-TRANSIENT THERMAL RESPONSE CURVE

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■ Characteristics Test Circuit & Waveform

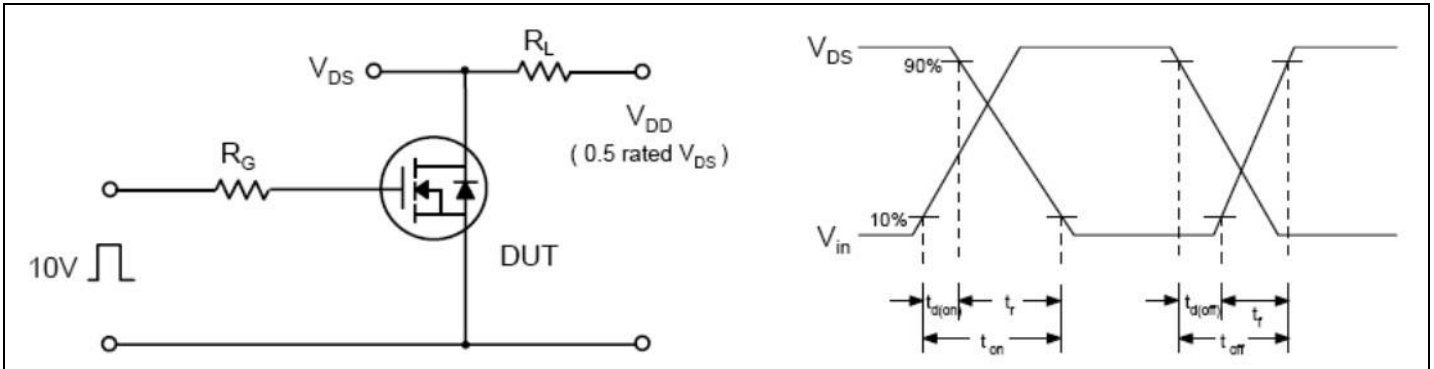


FIG.12-RESISTIVE SWITCHING TEST CIRCUIT & WAVEFORMS

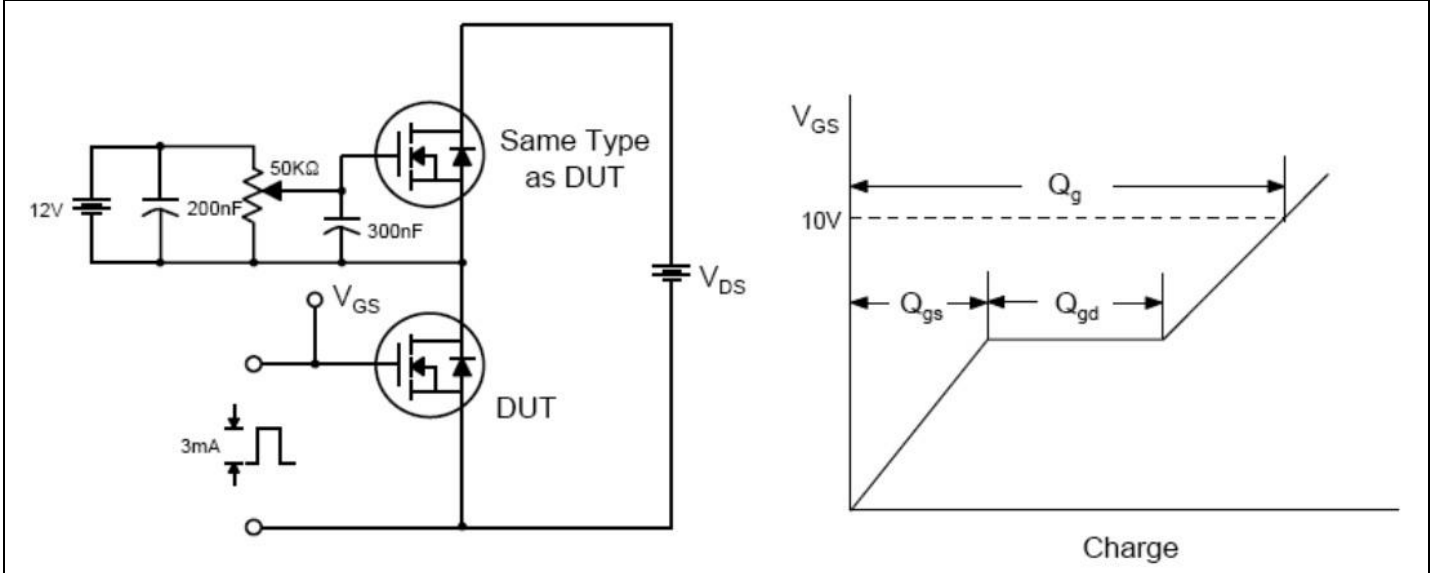


FIG.13-GATE CHARGE TEST CIRCUIT & WAVEFORM

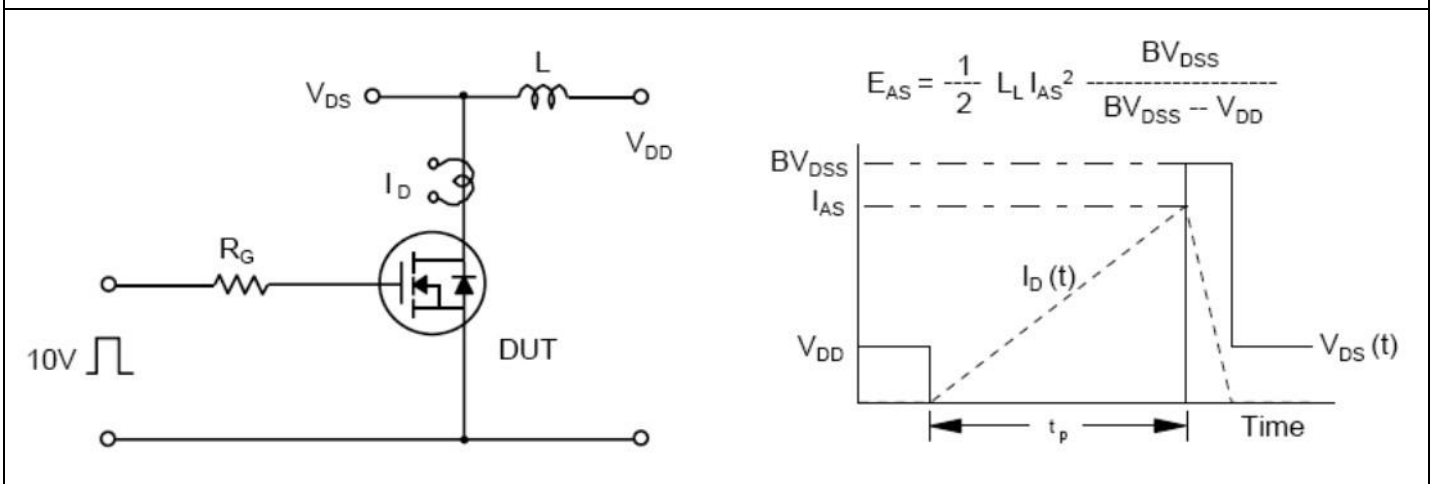


FIG.14-UNCLAMPED LINDUCTIVE SWITCHING TEST CIRCUIT & WAVEFORMS

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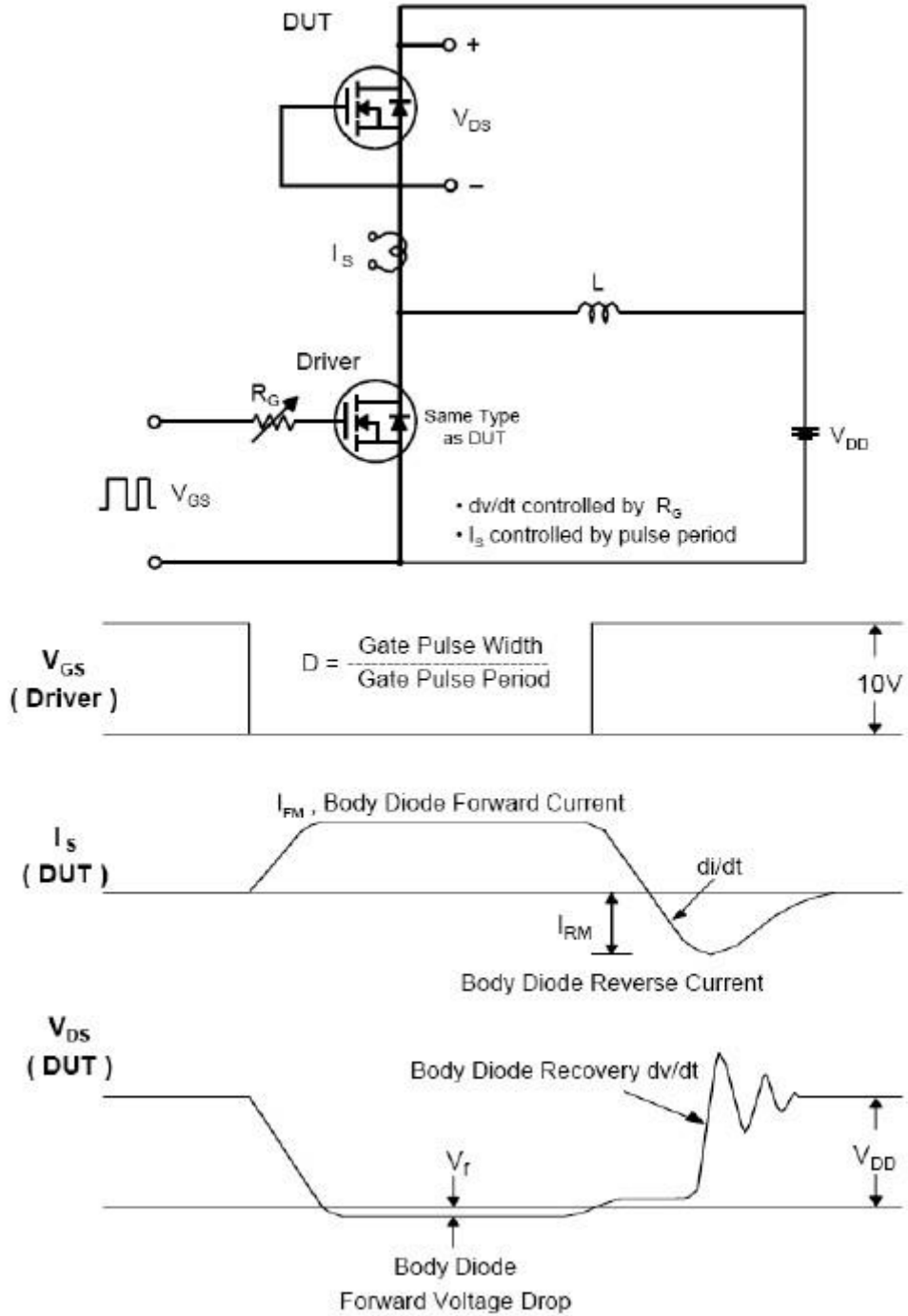


Fig 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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