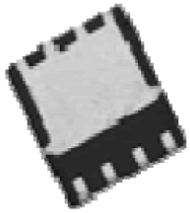
MS40N06 60V N-Channel MOSFET

GENERAL DESCRIPTION

The MS40N06 is the highest performance trench N-ch MOSFETs with extreme high cell density , which provide excellent RDSON and gate charge for most of the synchronous buck converter applications .

The QM6006M6 meet the RoHS and Green Product requirement , 100% EAS guaranteed with full function reliability approved.



RoHS COMPLIANT

HALOGEN FREE Avaliable

FEATURES

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

Symbol	Parameter	Rating		Units
VDS	Drain-Source Voltage	60		V
VGS	Gate-Source Voltage	±20		V
ID@TC=25°C	Continuous Drain Current, VGS @ 10V[1]	40		A
ID@TC=100°C	Continuous Drain Current, VGS @ 10V[1]	25		A
ID@TA=25°C	Continuous Drain Current, VGS @ 10V[1]	7.4		A
ID@TA=70°C	Continuous Drain Current, VGS @ 10V[1]	6		A
IDM	Pulsed Drain Current[2]	80		A
EAS	Single Pulse Avalanche Energy[3]	67		mJ
IAS	Avalanche Current	28		A
PD@TC=25°C	Total Power Dissipation[4]	59		W
PD@TA=25°C	Total Power Dissipation[4]	2		W
TSTG	Storage Temperature Range	-55 to 150		°C
TJ	Operating Junction Temperature Range	-55 to 150		°C
Symbol	**Parameter**	**Typ.**	**Max.**	**Unit**
RθJA	Thermal Resistance Junction-Ambient [1]	---	62	°C/W
RθJC	Thermal Resistance Junction-Case[1]	---	2.1	°C/W

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Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	VGS=0V , ID=250uA	60	---	---	V
$\triangle BV_{DSS}/\triangle T_J$	BV_{DSS} Temperature Coefficient	Reference to 25°C, ID=1mA	---	0.057	---	V/°C
$R_{DS(ON)}$	Static Drain-Source On-Resistance[2]	VGS=10V , ID=30A	---	14	18	mΩ
		VGS=4.5V , ID=15A	---	16	20	
$V_{GS(th)}$	Gate Threshold Voltage	VGS=VDS , ID =250uA	1.2	---	2.5	V
$\triangle V_{GS(th)}$	VGS(th) Temperature Coefficient		---	-5.68	---	mV/°C
I_{DSS}	Drain-Source Leakage Current	VDS=48V , VGS=0V , TJ=25°C	---	---	1	uA
		VDS=48V , VGS=0V , TJ=55°C	---	---	5	
I_{GSS}	Gate-Source Leakage Current	VGS=±20V , VDS=0V	---	---	±100	nA
gfs	Forward Transconductance	VDS=5V , ID=30A	---	35.2	---	S
Rg	Gate Resistance	VDS=0V , VGS=0V , f=1MHz	---	1.7	3.4	Ω
Qg	Total Gate Charge (4.5V)	VDS=48V , VGS=4.5V , ID=15A	---	19.3	27	nC
Q_{gs}	Gate-Source Charge		---	7.1	10	
Q_{gd}	Gate-Drain Charge		---	7.6	10.6	
$T_{d(on)}$	Turn-On Delay Time	VDD=30V , VGS=10V , RG=3.3Ω, ID=15A	---	7.2	14.4	ns
Tr	Rise Time		---	50	90	
$T_{d(off)}$	Turn-Off Delay Time		---	36.4	73	
Tf	Fall Time		---	7.6	15.2	
C_{iss}	Input Capacitance	VDS=15V , VGS=0V , f=1MHz	---	2423	3392	pF
C_{oss}	Output Capacitance		---	145	203	
C_{rss}	Reverse Transfer Capacitance		---	97	136	
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**
EAS	Single Pulse Avalanche Energy[5]	VDD=25V , L=0.1mH , IAS=15A	19	---	---	mJ
Symbol	**Parameter**	**Conditions**	**Min.**	**Typ.**	**Max.**	**Unit**

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I_S	Continuous Source Current[1,6]	VG=VD=0V , Force Current	---	---	40	A
I_{SM}	Pulsed Source Current[2,6]		---	---	80	A
V_{SD}	Diode Forward Voltage[2]	VGS=0V , IS=A , TJ=25°C	---	---	1	V
t_{rr}	Reverse Recovery Time	IF=15A , dI/dt=100A/μs , TJ=25°C	---	16.3	---	nS
Q_{rr}	Reverse Recovery Charge		---	11	---	nC

Note :

1 . The data tested by surface mounted on a 1 inch^2 FR-4 board with 2OZ copper.

2. The data tested by pulsed , pulse width ≦ 300us , duty cycle ≦ 2%

3 . The EAS data shows Max. rating . The test condition is VDD=25V,VGS=10V,L=0.1mH,IAS=28A

4. The power dissipation is limited by 150°C junction temperature

5. The Min. value is 100% EAS tested guarantee.

6. The data is theoretically the same as ID and IDM , in real applications , should be limited by total power dissipation.

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- **Characteristic Curves**

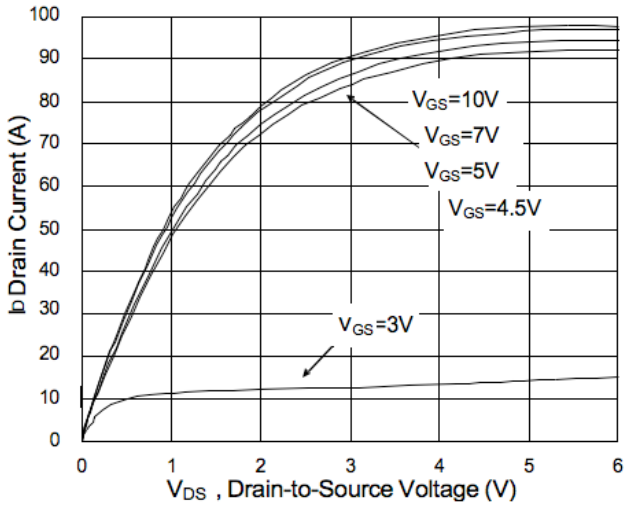

Figure 1. Typical Output Characteristics

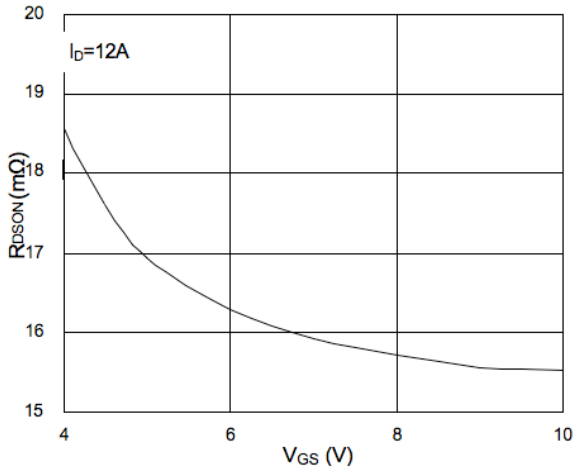

Figure 2. On-Resistance v.s Gate-Source

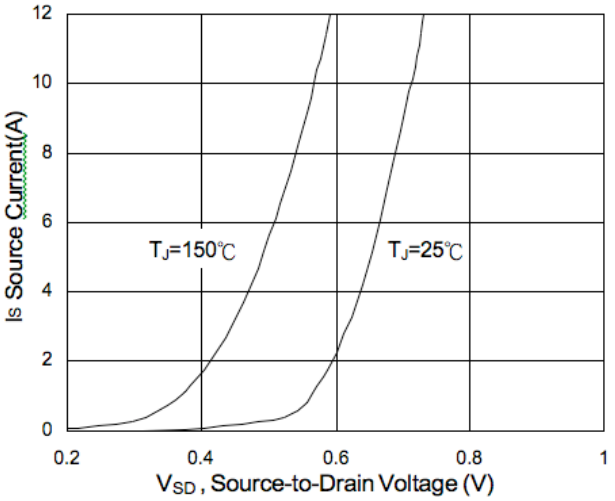

Figure 3. Forward Characteristics of Reverse

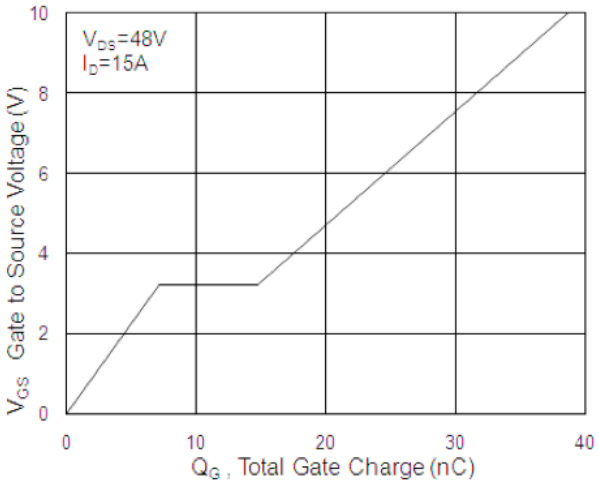

Figure 4. Gate-Charge Characteristics

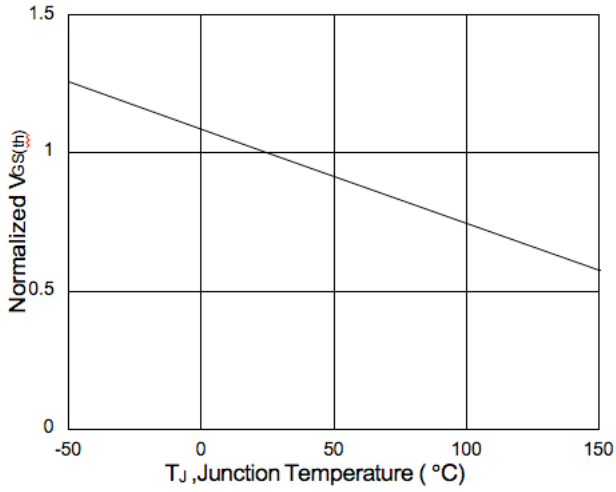

Figure 5. Normalized VGS(th) v.s TJ

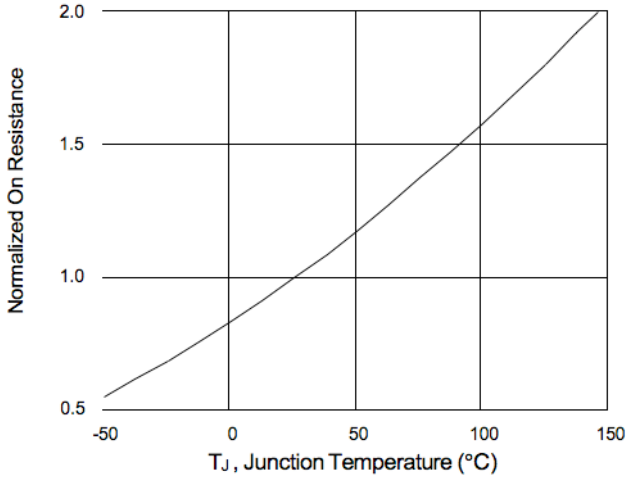

Figure 6. Normalized RDSON v.s TJ

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- **Characteristic Curves**

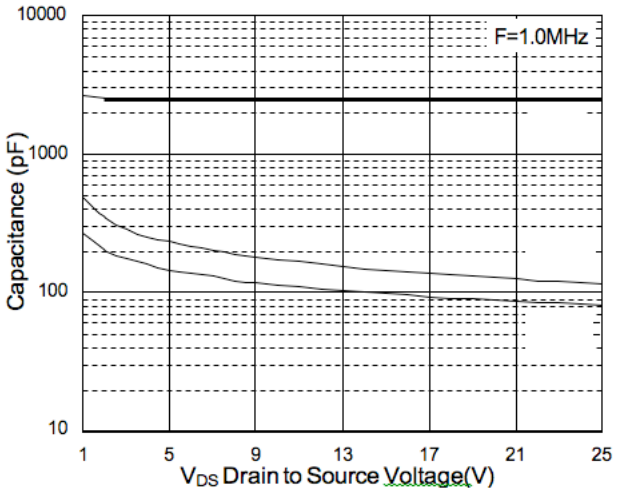


Figure 7. Capacitance

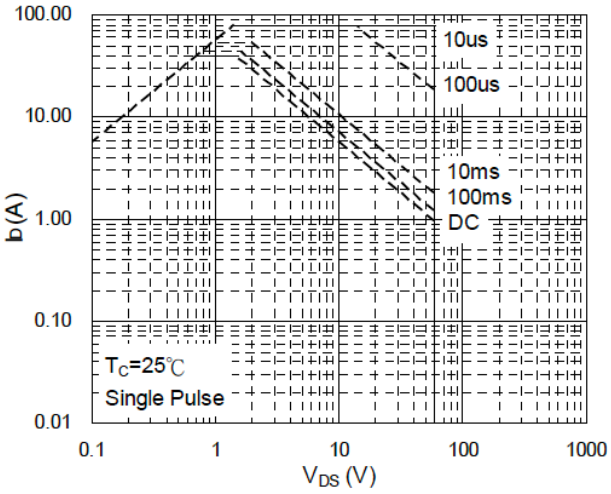


Figure 8. Safe Operating Area

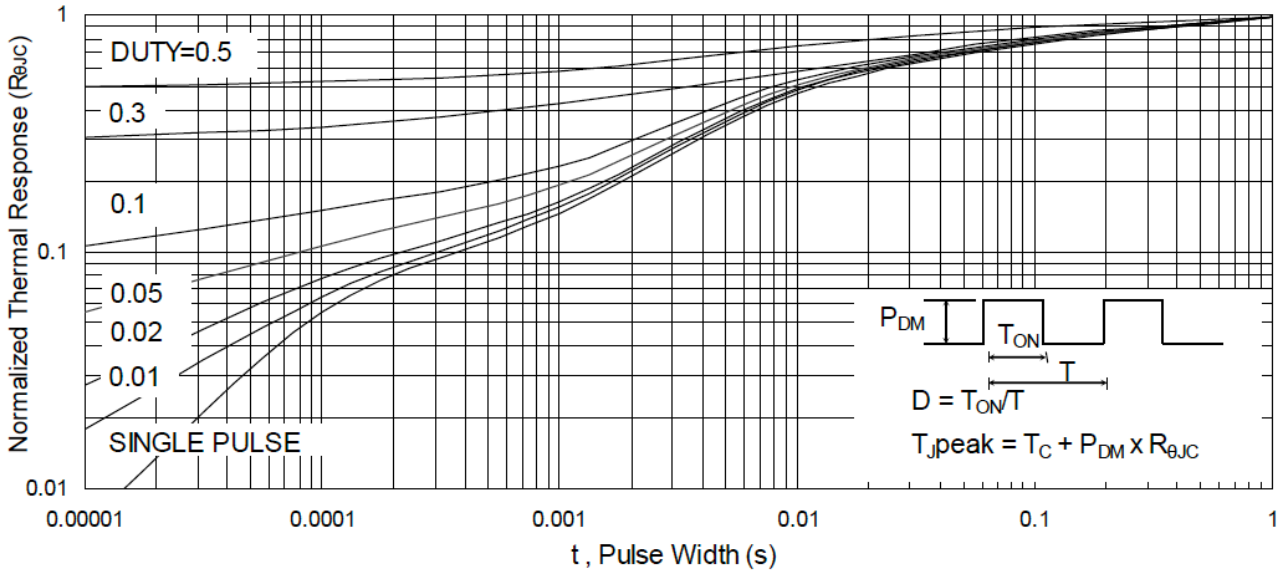


Figure 9. Normalized Maximum Transient Thermal Impedance

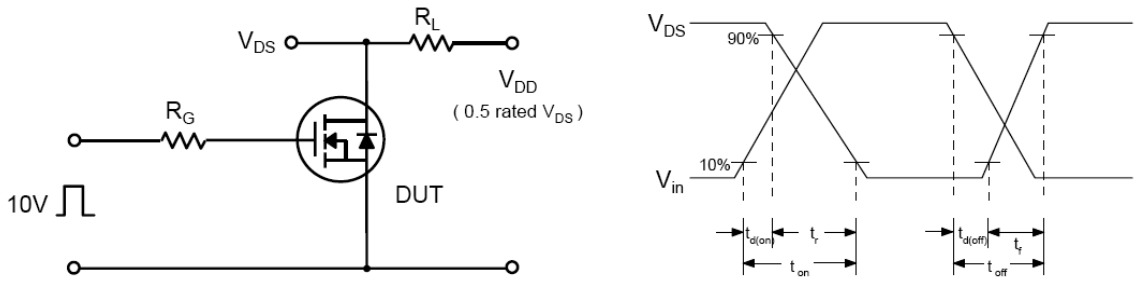


Fig 10. Resistive Switching Test Circuit & Waveforms

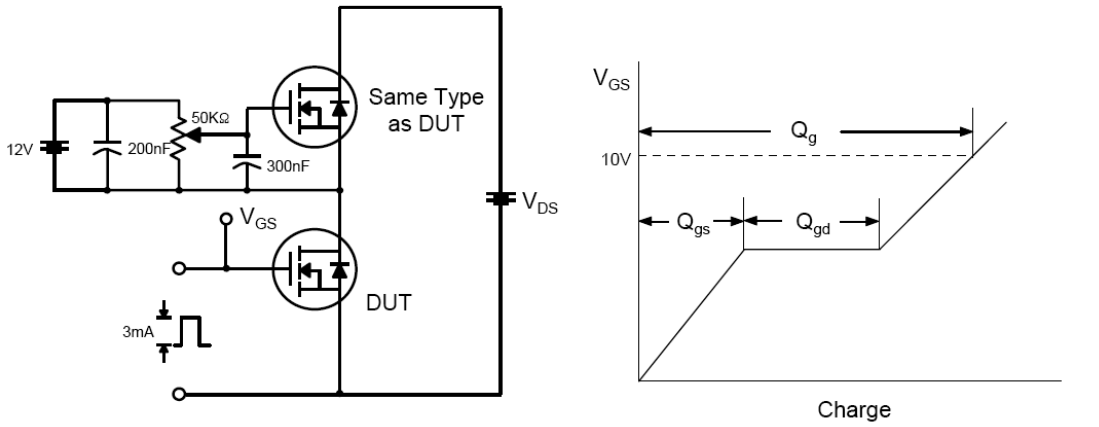


Fig 11. Gate Charge Test Circuit & Waveform

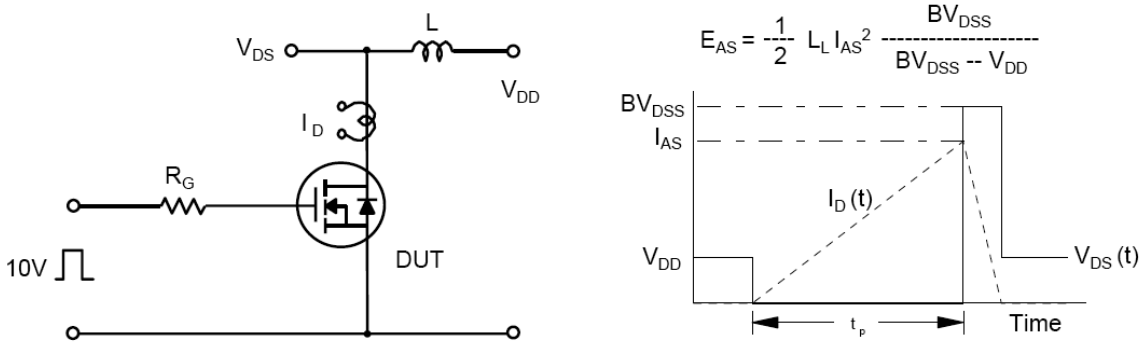
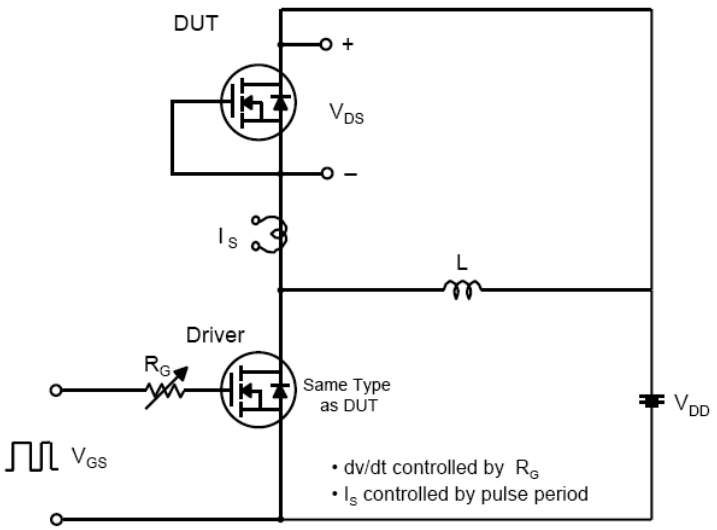


Fig 12. Unclamped Inductive Switching Test Circuit & Waveforms



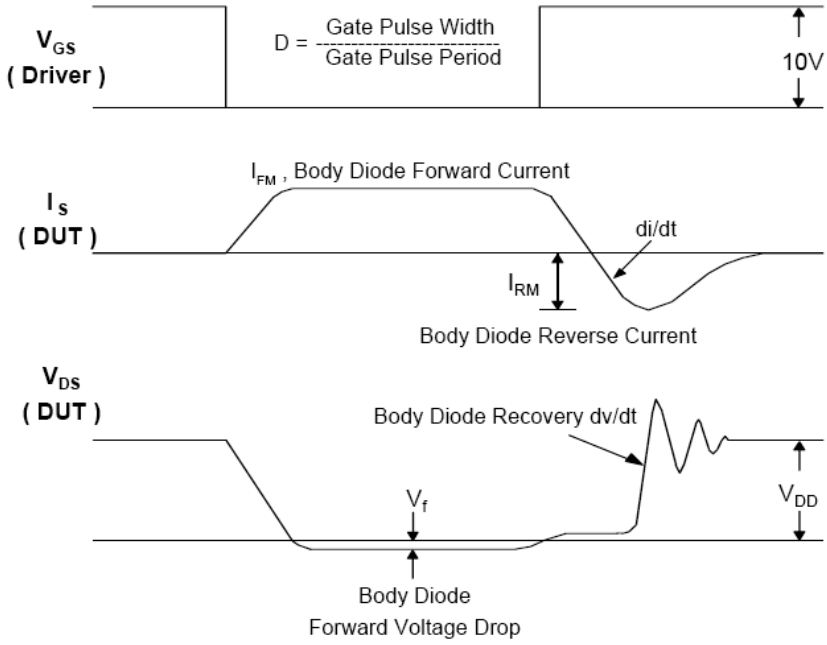


Fig 131. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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