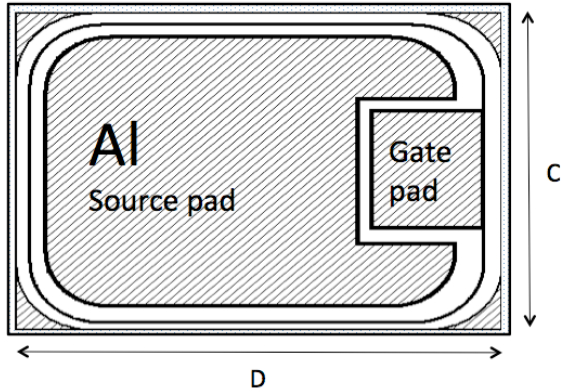
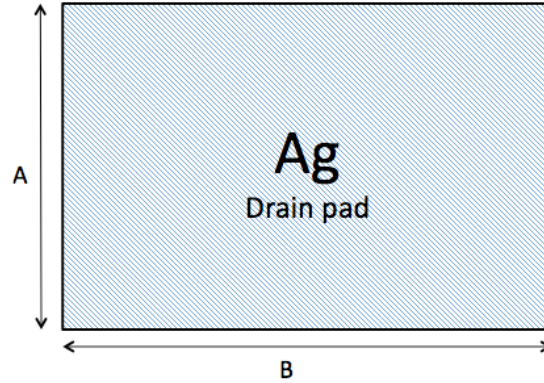


## Chip Features

### Front side



### Back side



Chip Size (um)	Thickness (um)	Pad Size-Gate (um)	Pad Size-Source (um)
4,300 * 3,320	350	430 * 550	1200 * 2400
Wafer Size 8 inch	Recommended Wire Bond	Gate Al 6mil * 1	Source Al 10mil * 1
Metalization	TOP: AL	BACK: VA/NI + Ag	

## Guaranteed PKG Electrical Ratings T<sub>C</sub> = 25°C unless otherwise noted

Symbol	Parameter	MIN	MAX	Units
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage (V <sub>GS</sub> =0V, I <sub>d</sub> =250uA)	600	-	V
V <sub>th</sub>	Gate Threshold Voltage (V <sub>DS</sub> =V <sub>GS</sub> , I <sub>d</sub> =250uA)	2.0	4.0	V
R <sub>dson</sub>	Drain-Source On-Resistance (V <sub>GS</sub> =10V, I <sub>d</sub> =3.5A)	-	1.2	Ohm
I <sub>gss</sub>	Gate-Source Leakage Current (V <sub>GS</sub> =30V, V <sub>DS</sub> =0V)	-	100	nA
I <sub>dss</sub>	Drain-Source Leakage Current (V <sub>DS</sub> =600V, V <sub>GS</sub> =0V)	-	1.0	uA
V <sub>sd</sub>	Drain-Source Forward Voltage Drop (V <sub>GS</sub> =0V, I <sub>s</sub> =7.0A)	-	1.5	V

## NOTES

1. Detailed device characteristics are available in the device data sheet
2. Drain current limited by maximum junction temperature.