

GSM5008S

40V N-Channel Enhancement Mode MOSFET

Product Description

GSM5008S, N-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

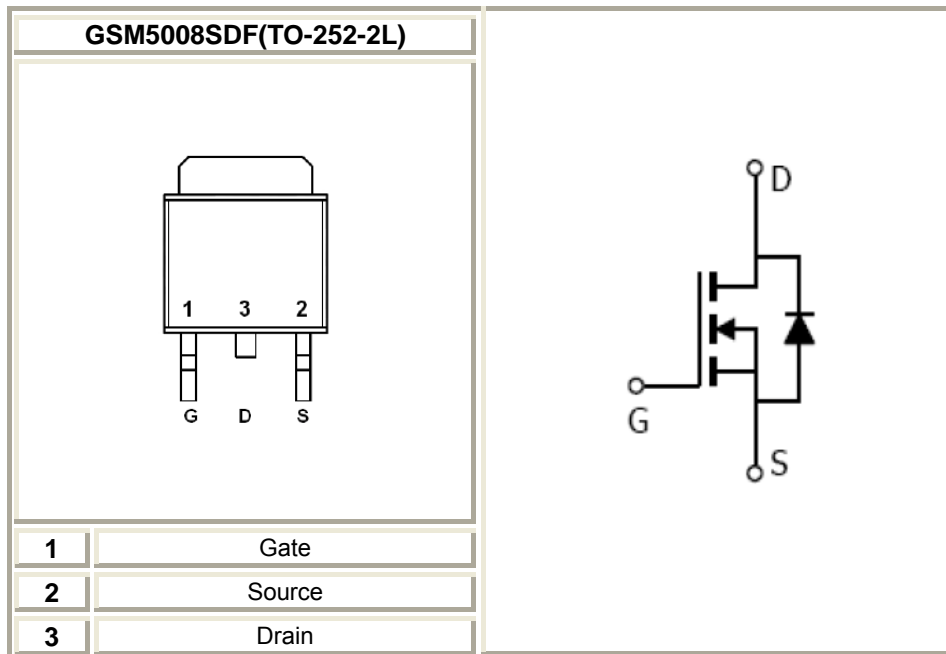
Features

- 40V/20A, $R_{DS(ON)} = 8.5m\Omega @ V_{GS} = 10V$
- 40V/15A, $R_{DS(ON)} = 10.5m\Omega @ V_{GS} = 4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- TO-252-2L package design

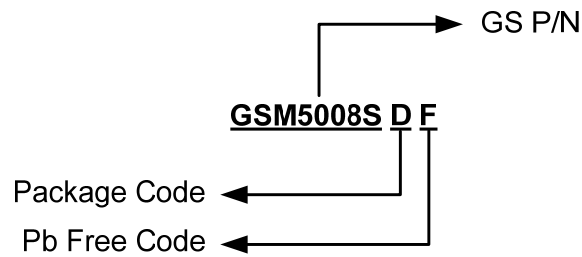
Applications

- Backlight Inverter for LCD Display
- DC/DC Converters

Packages & Pin Assignments

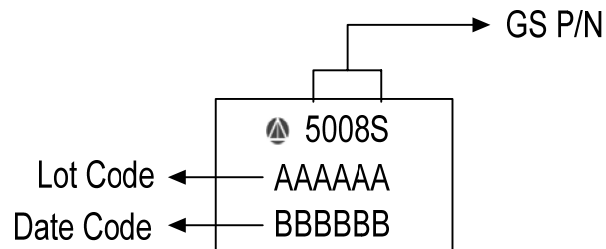


Ordering Information



Part Number	Package	Quantity Reel
GSM5008SDF	TO-252-2L	2500 PCS

Marking Information



Absolute Maximum Ratings

($T_A=25^\circ\text{C}$ unless otherwise noted)

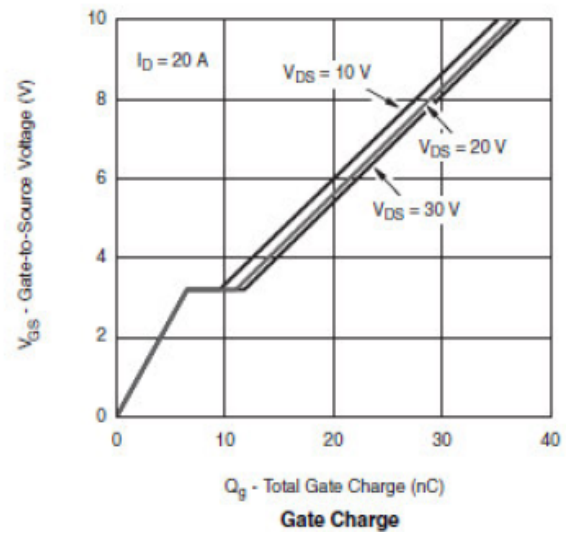
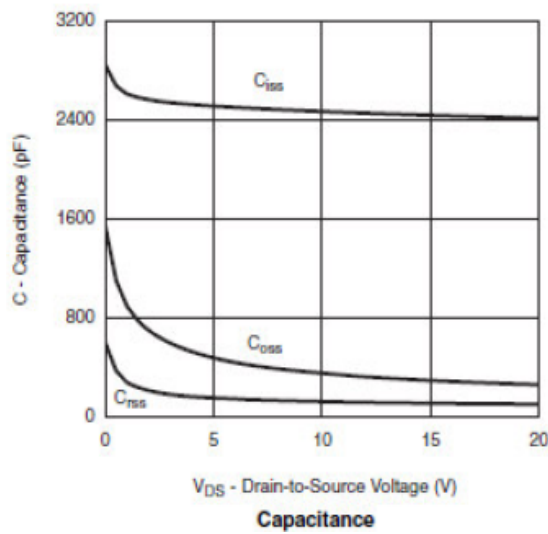
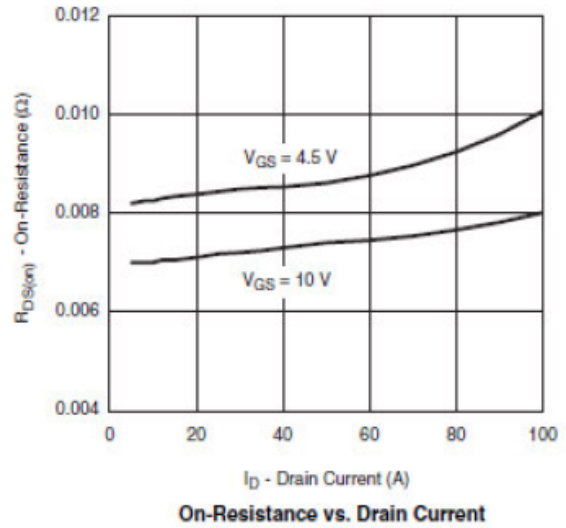
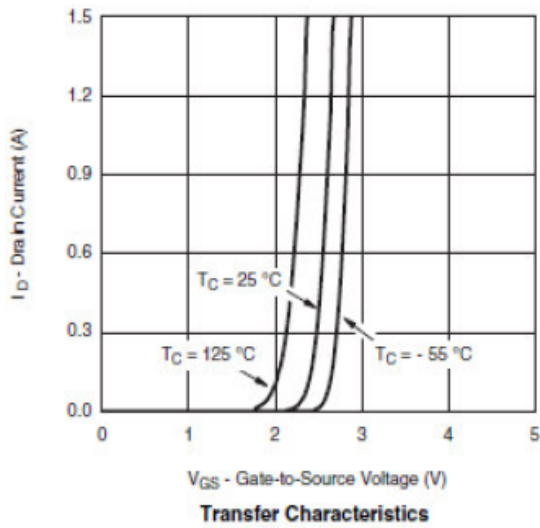
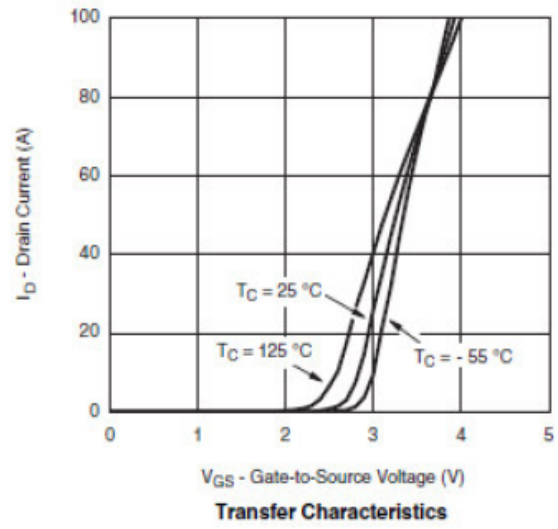
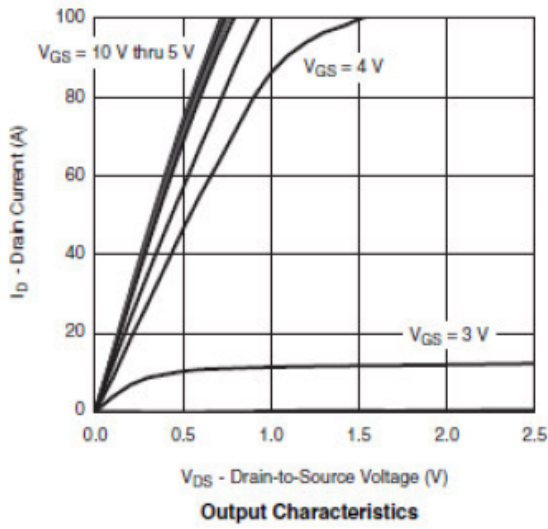
Symbol	Parameter	Typical	Unit	
V_{DSS}	Drain-Source Voltage	40	V	
V_{GSS}	Gate –Source Voltage	± 20	V	
I_D	Continuous Drain Current($T_J=150^\circ\text{C}$)	$T_A=25^\circ\text{C}$	50	A
		$T_A=70^\circ\text{C}$	44	
I_{DM}	Pulsed Drain Current	100	A	
I_S	Continuous Source Current(Diode Conduction)	40	A	
I_{AS}	Single Pulse Avalanche Current	L=0.1mH	30	A
E_{AS}	Avalanche Energy		45	mJ
P_D	Power Dissipation	$T_A=25^\circ\text{C}$	40	W
		$T_A=70^\circ\text{C}$	15	
T_J	Operating Junction Temperature	150	$^\circ\text{C}$	
T_{STG}	Storage Temperature Range	-55/150	$^\circ\text{C}$	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5	$^\circ\text{C}/\text{W}$	

Electrical Characteristics

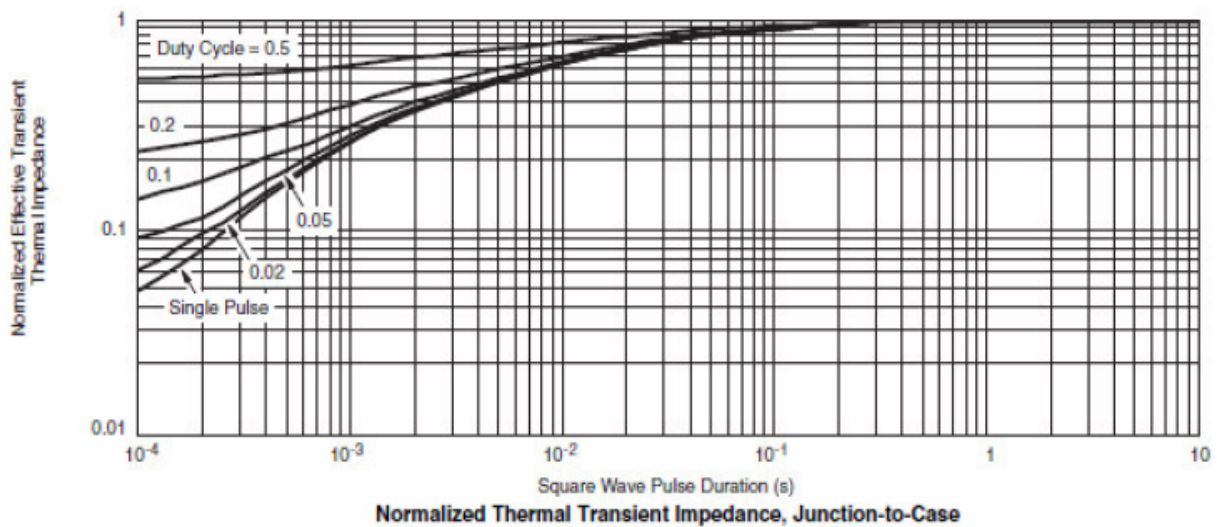
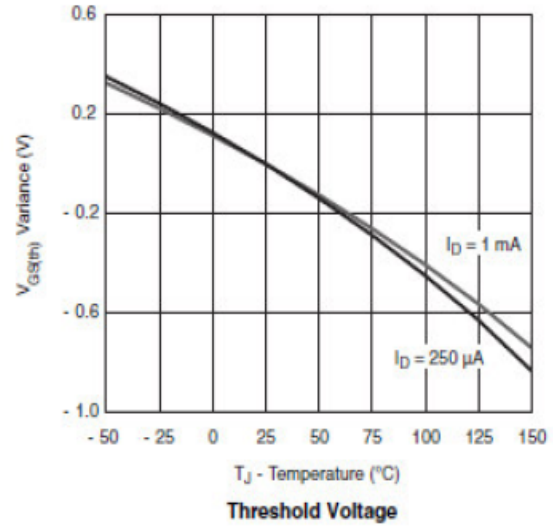
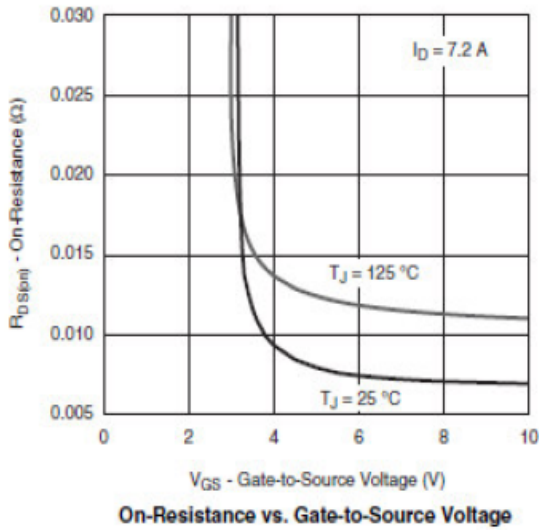
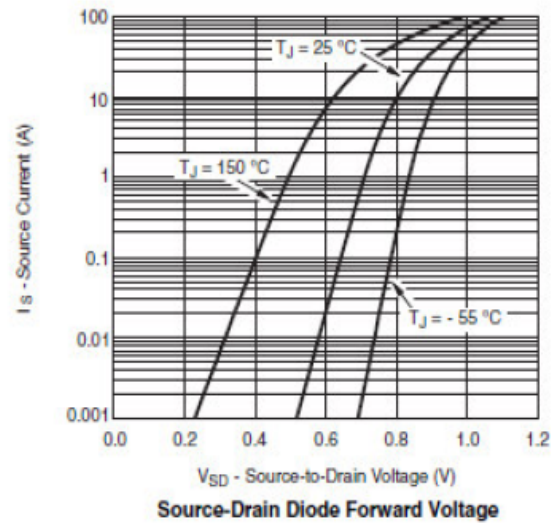
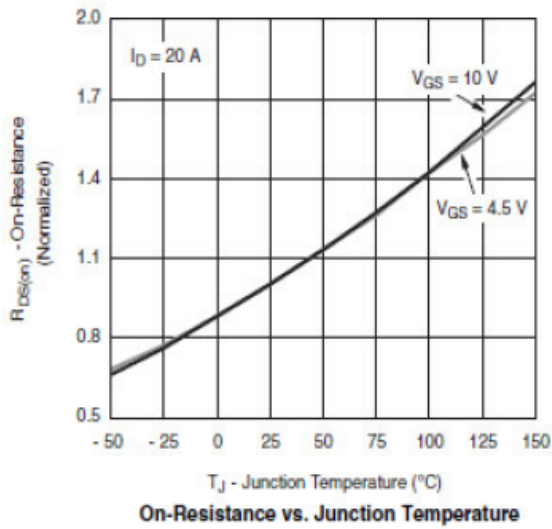
($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ	Max.	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	40			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.0	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=32V, V_{GS}=0V$			1	uA
		$V_{DS}=32V, V_{GS}=0V, T_J=85^\circ\text{C}$			10	
$I_{D(on)}$	On-State Drain Current	$V_{DS}\geq 5V, V_{GS}=10V$	50			A
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=20A$		6.8	8.5	m Ω
		$V_{GS}=4.5V, I_D=15A$		8.4	10.5	
g_{FS}	Forward Transconductance	$V_{DS}=15V, I_D=15A$		75		S
V_{SD}	Diode Forward Voltage	$I_S=10A, V_{GS}=0V$		0.85	1.3	V
Dynamic						
C_{iss}	Input Capacitance	$V_{DS}=20V, V_{GS}=0V, f=1\text{MHz}$		2400		pF
C_{oss}	Output Capacitance			260		
C_{riss}	Reverse Transfer Capacitance			100		
Q_g	Total Gate Charge	$V_{DS}=20V, V_{GS}=4.5V, I_D=20A$		16	24	nC
Q_{gs}	Gate-Source Charge			6.5		
Q_{gd}	Gate-Drain Charge			4.5		
$t_{d(on)}$	Turn-On Time	$V_{DD}=20V, R_L=1\Omega, I_D=20A, V_{GEN}=10V, R_G=1\Omega$		8	15	ns
T_r				5	10	
$t_{d(off)}$				40	60	
T_f				5	10	

Typical Performance Characteristics

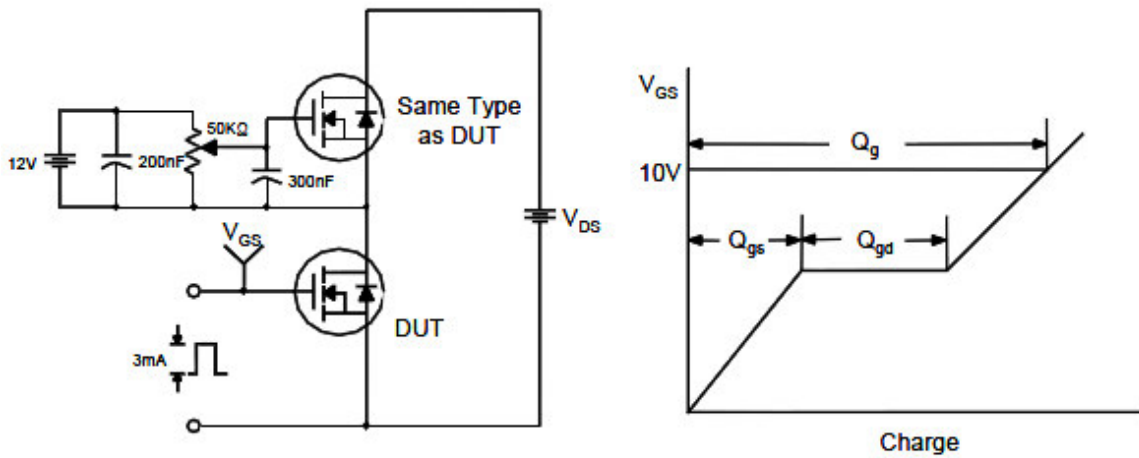


Typical Performance Characteristics (continue)

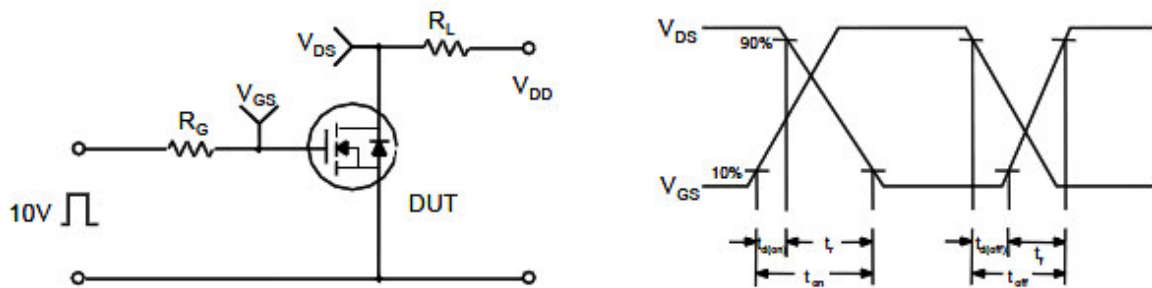


Typical Characteristics

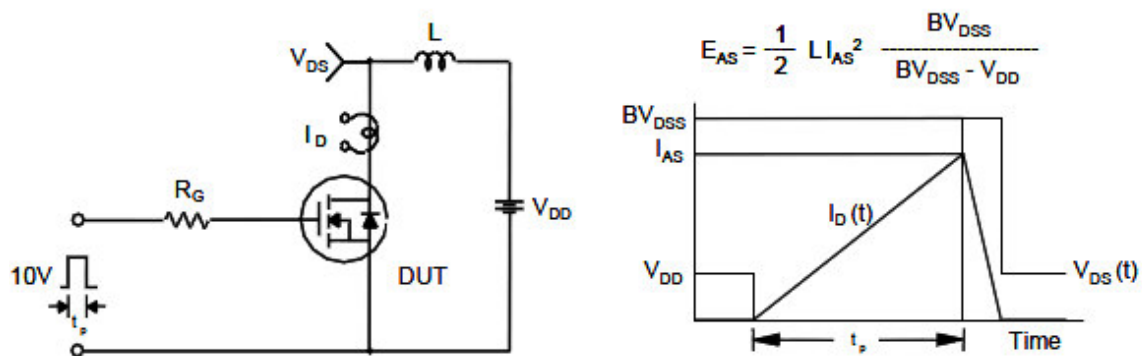
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

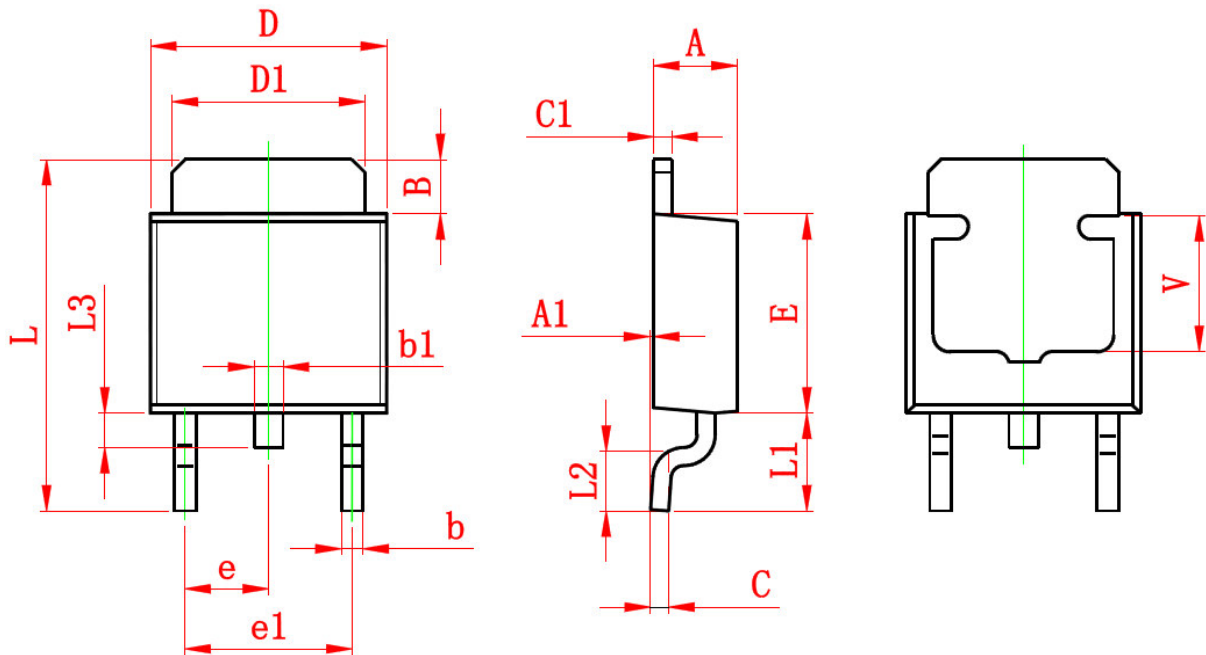


Unclamped Inductive Switching Test Circuit & Waveforms



Package Dimension

TO-252-2L PLASTIC PACKAGE







Dimensions





SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
B	1.350	1.650	0.053	0.065
b	0.500	0.700	0.020	0.028
b1	0.700	0.900	0.028	0.035
c	0.430	0.580	0.017	0.023
c1	0.430	0.580	0.017	0.023
D	6.350	6.650	0.250	0.262
D1	5.200	5.400	0.205	0.213
E	5.400	5.700	0.213	0.224
e	2.300 TYP.		0.091 TYP.	
e1	4.500	4.700	0.177	0.185
L	9.500	9.900	0.374	0.390
L1	2.550	2.900	0.100	0.114
L2	1.400	1.780	0.055	0.070
L3	0.600	0.900	0.024	0.035
V	3.800 REF.		0.150 REF.	



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