

GSM4948

60V P-Channel Enhancement Mode MOSFET

Product Description

GSM4948, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

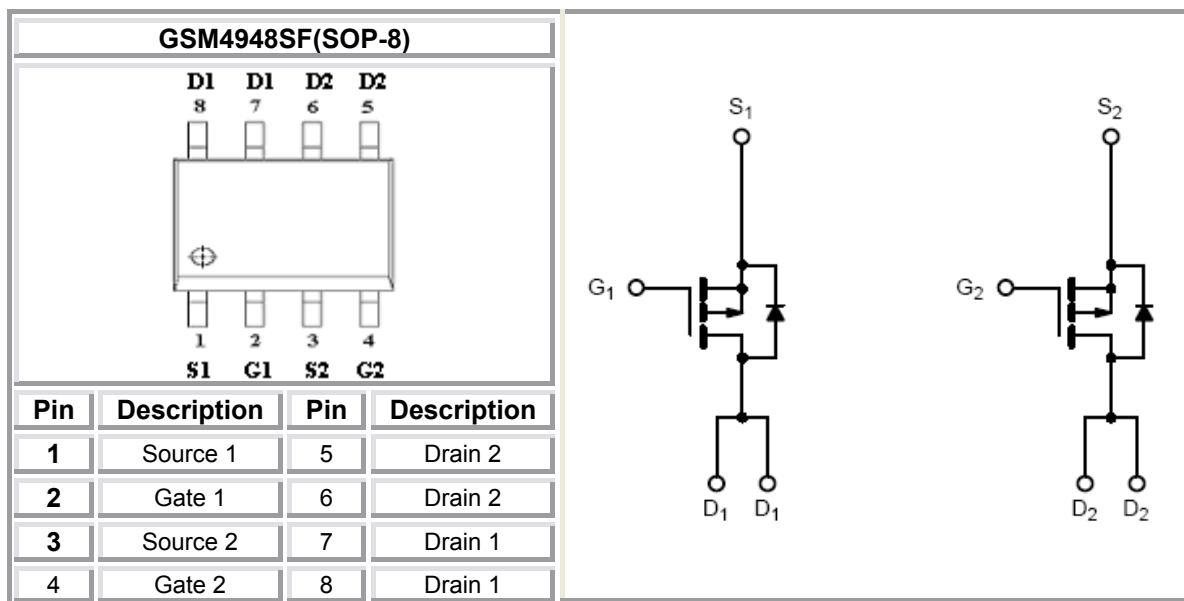
Features

- -60V/-4.0A, $R_{DS(ON)} = 100m\Omega @ V_{GS} = -10V$
- -60V/-3.0A, $R_{DS(ON)} = 120m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOP-8P package design

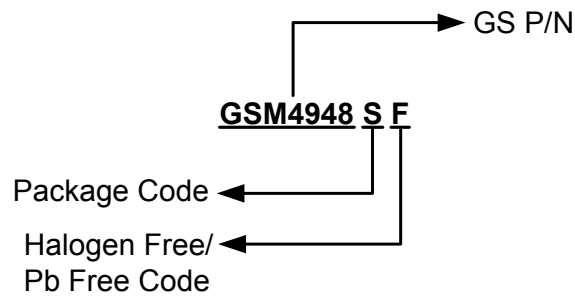
Applications

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter
- Load Switch
- CCFL Inverter

Packages & Pin Assignments

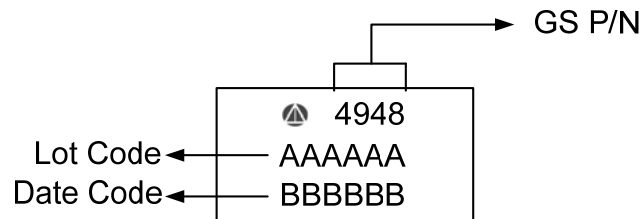


Ordering Information



Part Number	Package	Quantity Reel
GSM4948SF	SOP-8	3000 PCS

Marking Information



Absolute Maximum Ratings

(T_A=25°C unless otherwise noted)

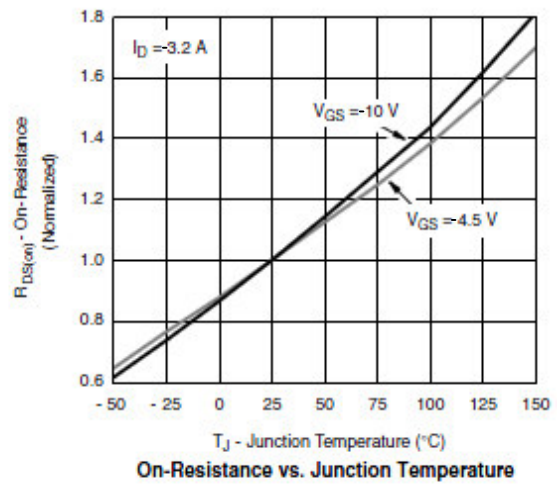
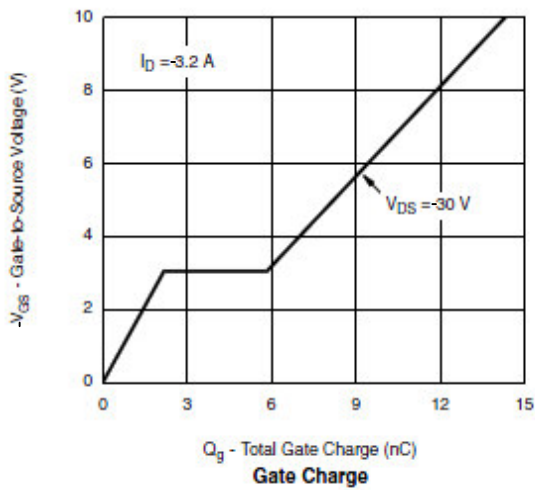
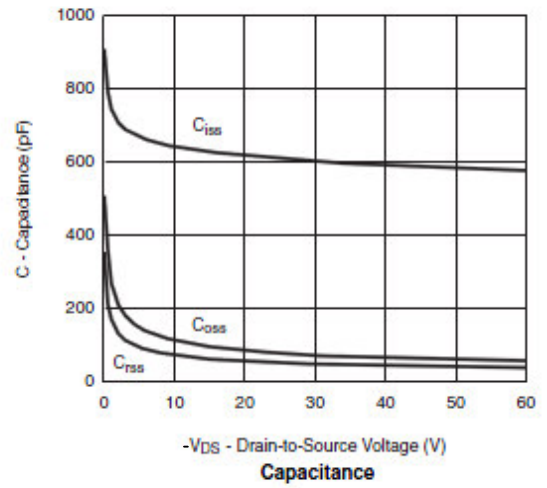
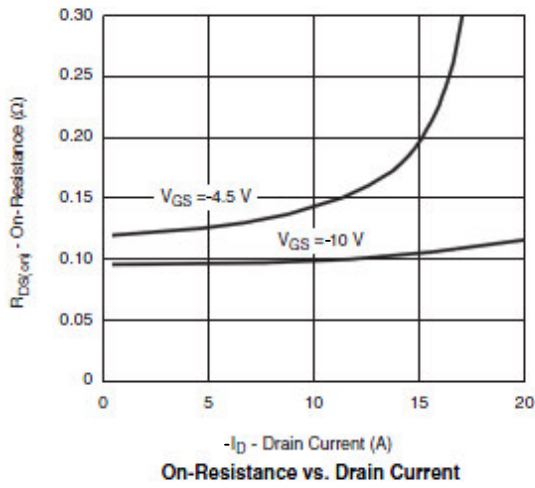
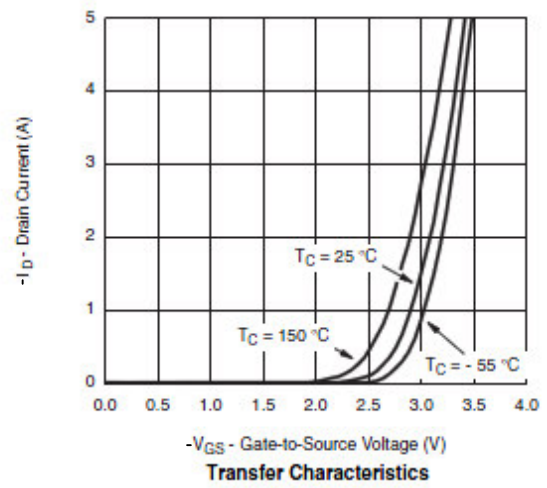
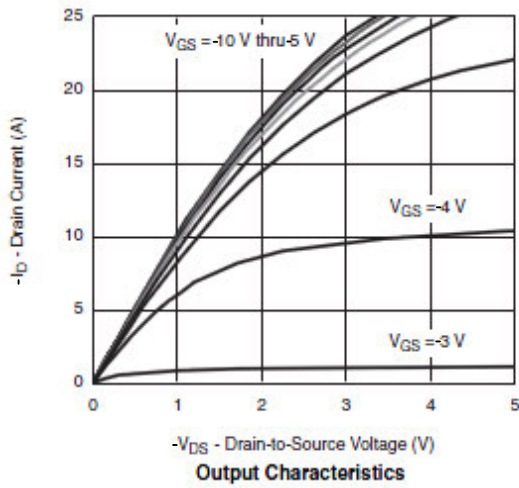
Symbol	Parameter	Typical	Unit
V _{DSS}	Drain-Source Voltage	-60	V
V _{GSS}	Gate -Source Voltage	±20	V
I _D	Continuous Drain Current(T _J =150°C)	T _A =25°C	-4.0
		T _A =70°C	-3.0
I _{DM}	Pulsed Drain Current	-20	A
I _S	Continuous Source Current(Diode Conduction)	-1.7	A
P _D	Power Dissipation	T _A =25°C	2.8
		T _A =70°C	1.8
T _J	Operating Junction Temperature	150	°C
T _{STG}	Storage Temperature Range	-55/150	°C
R _{θJA}	Thermal Resistance-Junction to Ambient	62.5	°C/ W

Electrical Characteristics

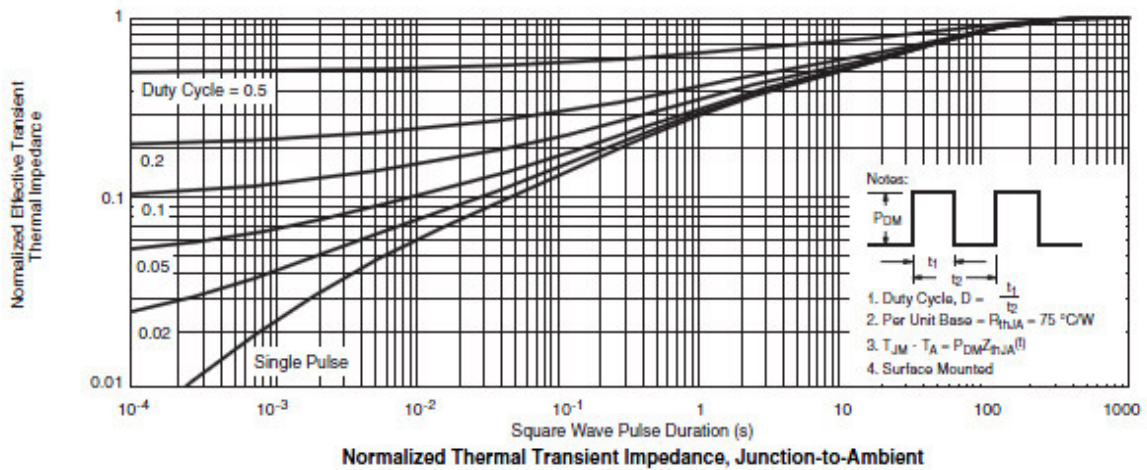
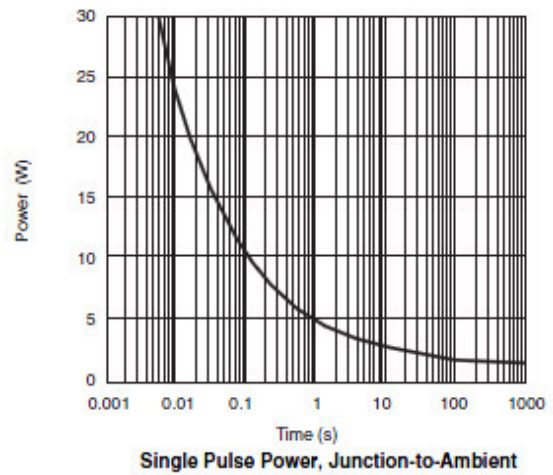
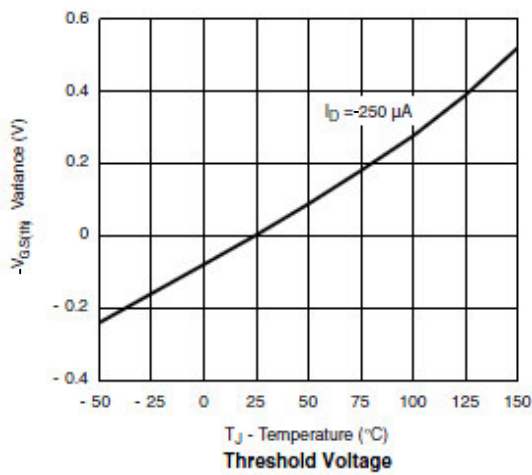
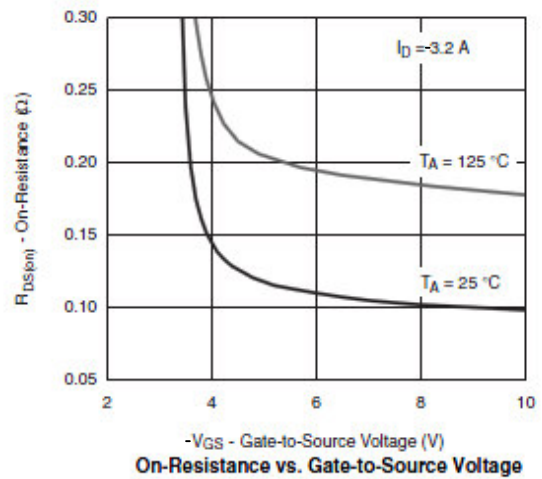
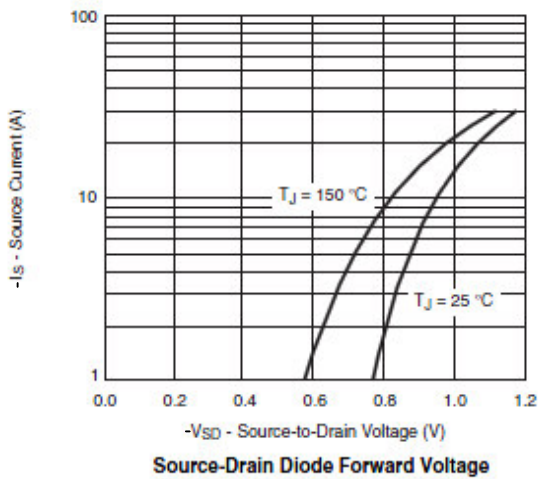
($T_A=25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=-250\mu A$	-0.8		-2.5	
I_{GSS}	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			± 100	nA
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS}=-48V, V_{GS}=0V$			-1	uA
		$V_{DS}=-48V, V_{GS}=0V, T_J=85^\circ\text{C}$			-20	
$I_{D(on)}$	On-State Drain Current	$V_{DS}\leq -5V, V_{GS}=-10V$	-20			A
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-4.0A$		88	100	m Ω
		$V_{GS}=-4.5V, I_D=-3.0A$		98	120	
g_{fs}	Forward Transconductance	$V_{DS}=-15V, I_D=-3.2A$		12		S
V_{SD}	Diode Forward Voltage	$I_S=-2A, V_{GS}=0V$		-0.8	-1.2	V
Dynamic						
C_{iss}	Input Capacitance	$V_{DS}=-30V, V_{GS}=0V, f=1\text{MHz}$		900		pF
C_{oss}	Output Capacitance			90		
C_{rss}	Reverse Transfer Capacitance			40		
Q_g	Total Gate Charge	$V_{DS}=-30V, V_{GS}=-10V, I_D=-4.0A$		12	20	nC
Q_{gs}	Gate-Source Charge			2.5		
Q_{gd}	Gate-Drain Charge			3.5		
$t_{d(on)}$	Turn-On Time	$V_{DD}=-30V, R_L=7.5\Omega, I_D=-3.0A, V_{GEN}=-10V, R_G=3\Omega$		10	20	ns
T_r				6	10	
$t_{d(off)}$	Turn-Off Time			30	45	
T_f				12	25	

Typical Performance Characteristics

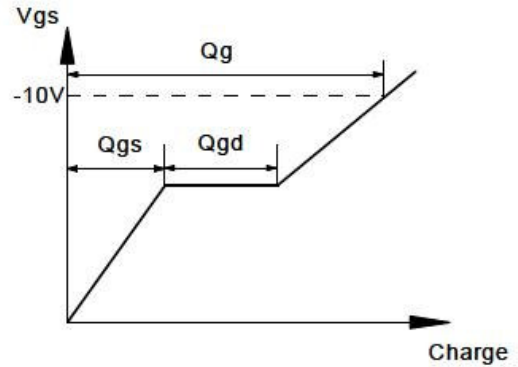
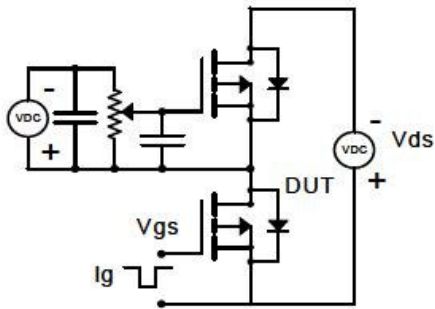


Typical Performance Characteristics (continue)

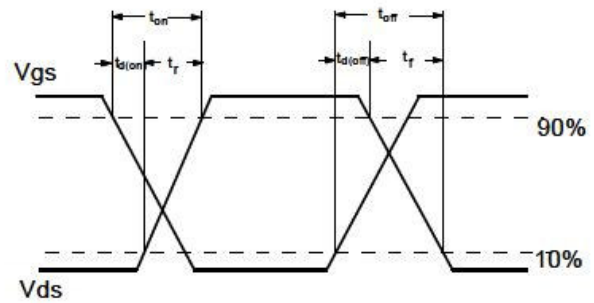
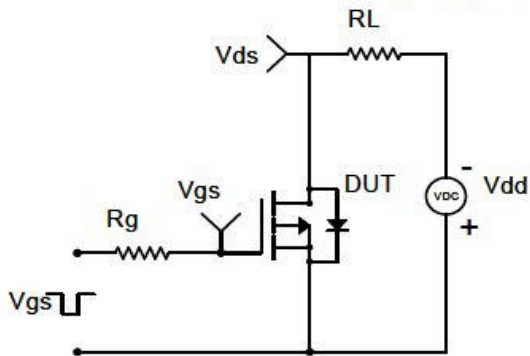


Typical Performance Characteristics (continue)

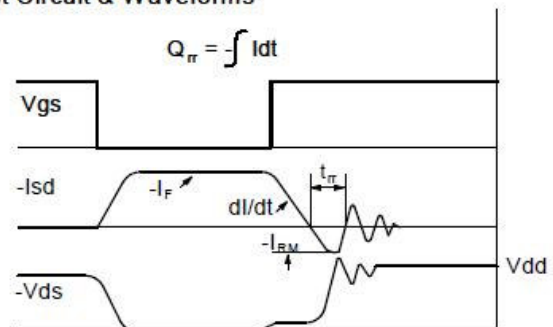
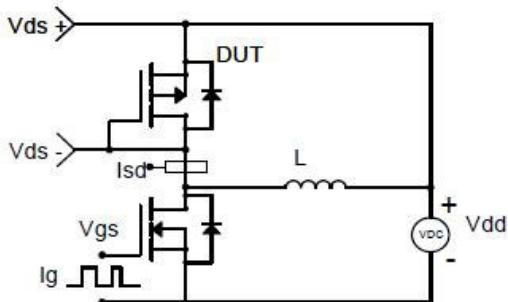
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

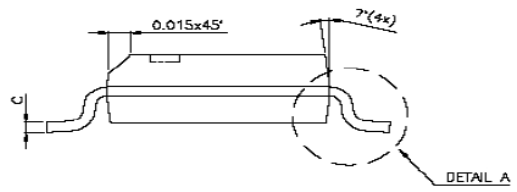
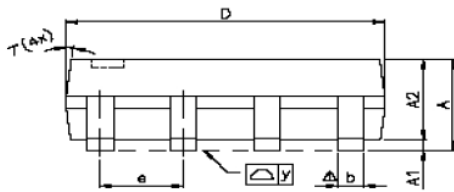
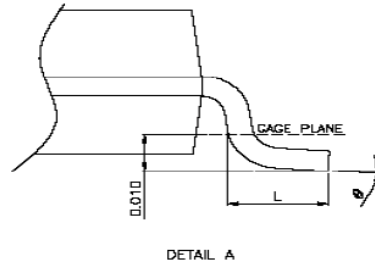
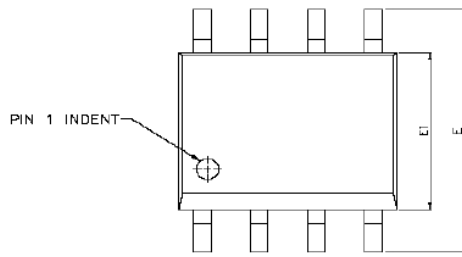


Diode Recovery Test Circuit & Waveforms



Package Dimension

SOP-8P PLASTIC PACKAGE











Dimensions						
SYMBOL	Millimeters			Inches		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
L	0.38	0.71	1.27	0.015	0.028	0.050
Δy	-	-	0.076	-	-	0.003
θ	0°	-	8°	0°	-	8°



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