

GSM4953WS

30V P-Channel Enhancement Mode MOSFET

Product Description

GSM4953WS, P-Channel enhancement mode MOSFET, uses Advanced Trench Technology to provide excellent $R_{DS(ON)}$, low gate charge.

These devices are particularly suited for low voltage power management, and low in-line power loss are needed in commercial industrial surface mount applications.

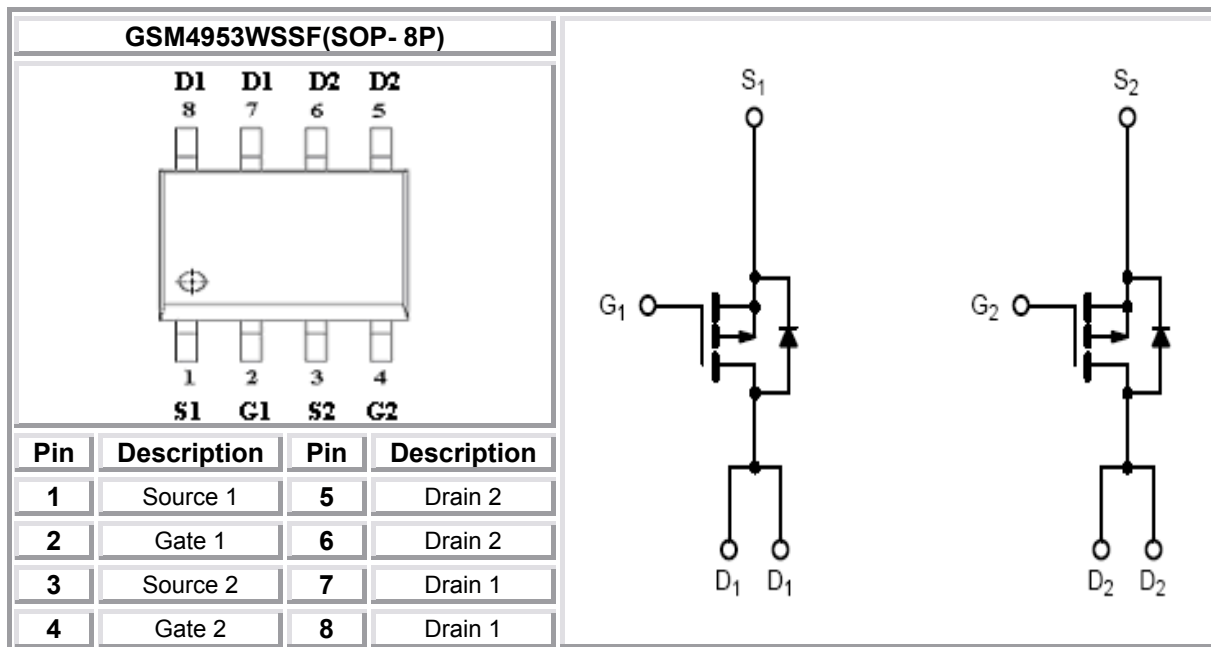
Features

- -30V/-5.4A, $R_{DS(ON)}=60m\Omega@V_{GS}=-10V$
- -30V/-4.2A, $R_{DS(ON)}=80m\Omega@V_{GS}=-4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$
- SOP-8P package design

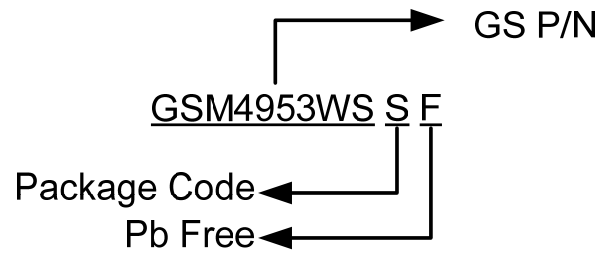
Applications

- LED Display
- Load Switch
- CCFL Inverter
- Power Management in Notebook Computer

Packages & Pin Assignments

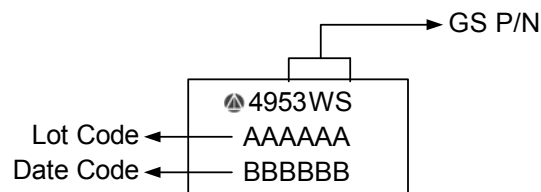


Ordering Information



Part Number	Package	Quantity Reel
GSM4953WSSF	SOP- 8P	2500 PCS

Marking Information



Absolute Maximum Ratings

$T_A=25^{\circ}\text{C}$ Unless otherwise noted

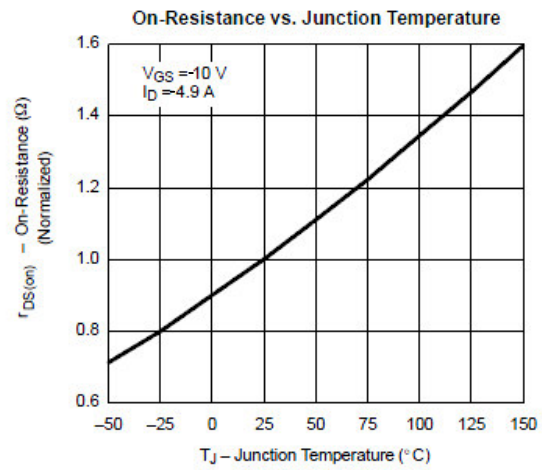
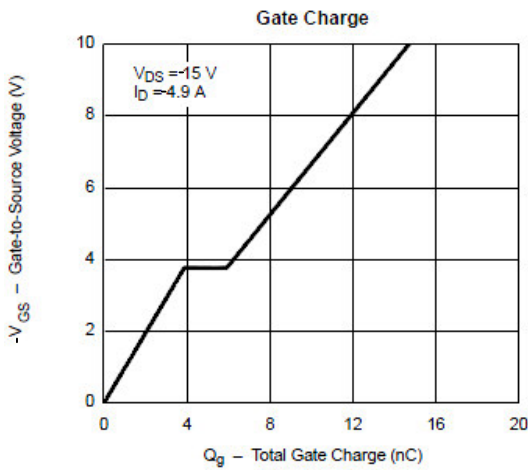
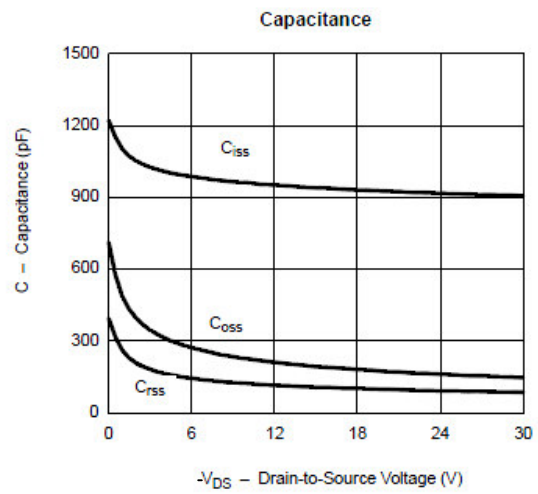
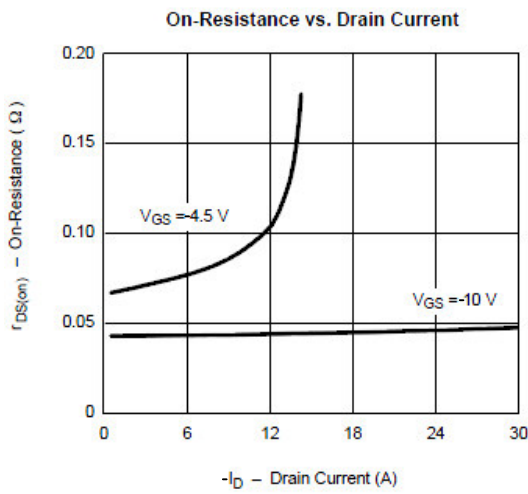
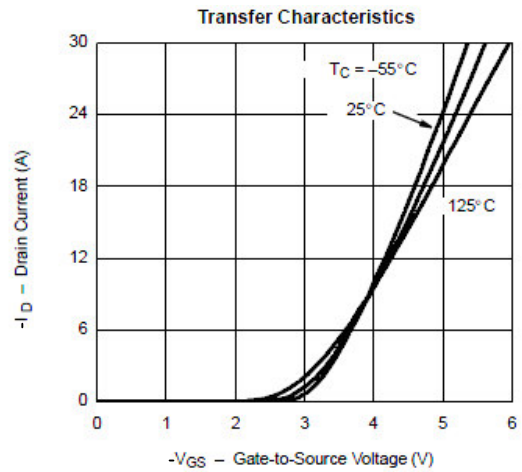
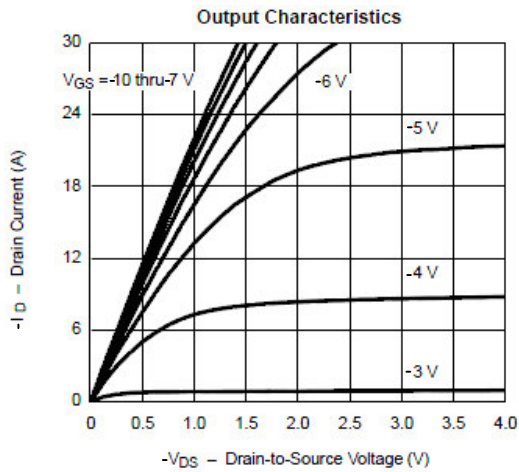
Symbol	Parameter	Typical	Unit	
V_{DSS}	Drain-Source Voltage	-30	V	
V_{GSS}	Gate -Source Voltage	± 20	V	
I_D	Continuous Drain Current($T_J=150^{\circ}\text{C}$)	$T_A=25^{\circ}\text{C}$	-5.4	A
		$T_A=70^{\circ}\text{C}$	-4.2	
I_{DM}	Pulsed Drain Current	-30	A	
I_S	Continuous Source Current(Diode Conduction)	-1.7	A	
P_D	Power Dissipation	$T_A=25^{\circ}\text{C}$	2.8	W
		$T_A=70^{\circ}\text{C}$	1.8	
T_J	Operating Junction Temperature	150	$^{\circ}\text{C}$	
T_{STG}	Storage Temperature Range	-55/150	$^{\circ}\text{C}$	
$R_{\theta JA}$	Thermal Resistance-Junction to Ambient	62.5	$^{\circ}\text{C}/\text{W}$	

Electrical Characteristics

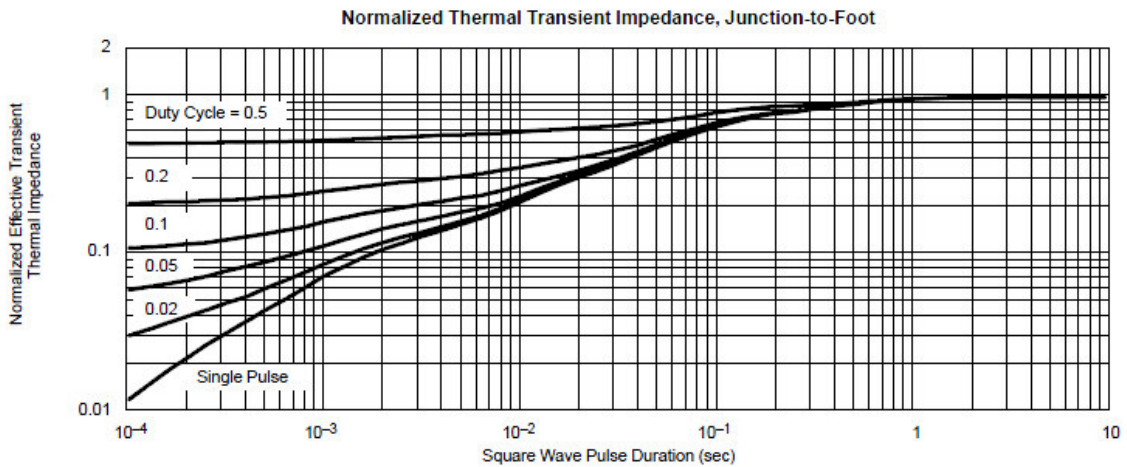
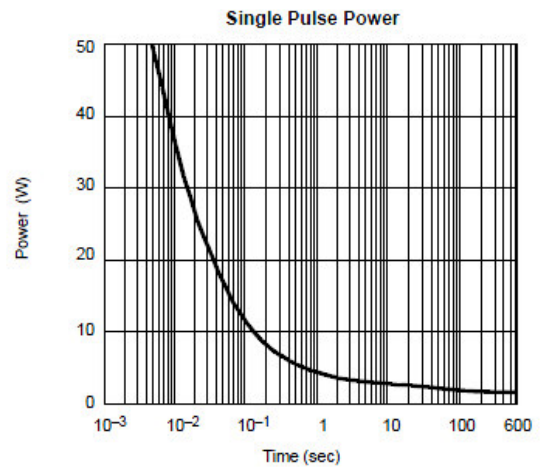
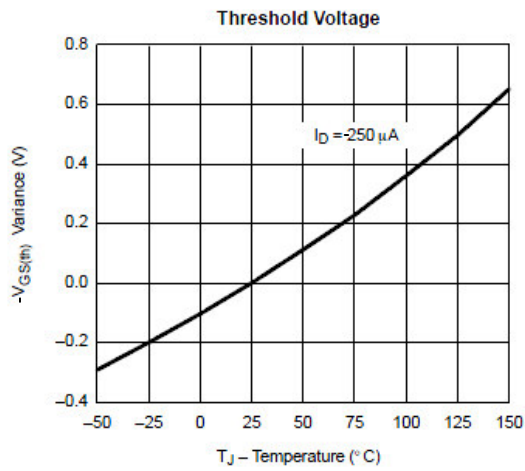
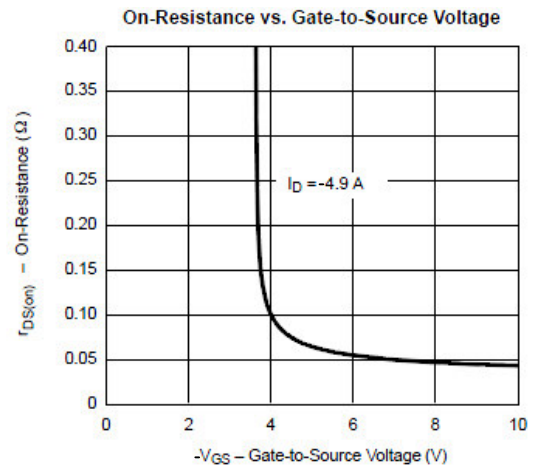
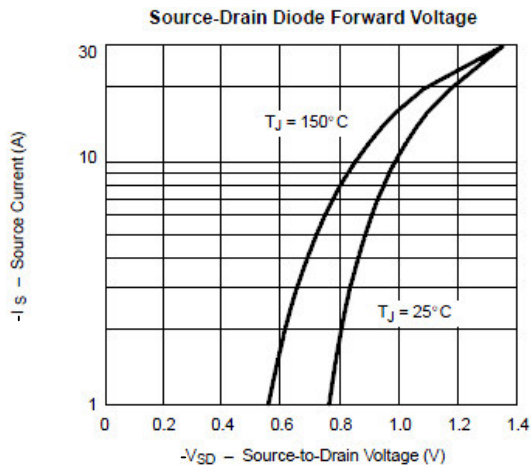
T_A=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D = -250uA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D = -250uA	-1.0		-2.5	
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = -24V, V _{GS} =0V			-1	uA
		V _{DS} = -24V, V _{GS} =0V, T _J =85°C			-30	
I _{D(on)}	On-State Drain Current	V _{DS} ≤ -5V, V _{GS} =-10V	-25			A
R _{DS(on)}	Drain-Source On-Resistance	V _{GS} = -10V, I _D = -5.4A		50	60	mΩ
		V _{GS} = -4.5V, I _D = -4.2A		70	80	
g _{FS}	Forward Transconductance	V _{DS} = -10V, I _D = -4.9A		10		S
V _{SD}	Diode Forward Voltage	I _S = -1.7A, V _{GS} =0V		-0.8	-1.3	V
Dynamic						
Q _g	Total Gate Charge	V _{DS} = -15V, V _{GS} = -10V, I _D = -5.0A		10	18	nC
Q _{gs}	Gate-Source Charge			1.6		
Q _{gd}	Gate-Drain Charge			3.0		
C _{iss}	Input Capacitance	V _{DS} = -15V, V _{GS} =0V, f=1MHz		500		pF
C _{oss}	Output Capacitance			100		
C _{rss}	Reverse Transfer Capacitance			55		
t _{d(on)}	Turn-On Time	V _{DD} =-15V, R _L =15Ω, I _D =-1.0A, V _{GEN} = -10V, R _G =6Ω		8	18	ns
t _r				8	18	
t _{d(off)}	Turn-Off Time			25	50	
t _f				25	35	

Typical Performance Characteristics

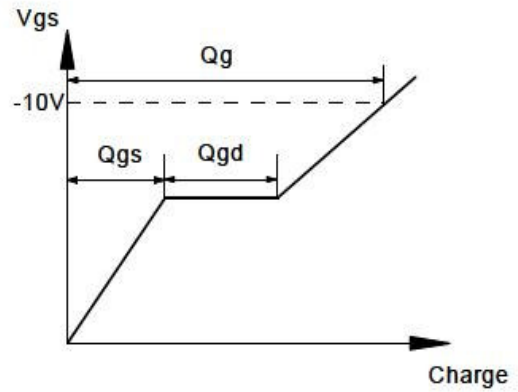
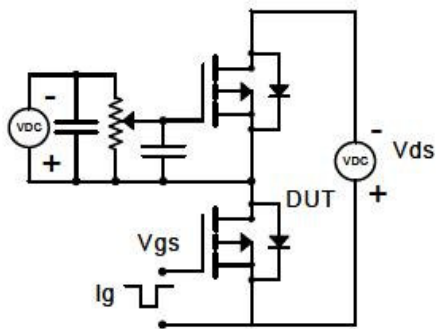


Typical Performance Characteristics (Continue)

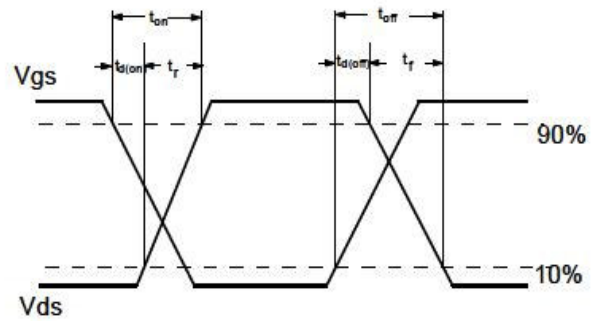
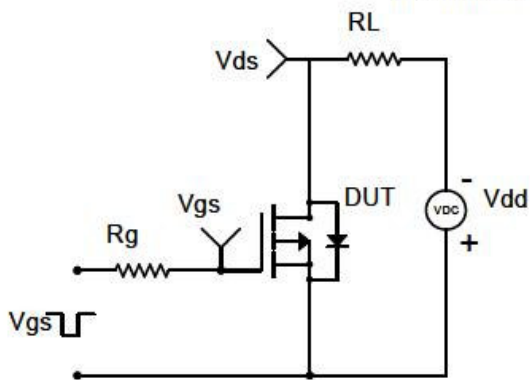


Typical Performance Characteristics (Continue)

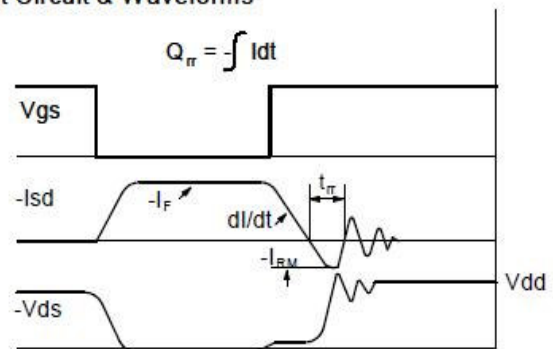
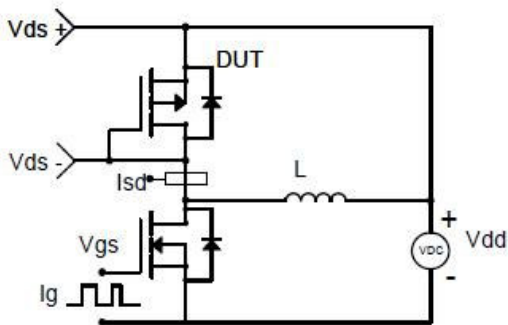
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms

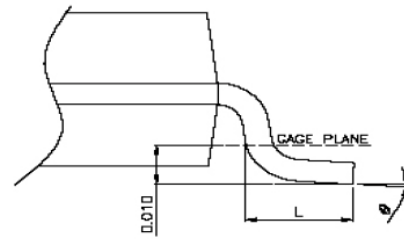
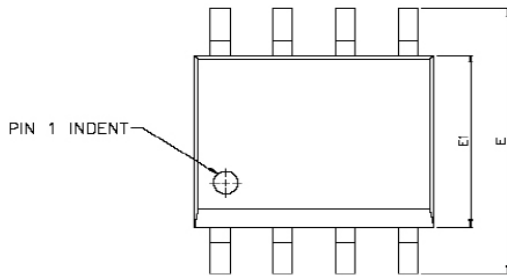


Diode Recovery Test Circuit & Waveforms

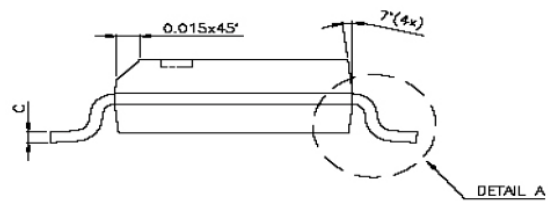
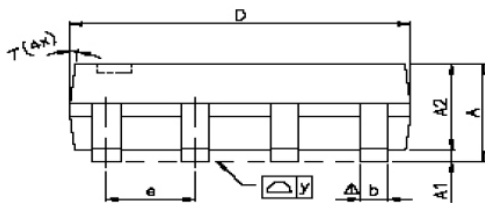


Package Dimension

SOP-8P



DETAIL A



DETAIL A





Dimensions

Symbol	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	1.47	1.60	1.73	0.058	0.063	0.068
A1	0.10	-	0.25	0.004	-	0.010
A2	-	1.45	-	-	0.057	-
b	0.33	0.41	0.51	0.013	0.016	0.020
C	0.19	0.20	0.25	0.0075	0.008	0.0098
D	4.80	4.85	4.95	0.189	0.191	0.195
E	5.80	6.00	6.20	0.228	0.236	0.244
E1	3.80	3.90	4.00	0.150	0.154	0.157
e	-	1.27	-	-	0.050	-
L	0.38	0.71	1.27	0.015	0.028	0.050
Δy	-	-	0.076	-	-	0.003
θ	0°	-	8°	0°	-	8°



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