

# GSM7002

## 60V N-Channel Enhancement Mode MOSFET

### Product Description

The GS7002 is the N-Channel enhancement mode field effect transistors are produced using high cell density DMOS technology. These products have been designed to minimize on-state resistance while provide rugged, reliable, and fast switching performance.

They can be used in most applications requiring up to 300mA DC and can deliver pulsed currents up to 1.0A.

These products are particularly suited for low voltage, low current applications such as small servo motor control, power MOSFET gate drivers, and other switching applications.

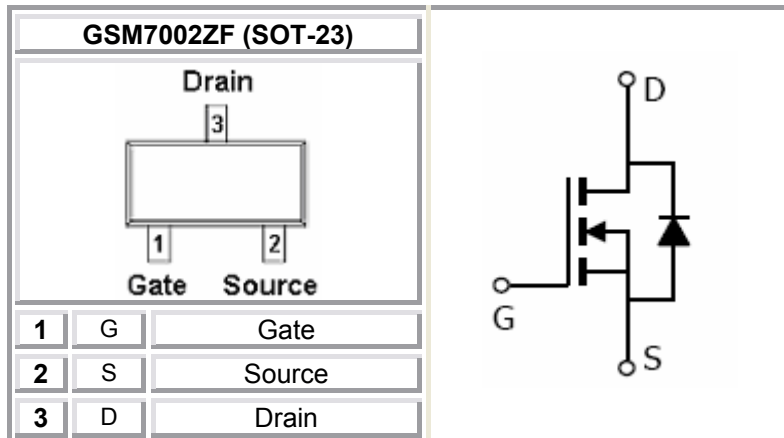
### Features

- 60V/0.50A ,  $R_{DS(ON)} = 6.0\Omega @ V_{GS} = 10V$
- 60V/0.30A ,  $R_{DS(ON)} = 7.0\Omega @ V_{GS} = 5V$
- Super high density cell design for extremely low  $R_{DS(ON)}$
- Exceptional on-resistance and maximum DC current capability
- SOT-23 package design

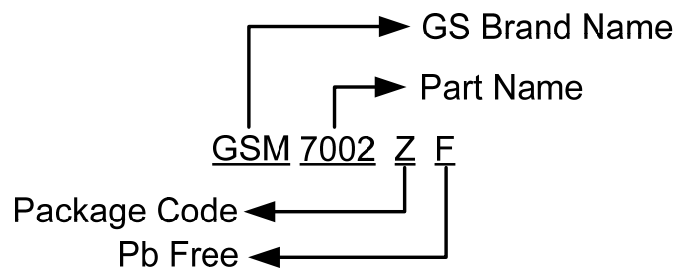
### Applications

- Drivers: Relays, Solenoids, Lamps, Hammers, Display, Memories, Transistors, etc.
- High saturation current capability. Direct Logic-Level Interface: TTL/CMOS
- Battery Operated Systems
- Solid-State Relays

### Packages & Pin Assignments



### Ordering Information



## Marking Information

Part Number	Package	Part Marking
GSM7002ZF	SOT-23	702

## Absolute Maximum Ratings

T<sub>A</sub>=25°C Unless otherwise noted

Symbol	Parameter	Typical	Unit
V <sub>DSS</sub>	Drain-Source Voltage	60	V
V <sub>GSS</sub>	Gate –Source Voltage - Continuous	±20	V
V <sub>GSS</sub>	Gate –Source Voltage - Non Repetitive ( t <sub>p</sub> < 50µs)	±40	V
I <sub>D</sub>	Continuous Drain Current(T <sub>J</sub> =150°C)	T <sub>A</sub> =25 °C 0.3	A
I <sub>DM</sub>	Pulsed Drain Current (*)	1.0	A
P <sub>D</sub>	Power Dissipation	T <sub>A</sub> =25 °C 0.35	W
T <sub>J</sub>	Operating Junction Temperature	-55/150	°C
T <sub>STG</sub>	Storage Temperature Range	-55/150	°C
R <sub>θJA</sub>	Thermal Resistance-Junction to Ambient	375	°C/W

(\*) Pulse width limited by safe operating area

## Electrical Characteristics

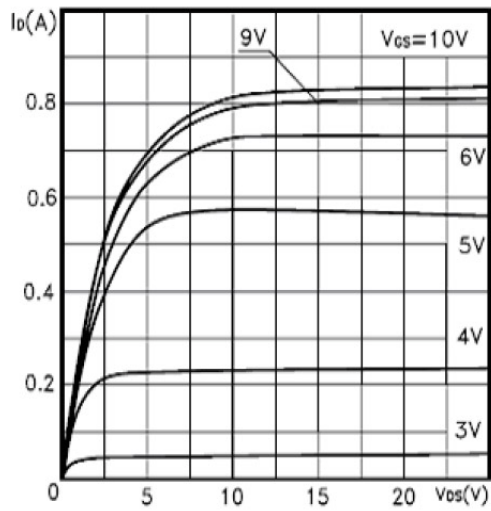
TA=25°C Unless otherwise noted

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static</b>						
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	60			V
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0	1.7	2.5	
$I_{GSS}$	Gate Leakage Current	$V_{DS}=0V, V_{GS}=\pm 20V$			$\pm 100$	nA
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS}=60V, V_{GS}=0V$			1	uA
		$V_{DS}=60V, V_{GS}=0V$ $T_J=125^\circ C$			10	
$R_{DS(on)}$	Drain-Source On-Resistance	$V_{GS}=10V, I_D=0.50A$		2.5	6.0	$\Omega$
		$V_{GS}= 5V, I_D=0.30A$		3.3	7.0	
$I_{SD}$	Source-drain Current				0.35	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				1.4	A
$G_{fs(1)}$	Forward Transconductance	$V_{DS} = 10 V, I_D = 0.5 A$		0.6		S
$V_{SD(1)}$	Diode Forward Voltage	$V_{GS} = 0 V, I_S = 0.12A$		0.85	1.5	V
<b>Dynamic</b>						
$Q_g$	Total Gate Charge	$V_{DD} = 30 V, I_D = 1 A,$ $V_{GS} = 5 V$		1.4	2.0	nC
$Q_{gs}$	Gate-Source Charge			0.8		
$Q_{gd}$	Gate-Drain Charge			0.5		
$C_{iss}$	Input Capacitance	$V_{DS} = 25 V,$ $f = 1 MHz, V_{GS} = 0V$		43		pF
$C_{oss}$	Output Capacitance			20		
$C_{rss}$	Reverse Transfer Capacitance			6		
$t_{d(on)}$	Turn-On Time	$V_{DD} = 30 V, I_D = 0.5 A$ $R_G = 4.7\Omega, V_{GS} = 4.5V$		5		ns
$t_r$				15		
$t_{d(off)}$	Turn-Off Time			7		
$t_f$				8		

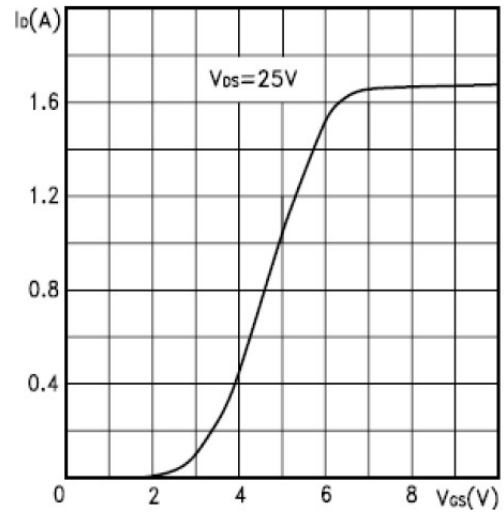
(1) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.

(2) Pulse width limited by safe operating area.

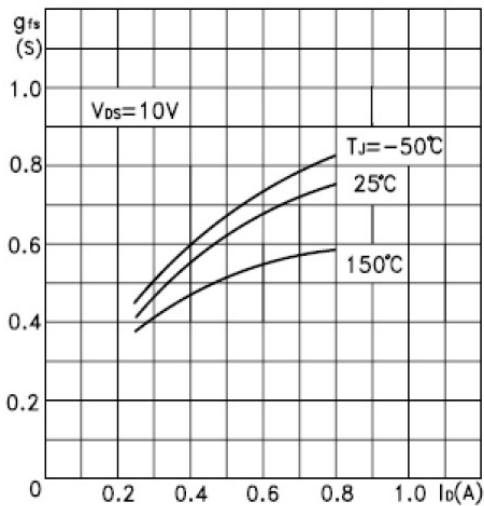
## Typical Performance Characteristics



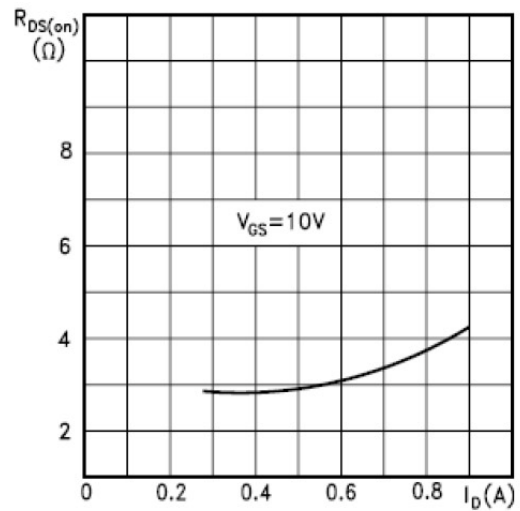
Output Characteristics



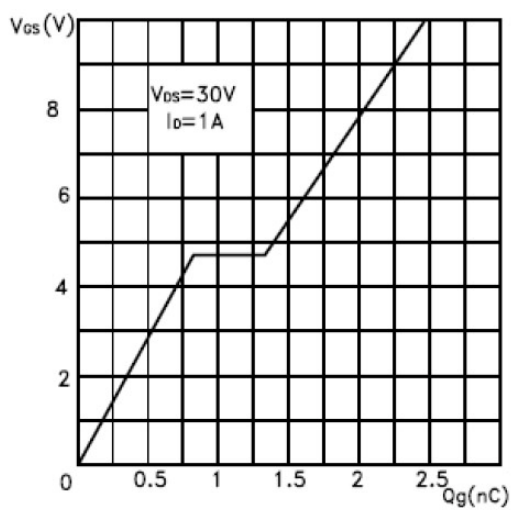
Transfer Characteristics



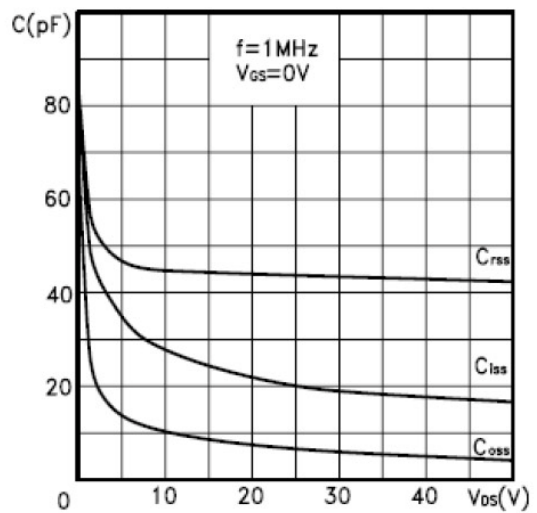
Transconductance



Static Drain-source On Resistance

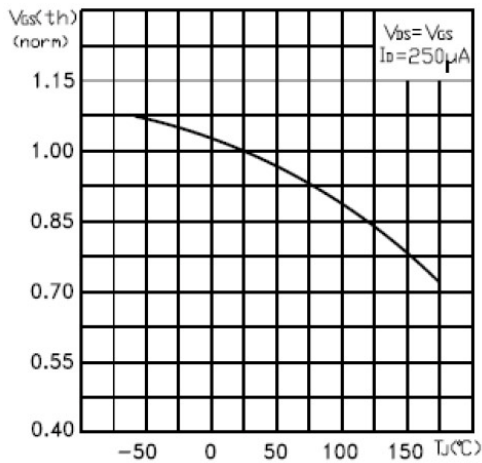


Gate Charge vs. Gate-source Voltage

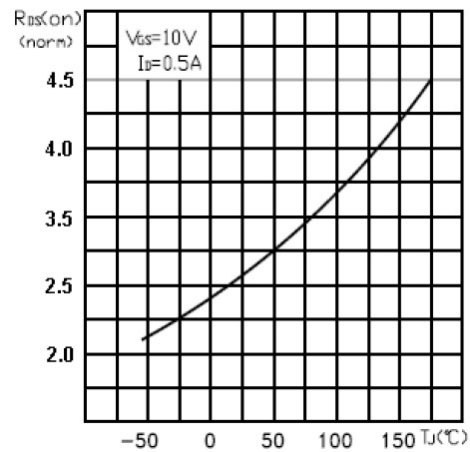


Capacitance Variations

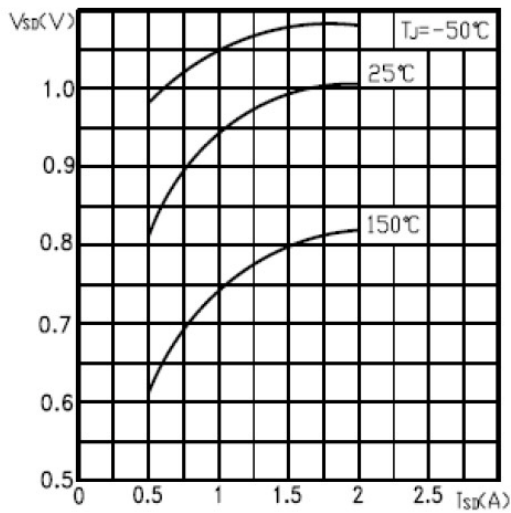
## Typical Performance Characteristics(Continue)



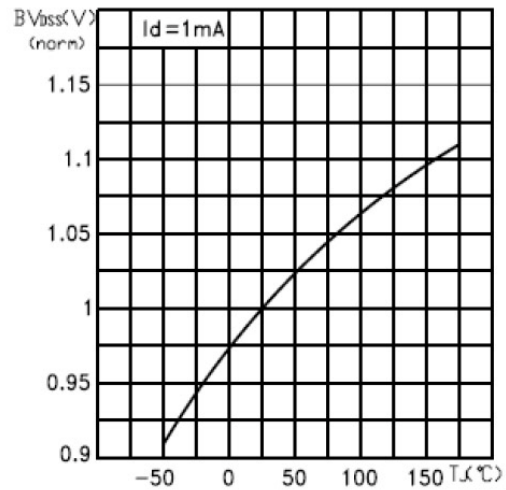
Normalized Gate Threshold Voltage vs. Temperature



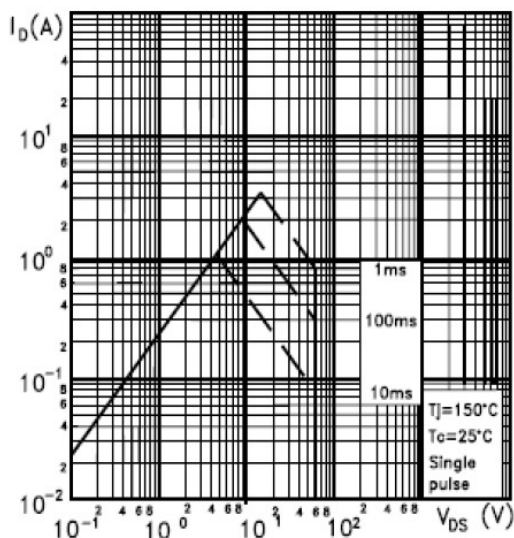
Normalized On Resistance vs. Temperature



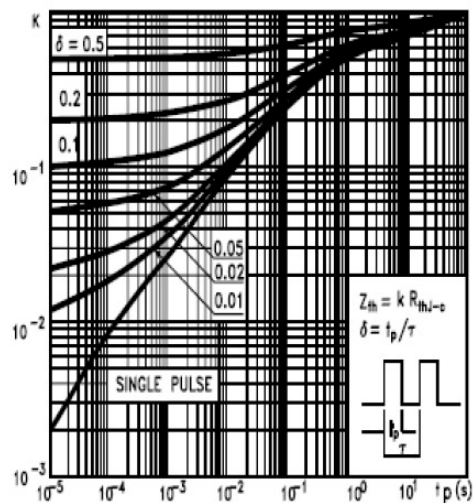
Source-Drain Forward



Normalized BVDSS vs. Temperature

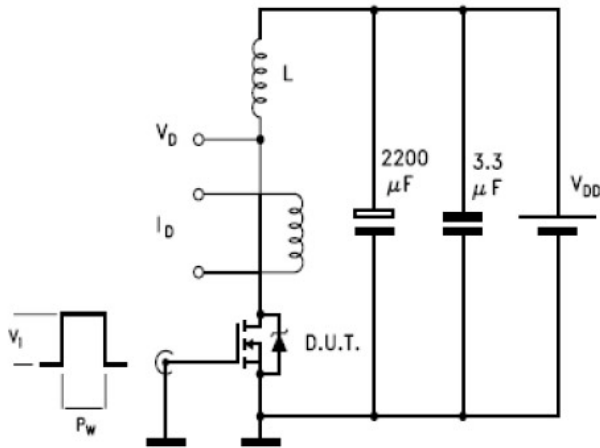


Safe Operating Area

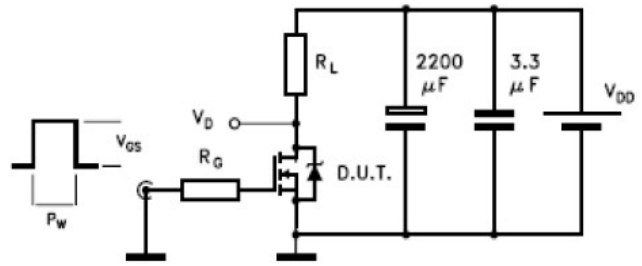


Thermal Impedance

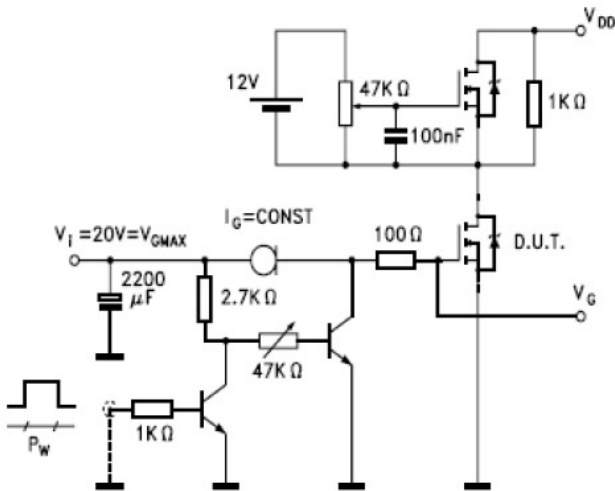
## Typical Testing Circuit



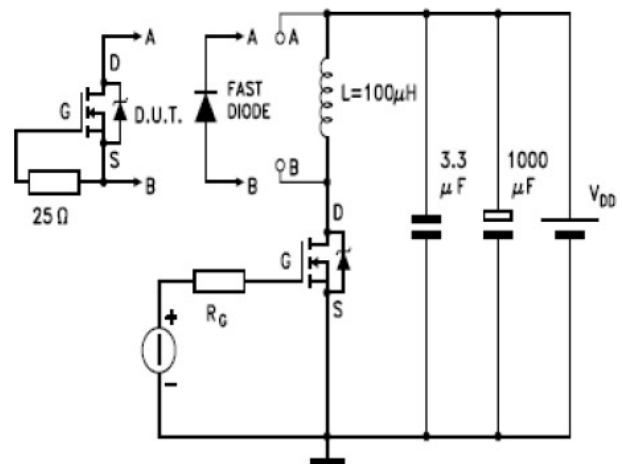
Unclamped Inductive Load Test



Switching Times Test Circuit



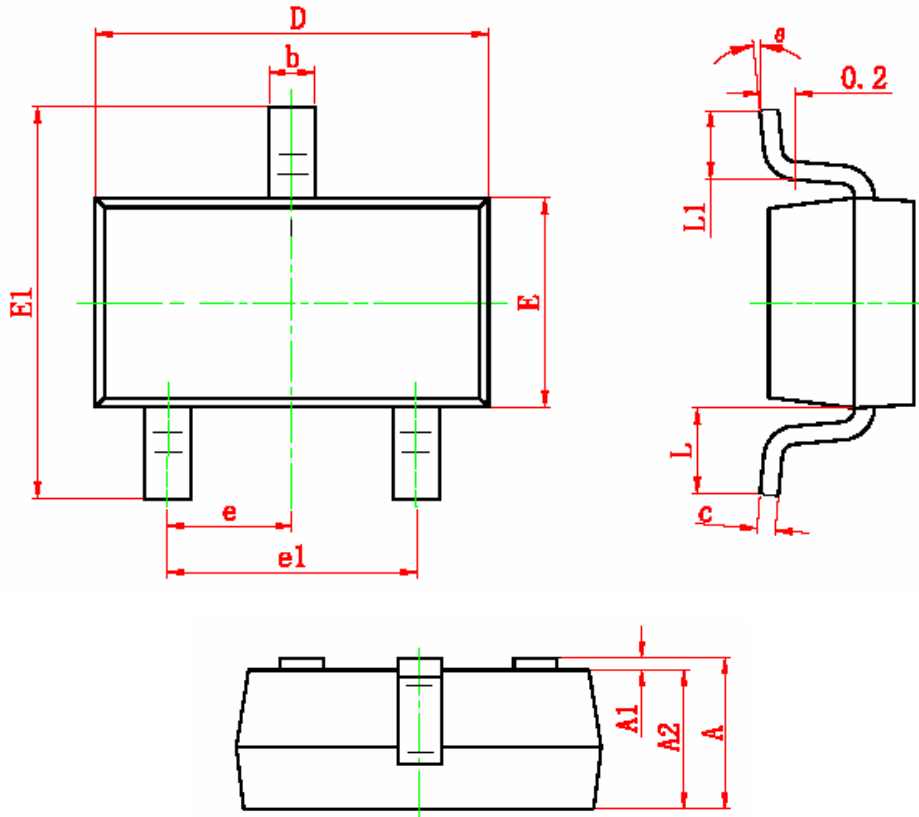
Gate Charge Test Circuit



Test Circuit For Inductive Load Switching and Diode Recovery Times

## Package Dimension

### SOT-23 PLASTIC PACKAGE







Dimensions				
SYMBOL	Millimeters		Inches	
	MIN	MAX	MIN	MAX
A	0.900	1.200	0.035	0.043
A1	0.000	0.100	0.000	0.004
A2	0.900	1.100	0.035	0.039
b	0.300	0.500	0.012	0.020
c	0.080	0.150	0.003	0.006
D	2.800	3.000	0.110	0.118
E	1.200	1.400	0.047	0.055
E1	2.250	2.550	0.089	0.100
e	0.950 TYP		0.037 TYP	
e1	1.800	2.000	0.071	0.079
L	0.550 REF		0.022 REF	
L1	0.300	0.500	0.012	0.020
θ	0°	8°	0°	8°



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## CONTACT US

GS Headquarter	
	4F.,No.43-1,Lane11,Sec.6,Minquan E.Rd NeiHu District Taipei City 114, Taiwan (R.O.C)
	886-2-2657-9980
	886-2-2657-3630
	sales_twn@gs-power.com

Wu-Xi Branch	
	No.21 Changjiang Rd., WND, Wuxi, Jiangsu, China (INFO. & TECH. Science Park Building A 210 Room)
	86-510-85217051
	86-510-85211238
	sales_cn@gs-power.com

RD Division	
	824 Bolton Drive Milpitas. CA. 95035
	1-408-457-0587