

Gate Turn-off Thyristor

DS4091-4 July 2014 (LN31735)

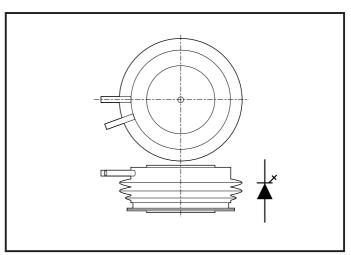
APPLICATIONS

- Variable speed A.C. motor drive inverters (VSD-AC)
- Uninterruptable Power Supplies
- High Voltage Converters
- Choppers
- Welding
- Induction Heating
- DC/DC Converters.

FEATURES

- Double Side Cooling
- High Reliability In Service
- High Voltage Capability
- Fault Protection Without Fuses
- High Surge Current Capability
- Turn-off Capability Allows Reduction In Equipment Size And Weight. Low Noise Emission Reduces Acoustic Cladding Necessary For Environmental Requirements

dV_D/dt 1000V/μs di₋/dt 300A/μs



Outline type code: P. See Package Details for further information.

VOLTAGE RATINGS

Type Number	Repetitive Peak Off-state Voltage V DRM V	Repetitive Peak Reverse Voltage V _{RRM} V	Conditions
DG408BP45	4500	16	$T_{vj} = 125^{\circ}C, I_{DM} = 50mA,$ $I_{RRM} = 50mA$

CURRENT RATINGS

Symbol	Parameter	Conditions	Max.	Units
I _{TCM}	Repetitive peak controllable on-state current	$V_{D} = V_{DRM}, T_{j} = 125^{\circ}C, di_{GQ}/dt = 30A/\mu s, Cs = 1.0\mu F$	1000	Α
I _{T(AV)}	Mean on-state current	T _{HS} = 80°C. Double side cooled. Half sine 50Hz.	320	Α
I _{T(RMS)}	RMS on-state current	T _{HS} = 80°C. Double side cooled. Half sine 50Hz.	500	Α

SURGE RATINGS

Symbol	Parameter	Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine. T _j = 125°C	7.0	kA
l²t	I²t for fusing	10ms half sine. T _j =125°C	0.245 x 10 ⁶	A²s
di _⊤ /dt	Critical rate of rise of on-state current	$V_D = 3000V$, $I_T = 1000A$, $T_j = 125^{\circ}C$, $I_{FG} > 30A$, Rise time $> 1.5\mu s$	300	A/μs
dV _□ /dt	Rate of rise of off-state voltage	To 66% V_{DRM} ; $R_{GK} \le 1.5Ω$, $T_j = 125$ °C	225	V/μs
		To 66% V _{DRM} ; V _{RG} = -2V, T _j = 125°C	1000	V/μs
L _s	Peak stray inductance in snubber circuit	-	200	nH

GATE RATINGS

Symbol	Parameter	Conditions	Min.	Max.	Units
V_{RGM}	Peak reverse gate voltage	This value maybe exceeded during turn-off	-	16	V
I _{FGM}	Peak forward gate current		20	70	Α
P _{FG(AV)}	Average forward gate power		-	10	W
P _{RGM}	Peak reverse gate power		-	15	kW
di _{gq} /dt	Rate of rise of reverse gate current		15	60	A/μs
t _{ON(min)}	Minimum permissable on time		20	-	μs
t _{OFF(min)}	Minimum permissable off time		100	-	μs

THERMAL RATINGS AND MECHANICAL DATA

Symbol	Parameter	Conditions		Min.	Max.	Units
	DC thermal resistance - junction to heatsink surface	Double side cooled		-	0.041	°C/W
R _{th(j-hs)}		Anode side cooled		-	0.07	°C/W
		Cathode side cooled		-	0.1	°C/W
R _{th(c-hs)}	Contact thermal resistance	Clamping force 12.0kN With mounting compound	per contact	-	0.009	°C/W
T _{vj}	Virtual junction temperature			-	125	°C
T _{OP} /T _{stg}	Operating junction/storage temperature range			-40	125	°C
-	Clamping force			11.0	15.0	kN

CHARACTERISTICS

T _j = 125°C unless stated otherwise						
Symbol	Parameter	Conditions	Min.	Max.	Units	
V_{TM}	On-state voltage	At 1000A peak, I _{G(ON)} = 4A d.c.	-	3.5	V	
I _{DM}	Peak off-state current	V _{DRM} = 4500V, V _{RG} = 0V	-	50	mA	
I _{RRM}	Peak reverse current	At V _{RRM}	-	50	mA	
$V_{\rm GT}$	Gate trigger voltage	V _D = 24V, I _T = 100A, T _j = 25°C	-	1.0	V	
I _{GT}	Gate trigger current	V _D = 24V, I _T = 100A, T _j = 25°C	-	1.5	Α	
I _{RGM}	Reverse gate cathode current	V _{RGM} = 16V, No gate/cathode resistor	-	50	mA	
E _{on}	Turn-on energy	V _D = 3000V	-	2300	mJ	
t _d	Delay time	$I_{T} = 1000A$, $dI_{T}/dt = 300A/\mu s$	-	1.5	μs	
t _r	Rise time	I_{FG} = 30A, rise time < 1.5 μ s	-	5.0	μs	
E _{OFF}	Turn-off energy		-	4120	mJ	
t _{gs}	Storage time		-	14.0	μs	
t _{gf}	Fall time	$I_{T} = 1000A, V_{DM} = V_{DRM}$	-	1.5	μs	
t _{gq}	Gate controlled turn-off time	Snubber Cap Cs = 1.0μF,	-	15.5	μs	
Q_{GQ}	Turn-off gate charge	di _{GQ} /dt = 30A/μs	-	3000	μС	
Q_{GQT}	Total turn-off gate charge		-	6000	μС	
I _{GQM}	Peak reverse gate current		-	420	А	

CURVES

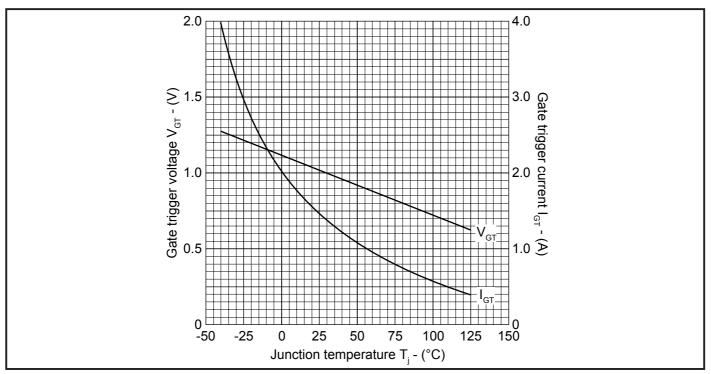
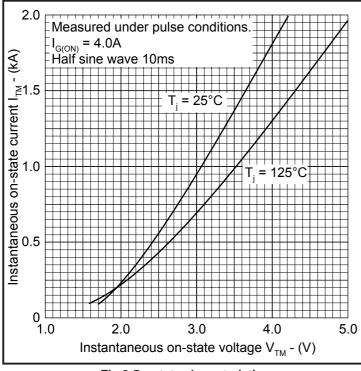
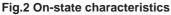


Fig.1 Maximum gate trigger voltage/current vs junction temperature





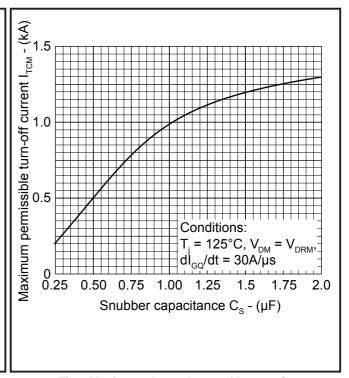


Fig.3 Maximum dependence of $\rm I_{TCM}$ on $\rm C_S$

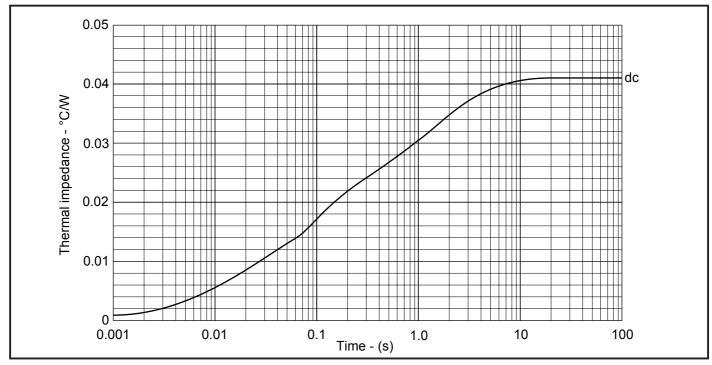


Fig.4 Maximum (limit) transient thermal impedance - double side cooled

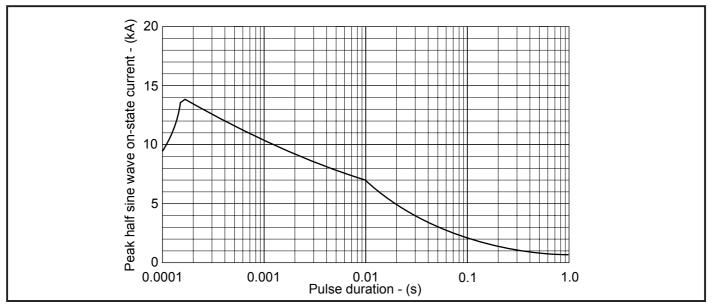


Fig.5 Surge (non-repetitive) on-state current vs time

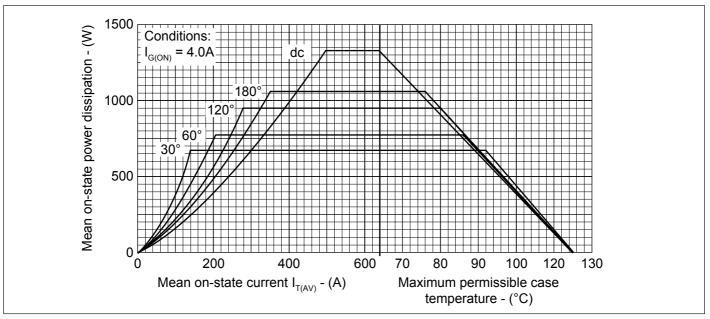


Fig.6 Steady state rectangluar wave conduction loss - double side cooled

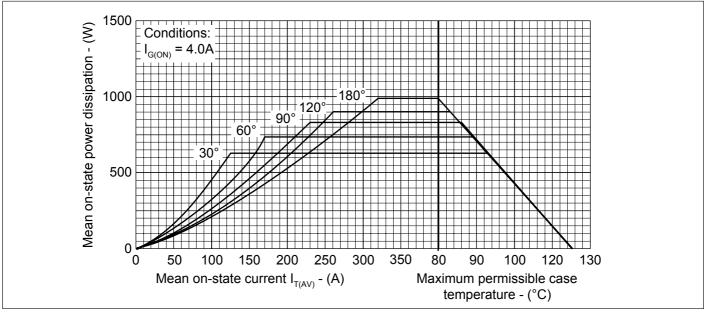


Fig.7 Steady state sinusoidal wave conduction loss - double side cooled

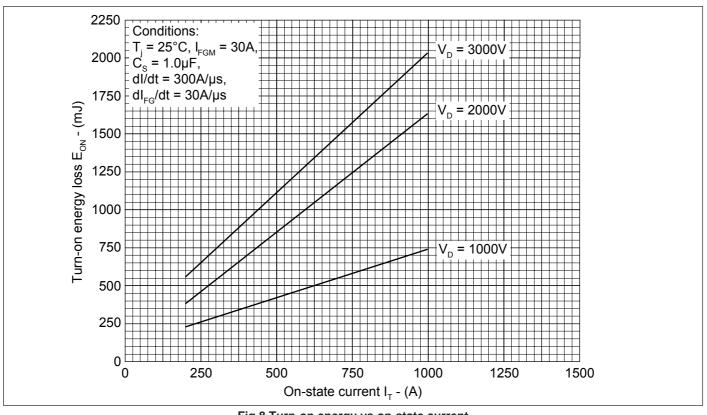


Fig.8 Turn-on energy vs on-state current

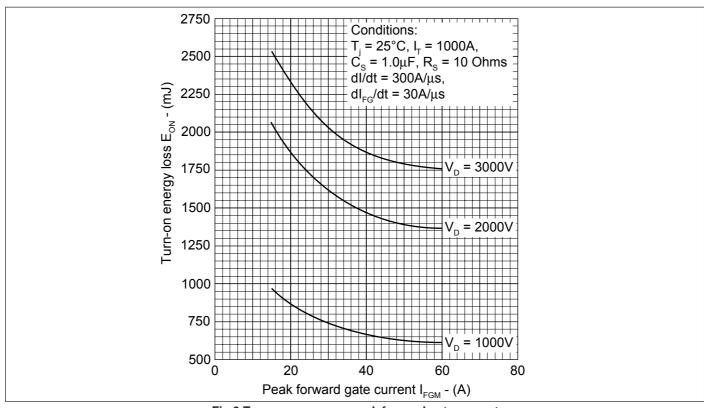


Fig.9 Turn-on energy vs peak forward gate current

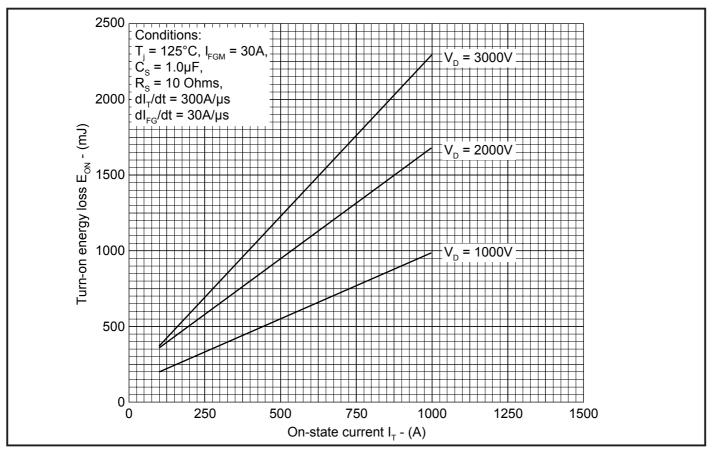


Fig.10 Turn-on energy vs on-state current

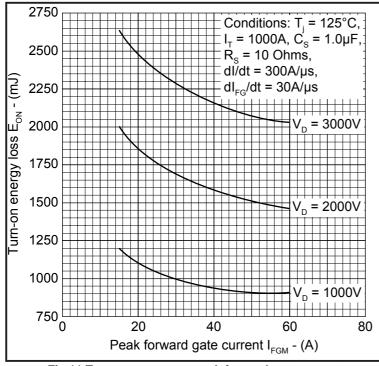


Fig.11 Turn-on energy vs peak forward gate current

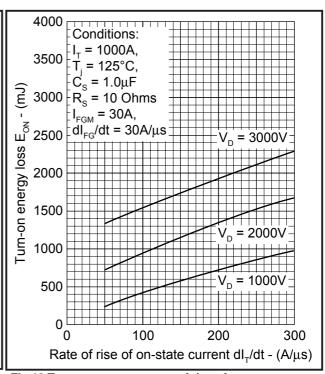


Fig.12 Turn-on energy vs rate of rise of on-state current

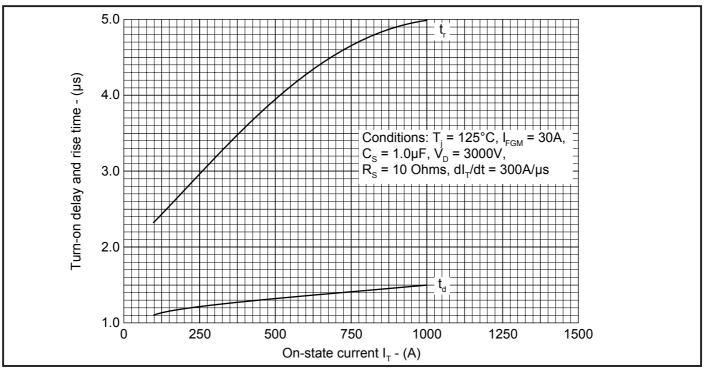


Fig.13 Delay time & rise time vs turn-on current

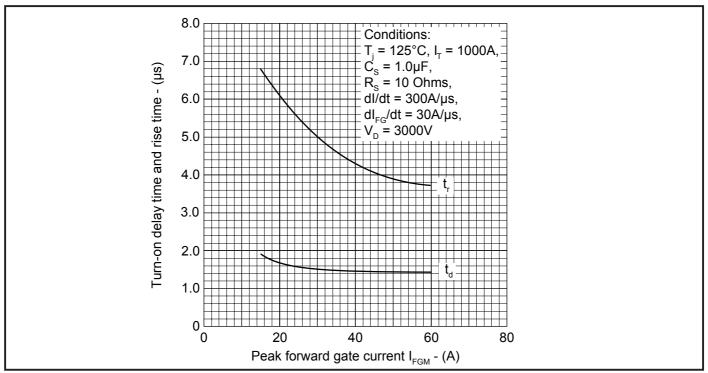


Fig.14 Delay time & rise time vs peak forward gate current

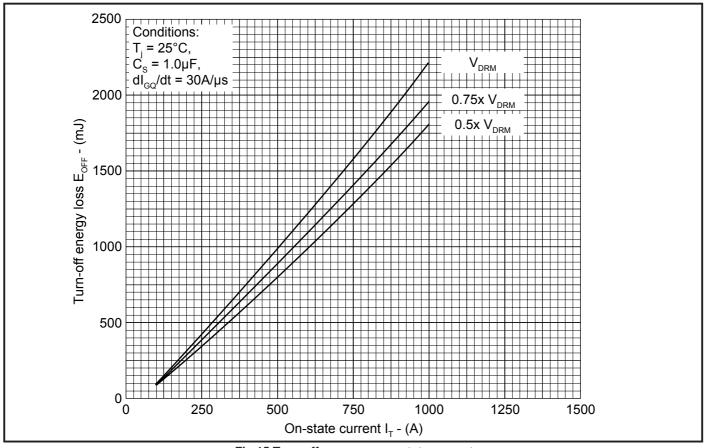


Fig.15 Turn-off energy vs on-state current

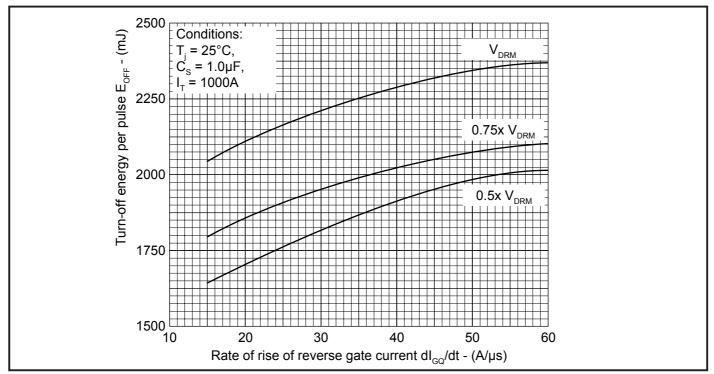


Fig.16 Turn-off energy vs rate of rise of reverse gate current

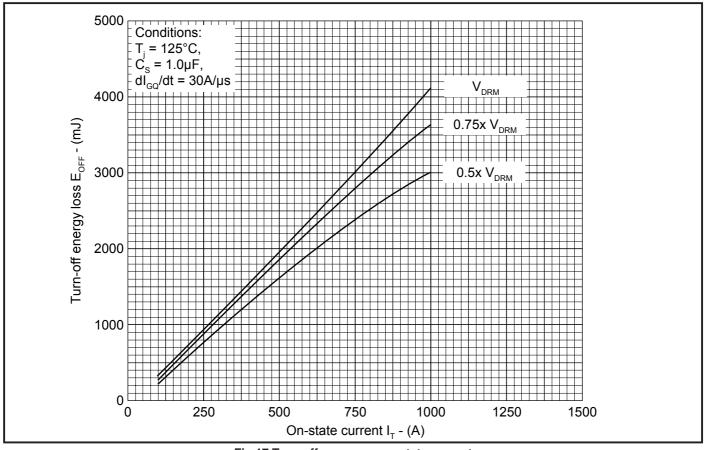


Fig.17 Turn-off energy vs on-state current

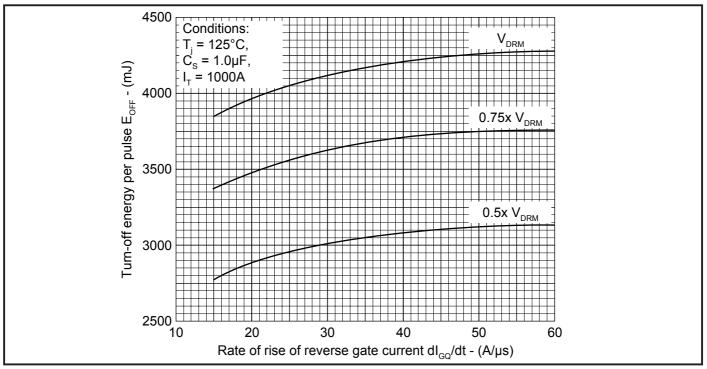


Fig.18 Turn-off energy loss vs rate of rise of reverse gate current

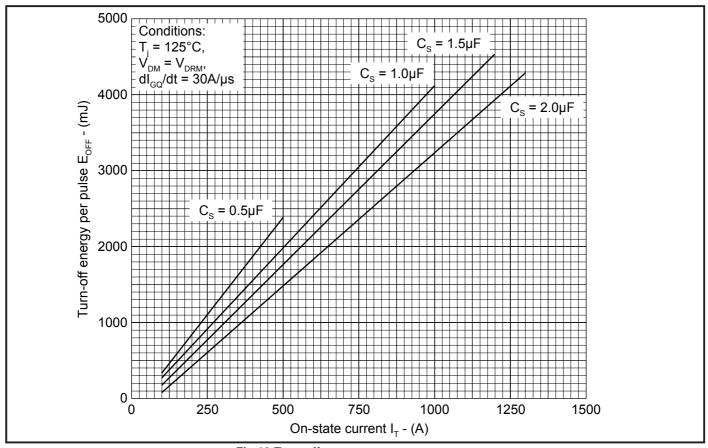


Fig.19 Turn-off energy vs on-state current

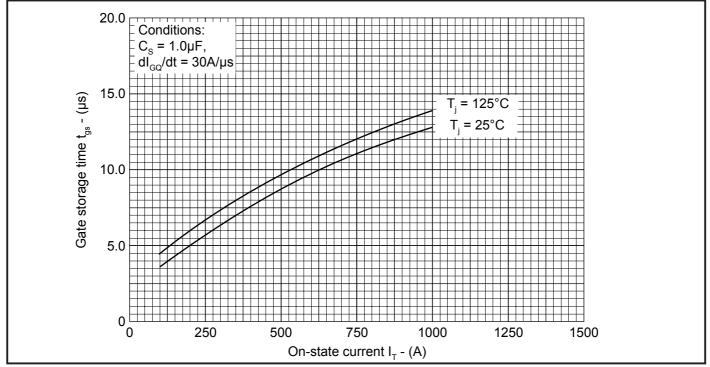


Fig.20 Gate storage time vs on-state current

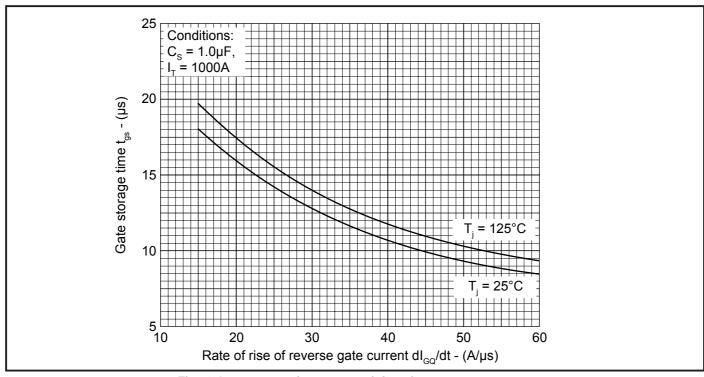


Fig.21 Gate storage time vs rate of rise of reverse gate current

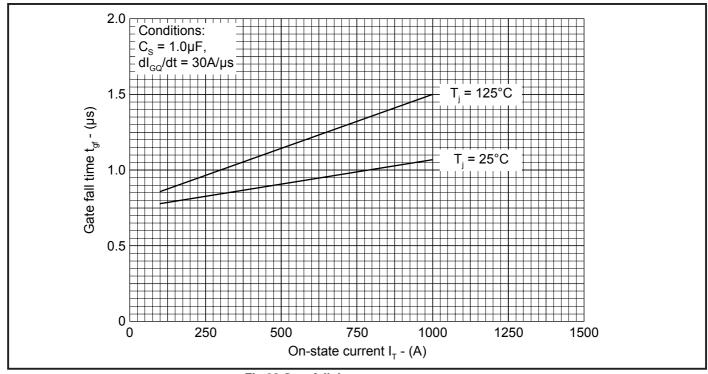


Fig.22 Gate fall time vs on-state current

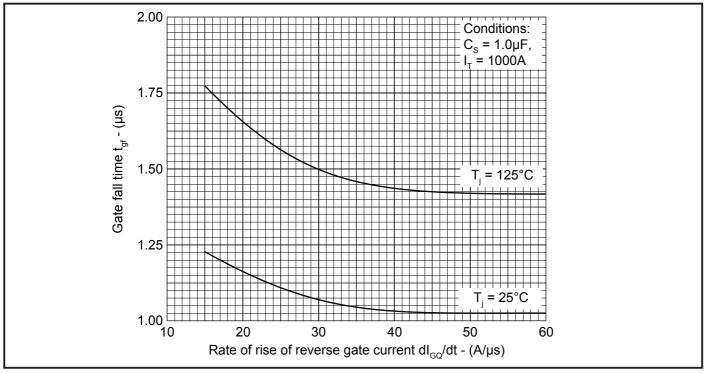


Fig.23 Gate fall time vs rate of rise of reverse gate current

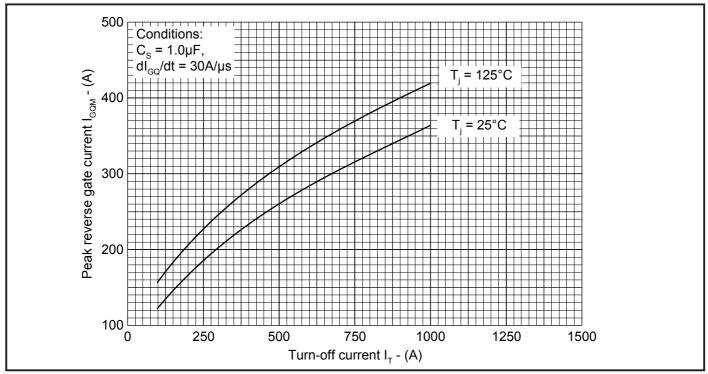


Fig.24 Peak reverse gate current vs turn-off current

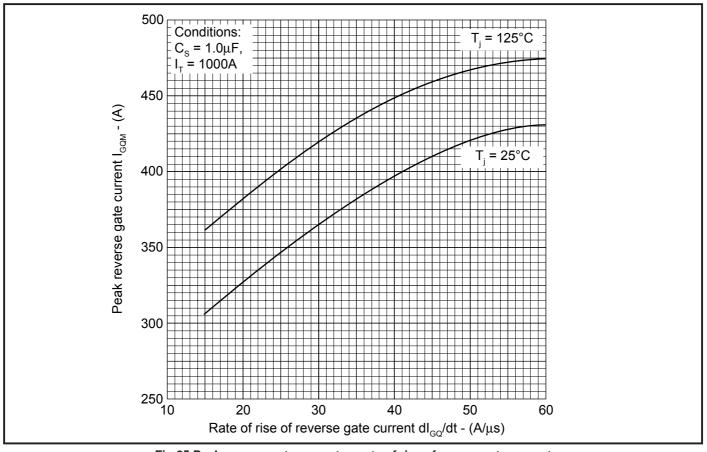


Fig.25 Peak reverse gate current vs rate of rise of reversegate current

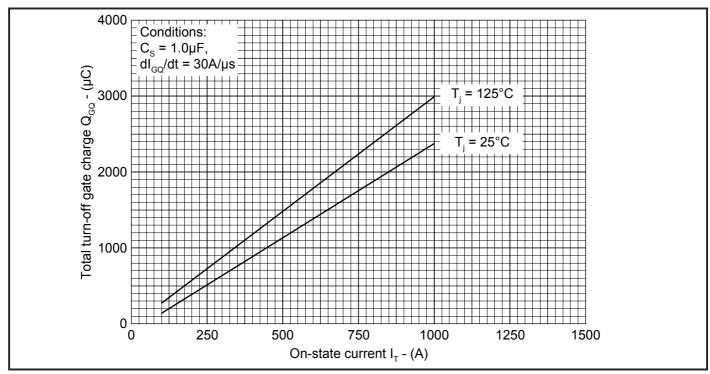


Fig.26 Turn-off gate charge vs on-state current

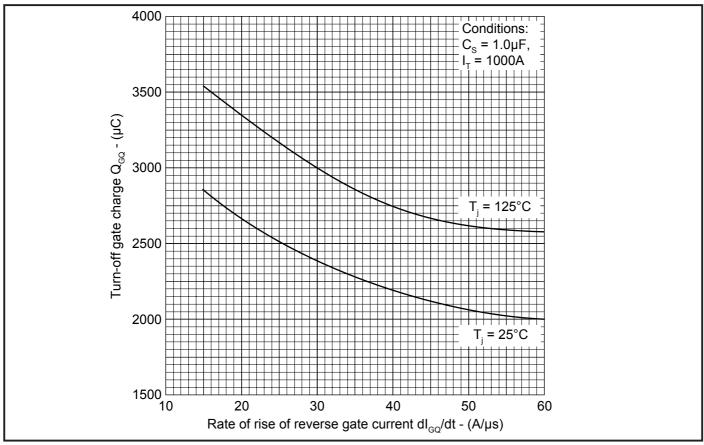


Fig.27 Turn-off gate charge vs rate of rise of reverse gate current

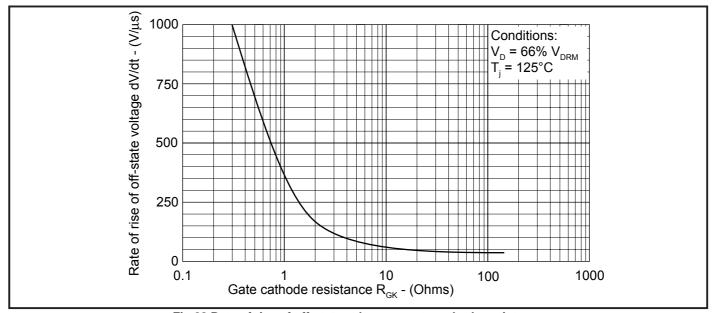


Fig.28 Rate of rise of off-state voltage vs gate cathode resistance

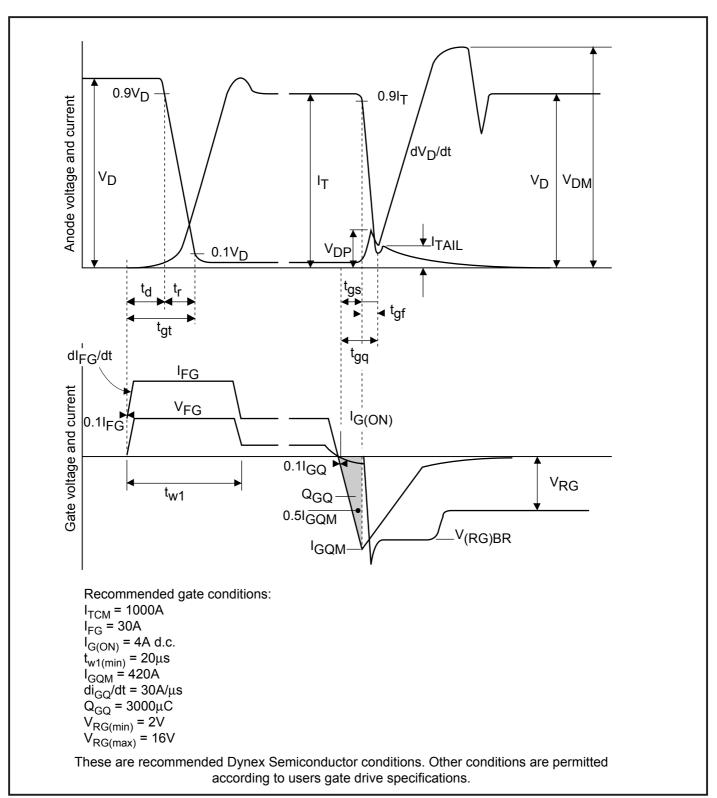
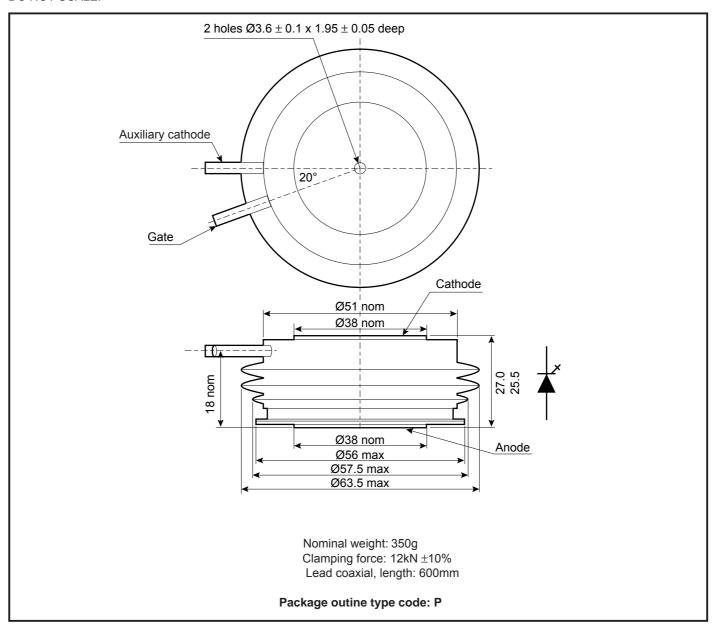


Fig.29 General switching waveforms

PACKAGE DETAILS

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ASSOCIATED PUBLICATIONS

Title	Application Note	
	Number	
Calculating the junction temperature or power semiconductors	AN4506	
GTO gate drive units	AN4571	
Recommendations for clamping power semiconductors	AN4839	
Use of V _{TO} , r _T on-state characteristic	AN5001	
Impoved gate drive for GTO series connections	AN5177	



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