DCR3640H85

Phase Control Thyristor

Preliminary Information

DS6140-2 October 2014 (LN32030)

FEATURES

- Double Side Cooling
- High Surge Capability

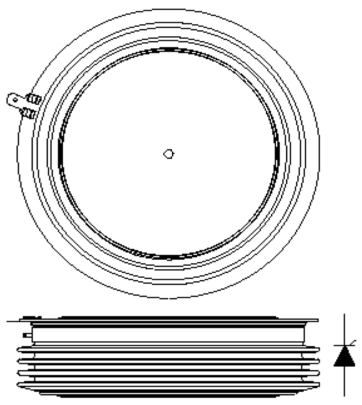
APPLICATIONS

- Bridge Rectifiers
- High Voltage Power Supplies
- Motor Drives

KEY PARAMETERS

V_{DRM}	**8500V**
$I_{T(AV)}$	**3640A**
I_{TSM}	**54000A**
dV/dt*	**2000V/µs**
dI/dt	**200A/µs**

*** Higher dV/dt selections available**



Outline type code: H

(See Package Details for further information)

Fig. 1 Package outline

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR3640H85* DCR3640H80 DCR3640H75	8500 8000 7500	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 600mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.
*8200V @ -40^{0}C, 8500V @ 0^0 C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR3640H85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	3640	A
$I_{T(RMS)}$	RMS value	-	5718	A
I_T	Continuous (direct) on-state current	-	5306	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	54.0	kA
I^2t	I^2t for fusing	V_R = 0	14.58	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.004255	°C/W
		Single side cooled	Anode DC	-	0.008	°C/W
			Cathode DC	-	0.0093	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 135.0kN	Double side	-	0.0009	°C/W
		(with mounting compound)	Single side	-	0.0018	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			120	155	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	600	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	2000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	500	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	500 to 4000A at T_{case} = 125°C		-	1.21	V
	Threshold voltage – High level	4000 to 8000A at T_{case} = 125°C		-	1.4067	V
r_T	On-state slope resistance – Low level	500A to 4000A at T_{case} = 125°C		-	0.33	mΩ
	On-state slope resistance – High level	4000A to 8000A at T_{case} = 125°C		-	0.2767	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	I_T = 3000A, T_j = 125°C, V_R = 200V, dI/dt = 1A/µs, dV_{DR}/dt = 20V/µs linear			1000	µs
Q_S	Stored charge	I_T = 3000A, T_j = 125°C, dI/dt – 1A/µs, V_{Rpeak} ~5100V, V_R ~ 3400V		3400	6700	µC
I_{RR}	Reverse recovery current			46	63	A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% $V_{DRM,}$ T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	350	mA
I_{GD}	Gate non-trigger current	At 50% $V_{DRM,}$ T_{case} = 125°C	10	mA

CURVES

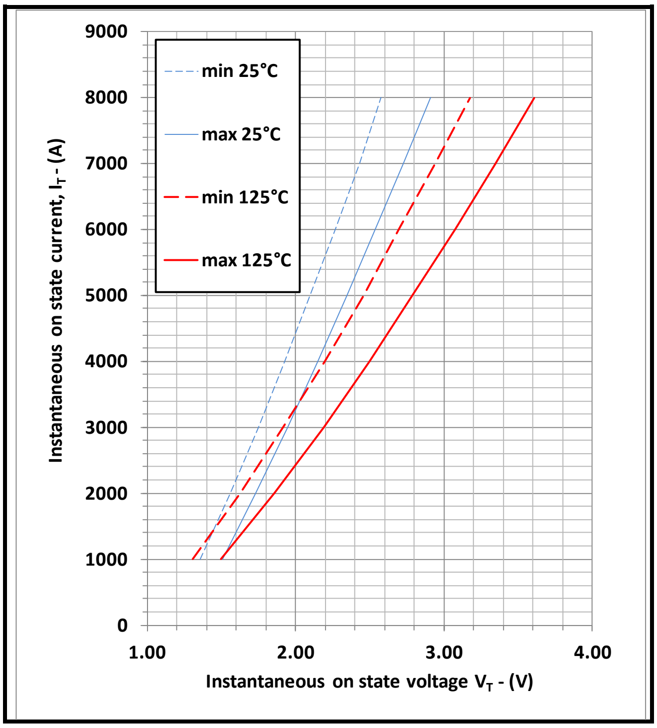


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 2.035252
B = -0.20854
C = 0.000150
D = 0.02514

these values are valid for T_j = 125°C for I_T 500A to 8000A

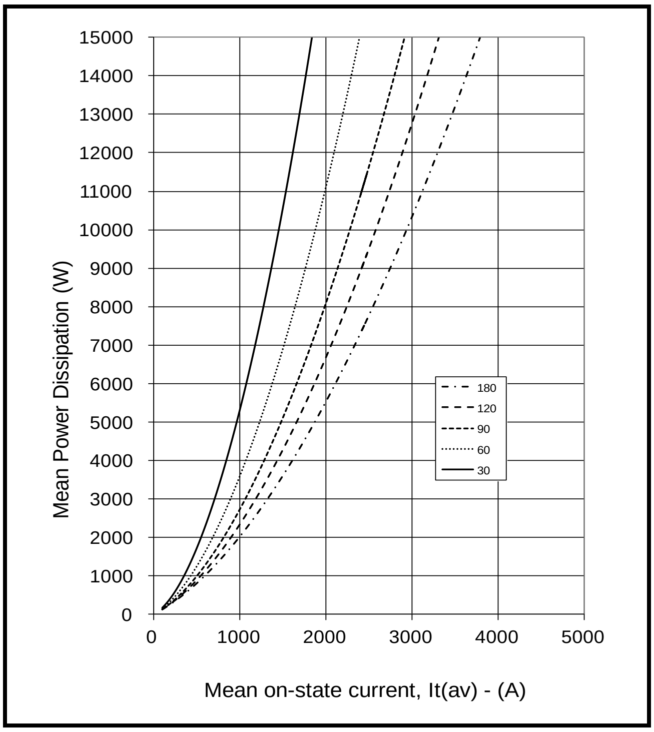


Fig.3 On-state power dissipation – sine wave

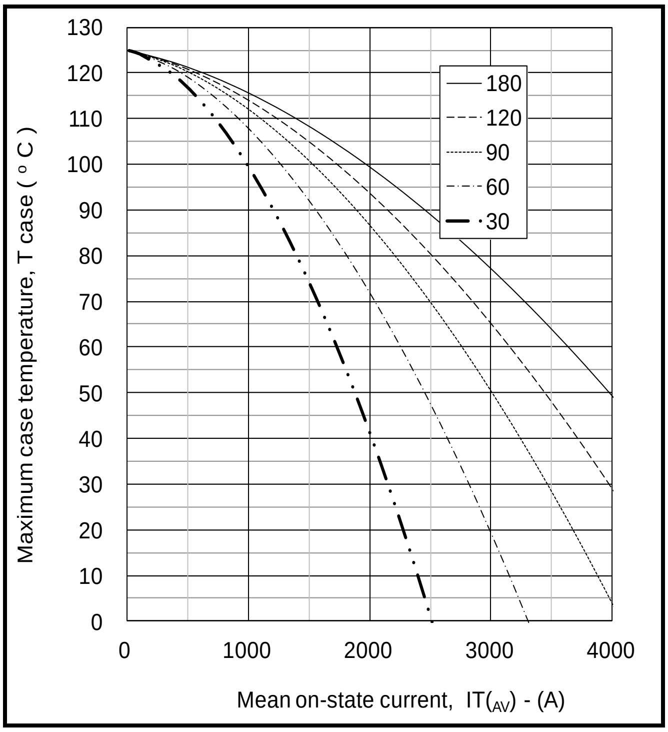


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

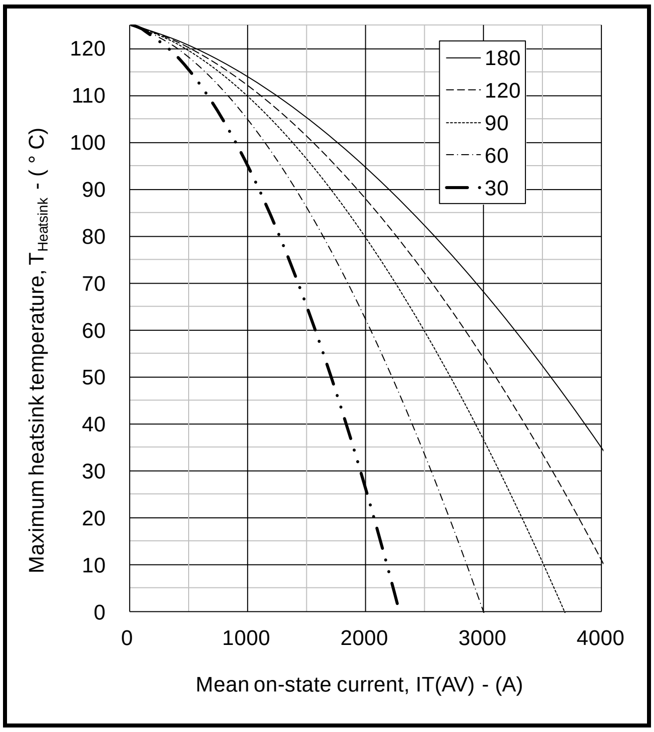


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

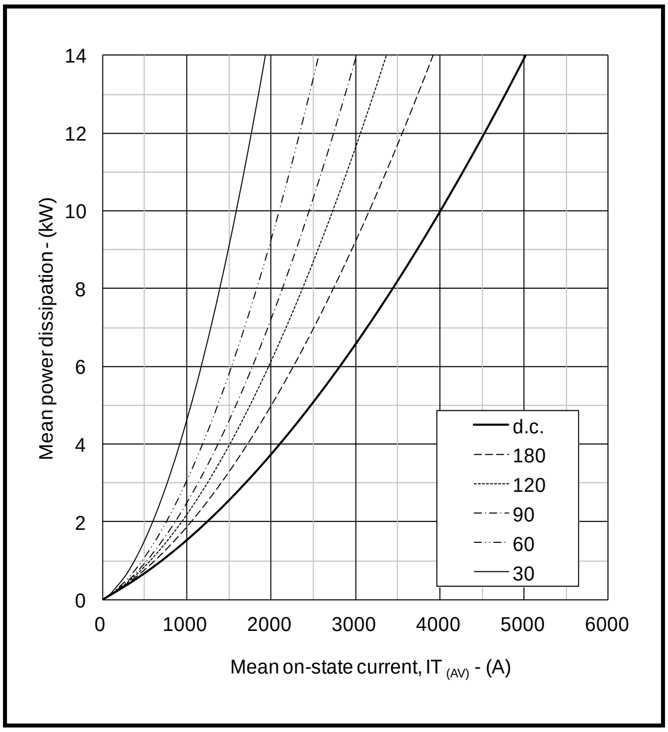


Fig.6 On-state power dissipation – rectangular wave

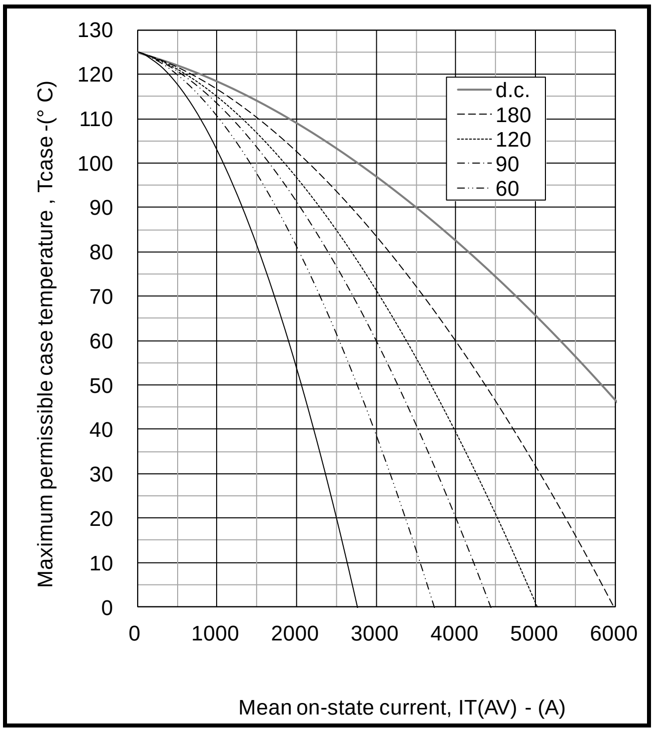


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

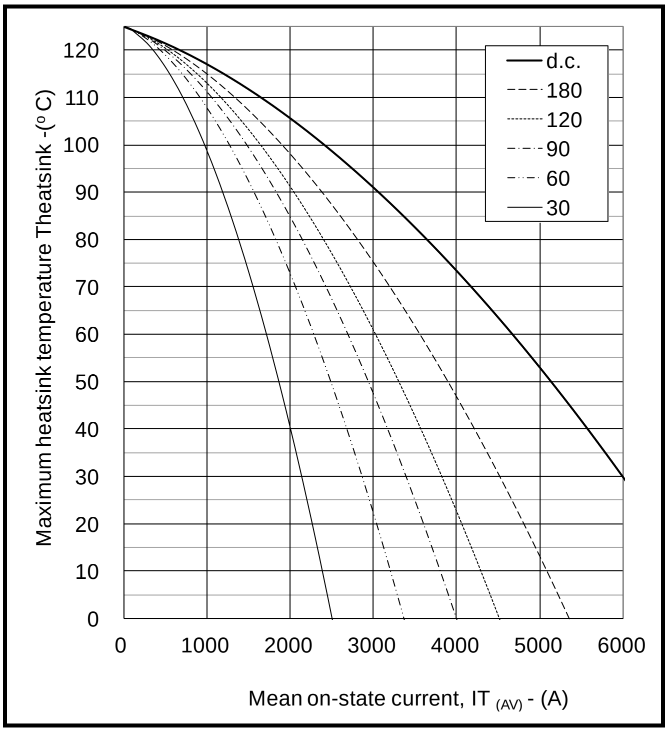
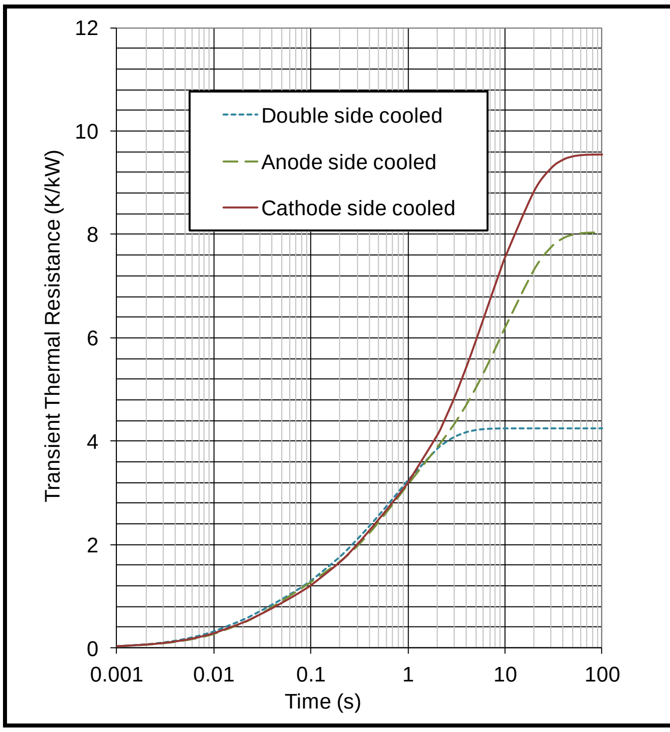


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	1.24786361	0.8334561	0.60621847	1.56769894
	T_i (s)	0.67007122	0.14563223	0.01981569	1.28702484
Anode side cooled	R_i (°C/kW)	0.51177271	1.94595762	0.91956601	4.66635596
	T_i (s)	2.89822124	0.50524092	0.0358286	10.6466908
Cathode side cooled	R_i (°C/kW)	2.41723953	1.53684913	0.62607497	4.9592331
	T_i (s)	3.44130269	0.26943359	0.02350127	10.172444

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T / T_i))]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.38	0.26
120	0.44	0.37
90	0.49	0.43
60	0.54	0.49
30	0.58	0.55
15	0.60	0.58

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.32	0.23
120	0.36	0.31
90	0.41	0.36
60	0.45	0.40
30	0.48	0.45
15	0.49	0.48

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.33	0.23
120	0.38	0.33
90	0.43	0.37
60	0.47	0.43
30	0.51	0.48
15	0.52	0.51

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

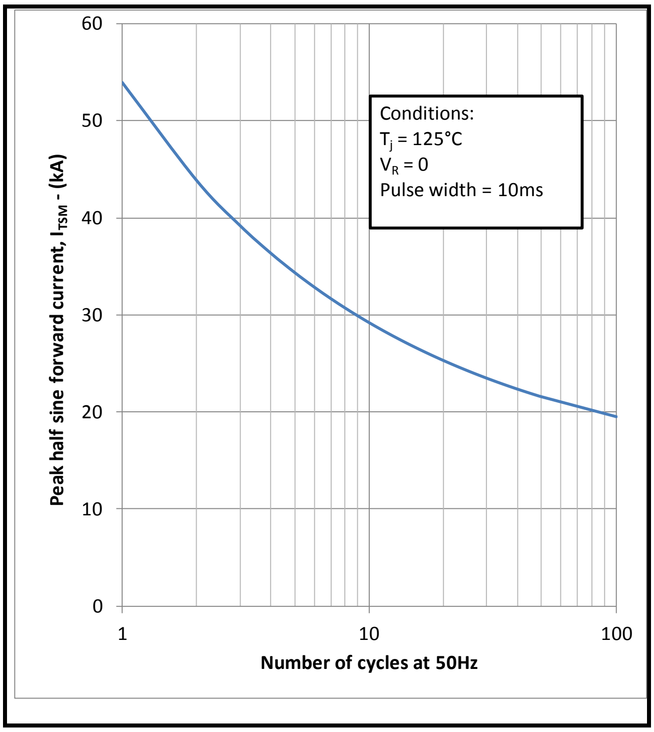


Fig.10 Multi-cycle surge current

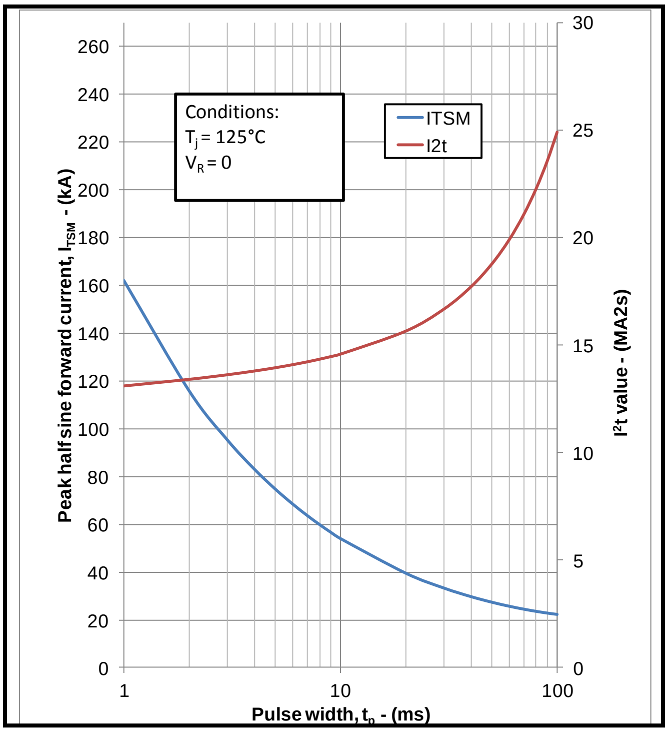


Fig.11 Single-cycle surge current

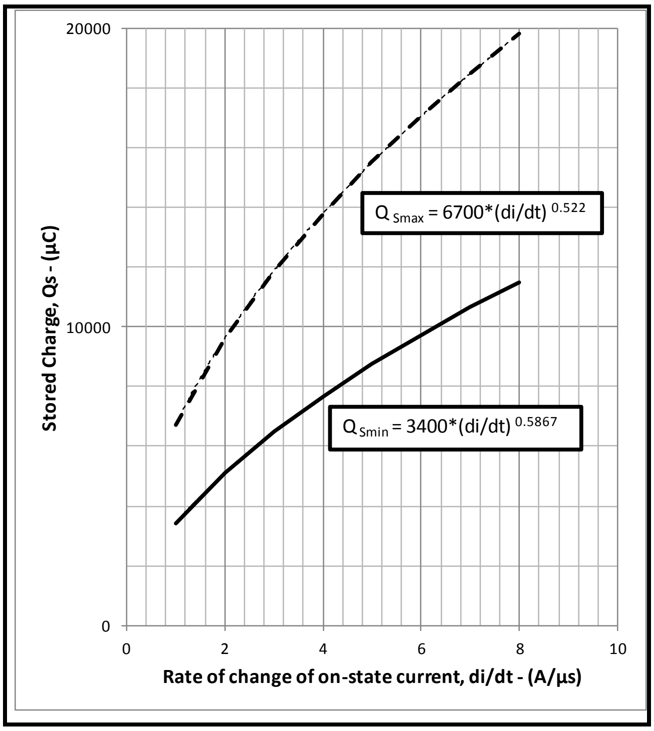


Fig.12 Stored charge

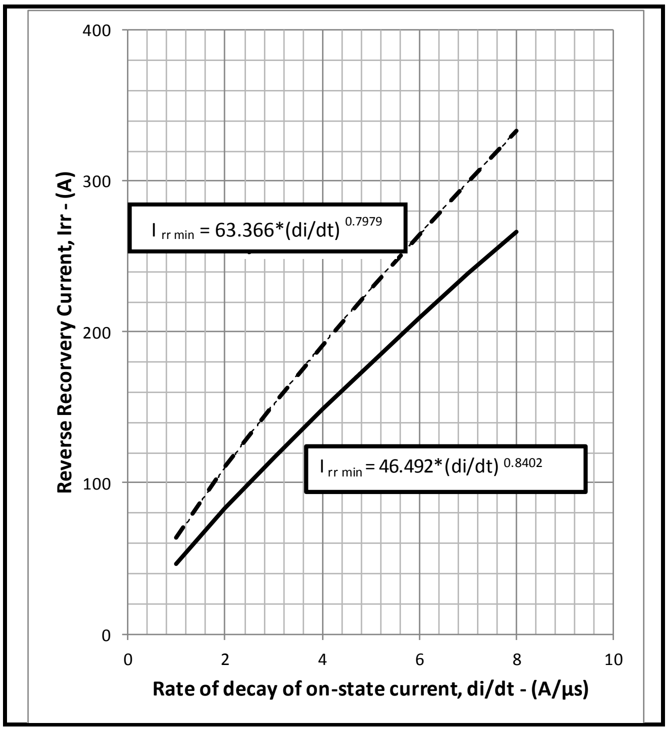
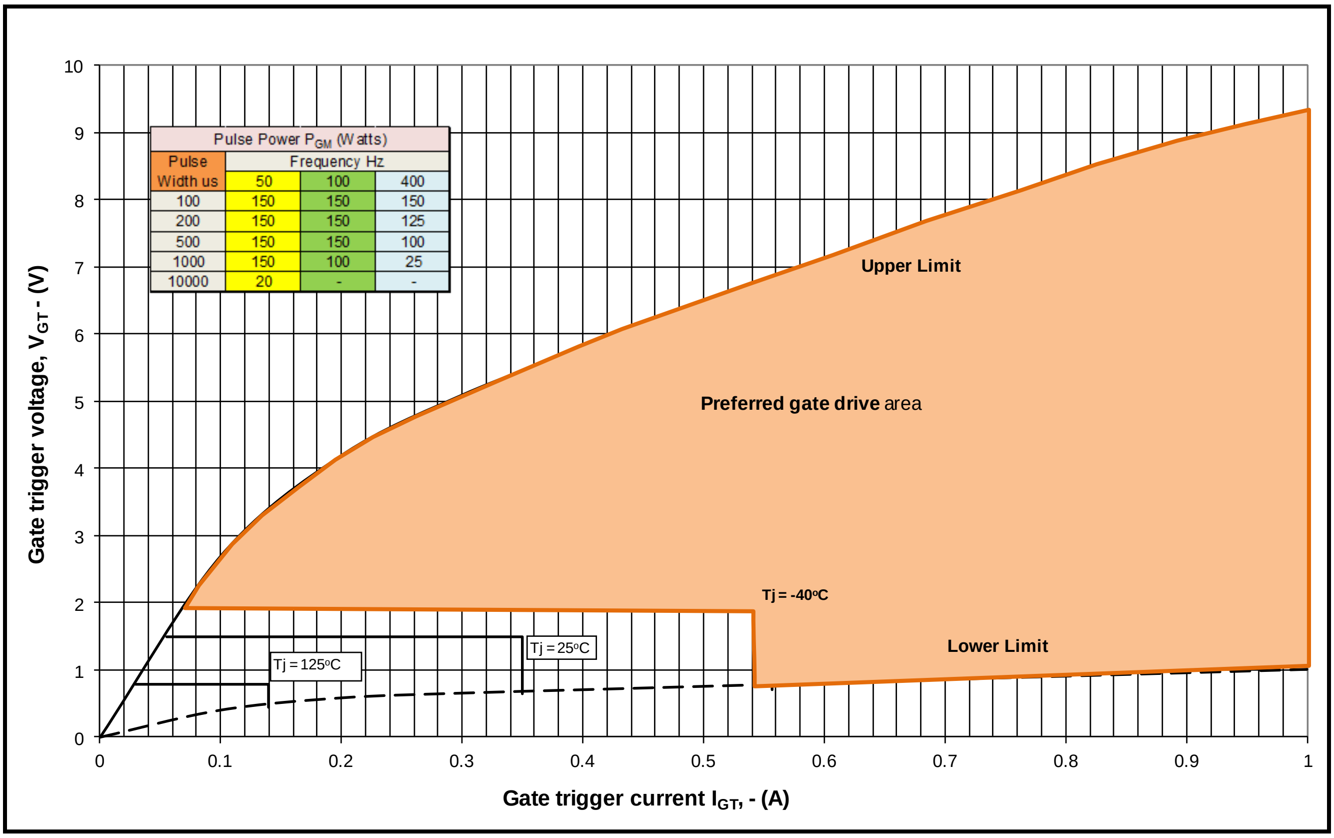


Fig.13 Reverse recovery current



Pulse Power P_{GM} (Watts)

Pulse Width us	Frequency Hz 50	100	400
100	150	150	150
200	150	150	125
500	150	150	100
1000	150	100	25
10000	20	-	-

Fig14 Gate Characteristics

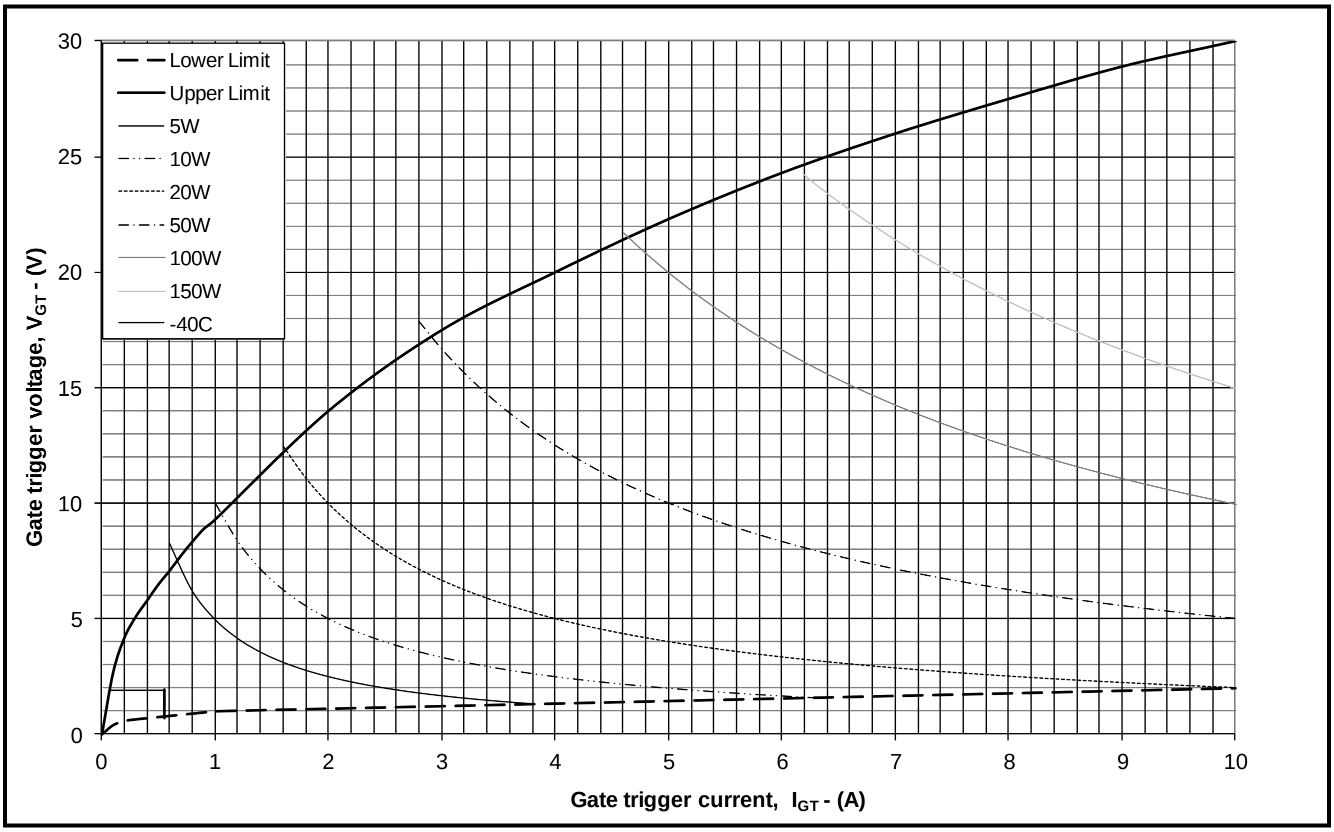
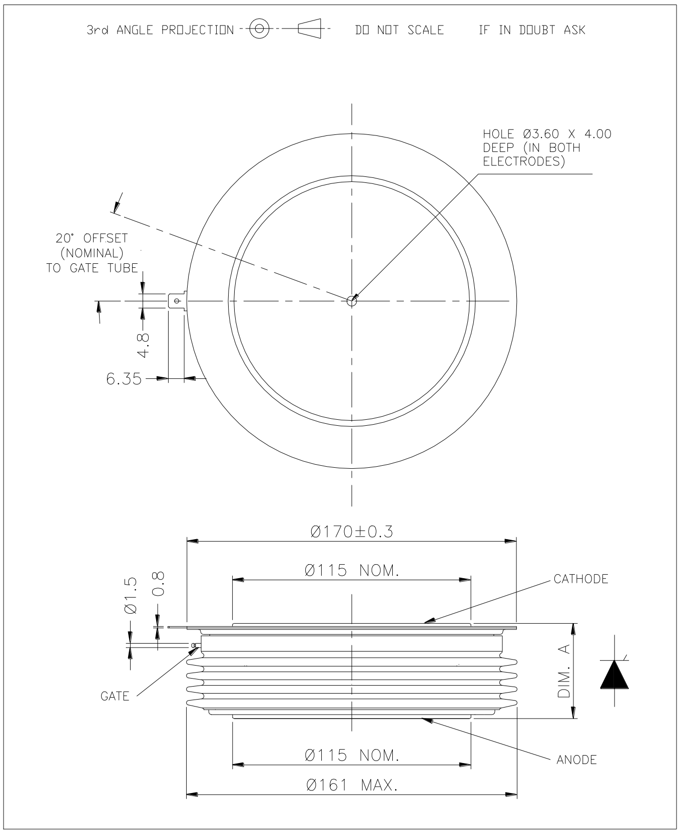


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

Device	Maximum Thickness (mm)	Minimum Thickness (mm)
DCRxxxxH42	35.15	34.28
DCRxxxxH52	35.27	34.4
DCR4420H65	35.3	34.7
DCR4660H65	35.3	34.7
DCR3640H85	**35.65**	**35.05**
DCR3980H85	35.65	35.05



Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code:H

Fig.16 Package outline

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