



# **Phase Control Thyristor**



DS5965-3 August 2014 (LN31843)

#### **FEATURES**

- Double Side Cooling
- High Surge Capability

### **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

#### **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR1110F52* DCR1110F50	5200 5000	$\begin{split} T_{vj} = -40^{\circ}\text{C to } 125^{\circ}\text{C}, \\ I_{DRM} = I_{RRM} = 100\text{mA}, \\ V_{DRM}, V_{RRM}  t_p = 10\text{ms}, \\ V_{DSM}  \&  V_{RSM} = \\ V_{DRM}  \&  V_{RRM} + 100V \\ respectively \end{split}$

Lower voltage grades available. \*5000V @ -40°C, 5200V @ 0°C

#### **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

#### DCR1110F52

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

### **KEY PARAMETERS**

$V_{DRM}$	5200V
$I_{T(AV)}$	1107A
I <sub>TSM</sub>	14800A
dV/dt*	1500V/µs
dI/dt	800A/μs

\* Higher dV/dt selections available

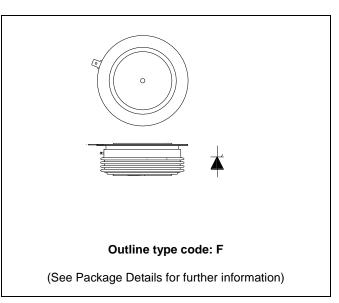


Fig. 1 Package outline





### **CURRENT RATINGS**

### $T_{\text{case}}$ = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	1107	Α
I <sub>T(RMS)</sub>	RMS value -		1739	А
I <sub>T</sub>	Continuous (direct) on-state current	-	1684	А

### **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	14.8	kA
l <sup>2</sup> t	I <sup>2</sup> t for fusing	$V_R = 0$	1.097	MA <sup>2</sup> s

### THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.0184	°C/W
		Single side cooled	Anode DC	-	0.0333	°C/W
			Cathode DC	-	0.0418	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 23kN Double side		-	0.004	°C/W
		(with mounting compound)	Single side	-	0.008	°C/W
T <sub>vj</sub>	Virtual junction temperature	Blocking V <sub>DRM</sub> / <sub>VRRM</sub>		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
F <sub>m</sub>	Clamping force			20.0	25.0	kN





## **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditio	Test Conditions		Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	100	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% $V_{DRM}$ , $T_j = 125$ °C, ga	ate open	-	1500	V/µs
dl/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub>	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	800	A/µs
		$t_r < 0.5 \mu s, T_j = 125 ^{\circ} C$				
V <sub>T(TO)</sub>	Threshold voltage – Low level	300A to 750A at T <sub>case</sub> = 125°	С	-	0.948	V
	Threshold voltage – High level	750A to 4000A at T <sub>case</sub> = 125	5°C	-	1.078	V
r <sub>T</sub>	On-state slope resistance – Low level	300A to 750A at T <sub>case</sub> = 125°C		-	0.783	mΩ
	On-state slope resistance – High level	750A to 4000A at T <sub>case</sub> = 125°C		-	0.610	mΩ
t <sub>gd</sub>	Delay time	$V_D$ = 67% $V_{DRM}$ , gate source 30V, $10\Omega$		-	3	μs
	,	$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$T_j = 125$ °C, $V_R = 100$ V, $dI/dt = 5$ A/ $\mu$ s,		-	1000	μs
		dV <sub>DR</sub> /dt = 20V/μs linear to 2000V				
Qs	Stored charge	$I_T = 1000A$ , $tp = 1000us$ , $T_i = 125$ °C,		2200	3800	μC
I <sub>RR</sub>	Reverse recovery current	dI/dt =5A/μs,		90	115	Α
IL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	А
I <sub>H</sub>	Holding current	$T_j = 25^{\circ}C, R_{G-K} = \infty, I_{TM} = 500$	0A, I <sub>T</sub> = 5A	-	300	mA





#### **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
$V_{GD}$	Gate non-trigger voltage	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	0.4	V
I <sub>GT</sub>	Gate trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	350	mA
I <sub>GD</sub>	Gate non-trigger current	At 50% V <sub>DRM</sub> , T <sub>case</sub> = 125°C	10	mA

#### **CURVES**

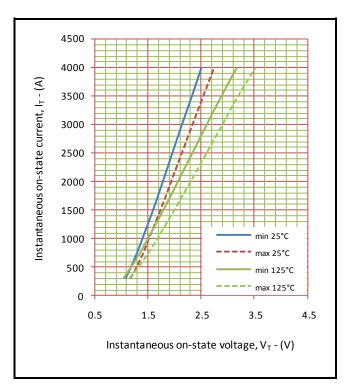


Fig.2 Maximum & minimum on-state characteristics

 $V_{\text{TM}}$  EQUATION

Where A = -0.069834B = 0.220863

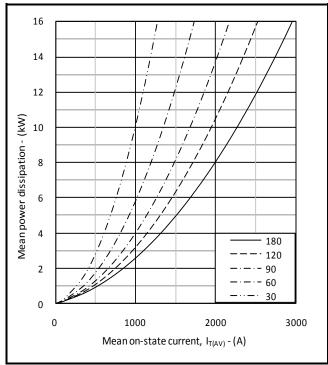
 $V_{TM} = A + BIn (I_T) + C.I_T + D.\sqrt{I_T}$ 

C = 0.000638

D = -0.013352

these values are valid for  $T_j$  = 125°C for  $I_T$  300A to 4000A





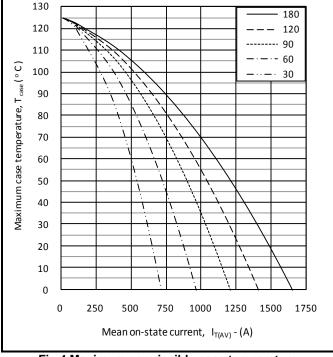
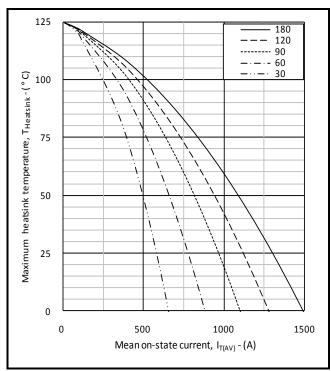
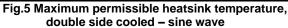


Fig.3 On-state power dissipation - sine wave

Fig.4 Maximum permissible case temperature, double side cooled – sine wave





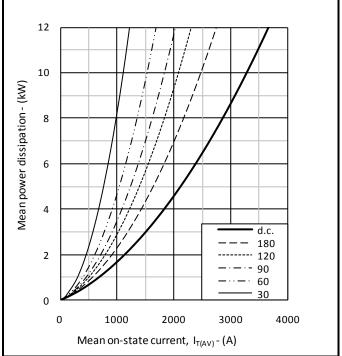


Fig.6 On-state power dissipation - rectangular wave



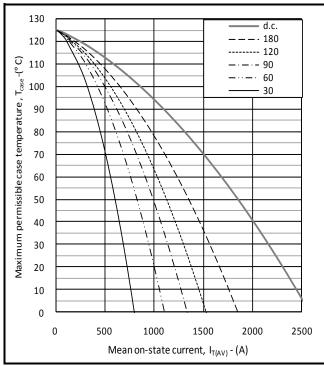


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

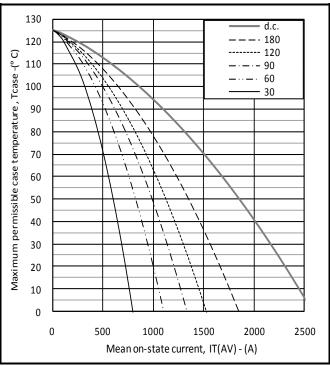
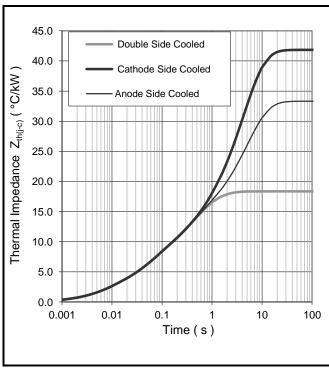


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	7.5608	4.0772	3.8420	2.8671
	T <sub>i</sub> (s)	0.6877	0.2537	0.0614	0.0101
Anode side cooled	R <sub>i</sub> (°C/kW)	6.7211	4.6219	15.5387	14.8631
	T <sub>i</sub> (s)	0.1910	0.0158	5.0011	3.3169
Cathode side cooled	R <sub>i</sub> (°C/kW)	11.5564	8.5810	4.7942	8.3643
	T: (s)	4 2216	6.0269	0.0166	0.2255

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

#### $\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance  $R_{th(j\cdot c)}$  when the device operates at conduction angles other than d.c.

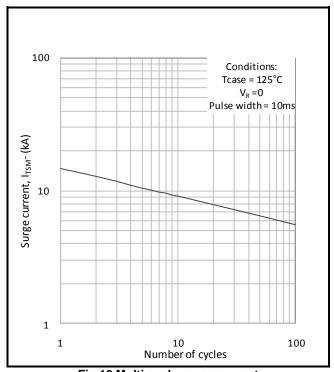
	Double side cooling				
	$\Delta Z_{th}(z)$				
θ°	sine. rect.				
180	3.19	2.14			
120	3.72	3.10			
90	4.29	3.64			
60	4.81	4.23			
30	5.22	4.88			
15	5.40	5.22			

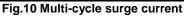
Anode Side Cooling				
	$\Delta Z_{th}(z)$			
θ°	sine.	rect.		
180	2.97	2.03		
120	3.43	2.89		
90	3.92	3.36		
60	4.36	3.87		
30	4.69	4.41		
15	181	4.70		

Č	Cathode Sided Cooling			
	$\Delta Z_{th}(z)$			
θ°	sine.	rect.		
180	2.95	2.02		
120	3.40	2.87		
90	3.88	3.34		
60	4.31	3.84		
30	4.64	4.37		
15	4.79	4.65		

Fig.9 Maximum (limit) transient thermal impedance - junction to case (°C/kW)







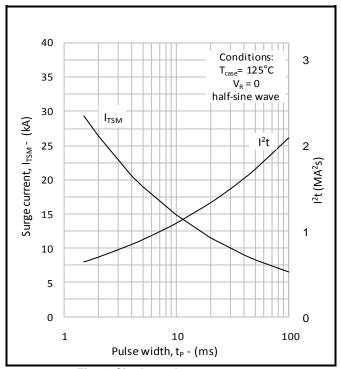


Fig.11 Single-cycle surge current

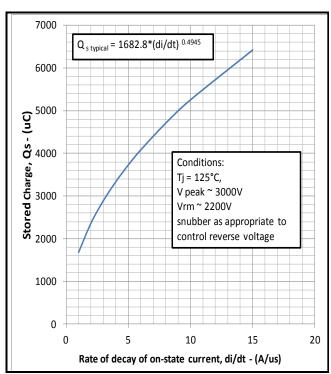


Fig.12 Stored charge vs di/dt

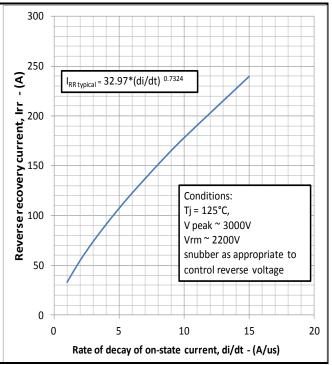


Fig.13 Reverse recovery current vs di/dt

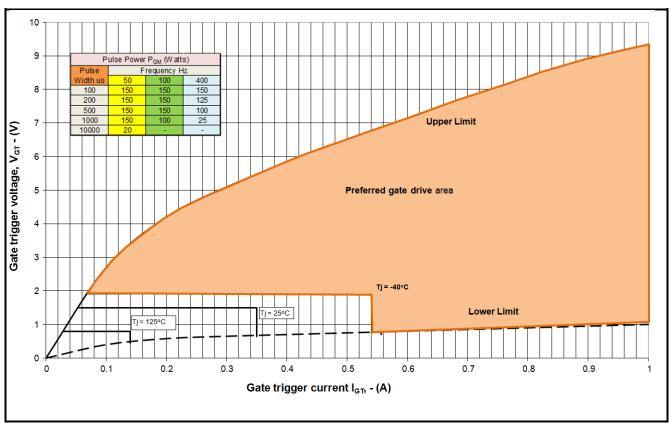


Fig14 Gate Characteristics

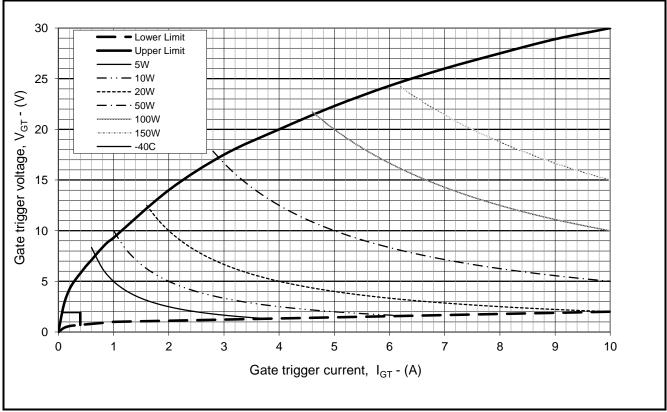


Fig. 15 Gate characteristics





#### PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

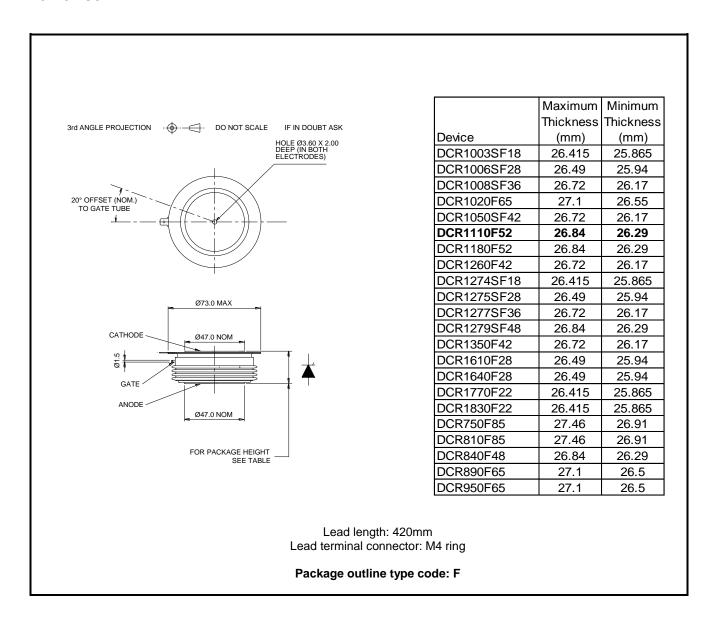


Fig.16 Package outline





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