



# **Phase Control Thyristor**

DS5810-3 January 2014 (LN31245)

## **FEATURES**

- Double Side Cooling
- High Surge Capability

## **APPLICATIONS**

- High Power Drives
- High Voltage Power Supplies
- Static Switches

## **VOLTAGE RATINGS**

Part and Ordering Number	Repetitive Peak Voltages V <sub>DRM</sub> and V <sub>RRM</sub> V	Conditions
DCR3030V42 DCR3030V40 DCR3030V35 DCR3030V30	4200 4000 3500 3000	$\begin{split} T_{vj} &= \text{-}40^{\circ}\text{C to 125}^{\circ}\text{C}, \\ I_{DRM} &= I_{RRM} = 200\text{mA}, \\ V_{DRM}, V_{RRM}  t_p &= 10\text{ms}, \\ V_{DSM}  \&  V_{RSM} &= \\ V_{DRM}  \&  V_{RRM}  + 100V \\ respectively \end{split}$

Lower voltage grades available.

## **ORDERING INFORMATION**

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

## DCR3030V42

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

## **KEY PARAMETERS**

4200V
3030A
40600A
1500V/µs
400A/μs

\* Higher dV/dt selections available

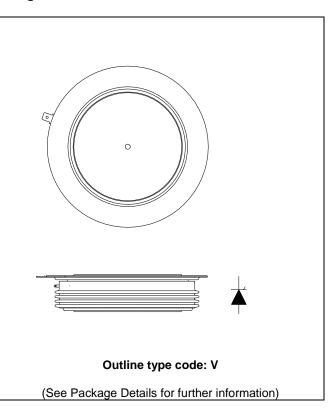


Fig. 1 Package outline





# **CURRENT RATINGS**

# $T_{\text{case}}$ = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Si	de Cooled			
I <sub>T(AV)</sub>	Mean on-state current	Half wave resistive load	3030	А
I <sub>T(RMS)</sub>	RMS value	-	4760	А
Ι <sub>Τ</sub>	Continuous (direct) on-state current	-	4550	А

# **SURGE RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
I <sub>TSM</sub>	Surge (non-repetitive) on-state current	10ms half sine, T <sub>case</sub> = 125°C	40.6	kA
I <sup>2</sup> t I <sup>2</sup> t for fusing		$V_R = 0$	8.24	MA <sup>2</sup> s

# THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R <sub>th(j-c)</sub>	Thermal resistance – junction to case	Double side cooled	DC	-	0.00746	°C/W
		Single side cooled	Anode DC	-	0.0130	°C/W
			Cathode DC	-	0.0178	°C/W
R <sub>th(c-h)</sub>	Thermal resistance – case to heatsink	Clamping force 54kN	Double side	-	0.002	°C/W
		(with mounting compound)	Single side	-	0.004	°C/W
T <sub>vj</sub>	Virtual junction temperature	Blocking V <sub>DRM</sub> / <sub>VRRM</sub>		-	125	°C
T <sub>stg</sub>	Storage temperature range			-55	125	°C
Fm	Clamping force			48.0	59.0	kN





# **DYNAMIC CHARACTERISTICS**

Symbol	Parameter	Test Conditio	Test Conditions		Max.	Units
I <sub>RRM</sub> /I <sub>DRM</sub>	Peak reverse and off-state current	At V <sub>RRM</sub> /V <sub>DRM</sub> , T <sub>case</sub> = 125°C		-	200	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V <sub>DRM</sub> , T <sub>j</sub> = 125°C, ga	ate open	-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V <sub>DRM</sub> to 2x I <sub>T(AV)</sub>	Repetitive 50Hz	-	200	A/µs
		Gate source 30V, 10Ω,	Non-repetitive	-	400	A/µs
		$t_r < 0.5 \mu s, T_j = 125$ °C				
$V_{T(TO)}$	Threshold voltage – Low level	200A to 1700A at T <sub>case</sub> = 125	5°C	-	0.82	>
	Threshold voltage – High level	1700A to 7000A at T <sub>case</sub> = 12	25°C	-	0.98	٧
r <sub>T</sub>	On-state slope resistance – Low level	200A to 1700A at T <sub>case</sub> = 125°C		-	0.292	mΩ
	On-state slope resistance – High level	1700A to 7000A at T <sub>case</sub> = 125°C		-	0.198	mΩ
t <sub>gd</sub>	Delay time	$V_D = 67\% V_{DRM}$ , gate source 30V, $10\Omega$		TBD	TBD	μs
		$t_r = 0.5 \mu s, T_j = 25^{\circ}C$				
tq	Turn-off time	$T_j = 125$ °C, $V_R = 200$ V, $dI/dt = 1$ A/ $\mu$ s,		250	500	μs
		dV <sub>DR</sub> /dt = 20V/μs linear				
Qs	Stored charge	$T_j = 125$ °C, dl/dt – 1A/ $\mu$ s, $V_{R pk} = 3000$ V, $V_{RM} = 1700$ V		1600	3500	μC
IL	Latching current	$T_j = 25^{\circ}C, V_D = 5V$		-	3	А
lн	Holding current	$T_j = 25^{\circ}\text{C}, R_{G-K} = \infty, I_{TM} = 50^{\circ}$	0A, I <sub>T</sub> = 5A	-	300	mA





## **GATE TRIGGER CHARACTERISTICS AND RATINGS**

Symbol	Parameter	Test Conditions	Max.	Units
$V_{GT}$	Gate trigger voltage	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	1.5	V
$V_{GD}$	Gate non-trigger voltage	At V <sub>DRM</sub> , T <sub>case</sub> = 125°C	TBD	V
I <sub>GT</sub>	Gate trigger current	$V_{DRM} = 5V$ , $T_{case} = 25$ °C	350	mA
I <sub>GD</sub>	Gate non-trigger current	V <sub>DRM</sub> = 5V, T <sub>case</sub> = 25°C	TBD	mA

# **CURVES**

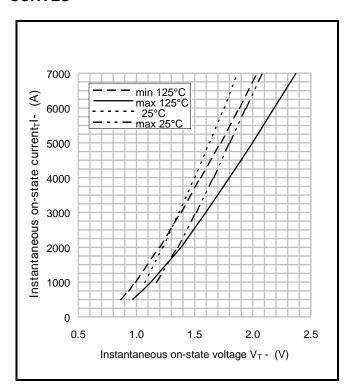


Fig.2 Maximum & minimum on-state characteristics

 $V_{TM}$  EQUATION Where A = 0.866995 B = -0.042053

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$  C = 0.000100

D = 0.014062

these values are valid for  $T_j$  = 125°C for  $I_T$  500A to 10000A



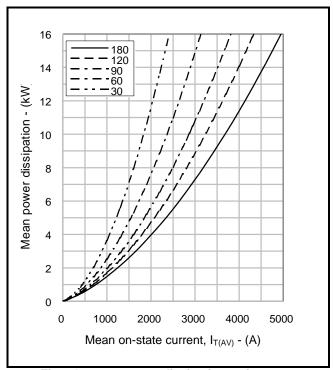


Fig.3 On-state power dissipation – sine wave

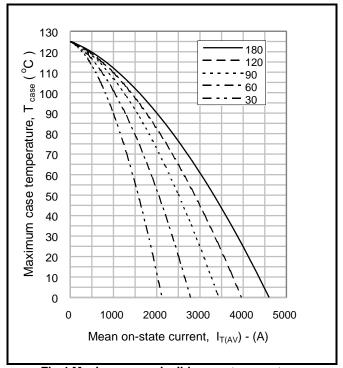


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

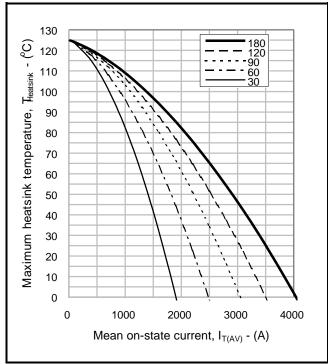


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

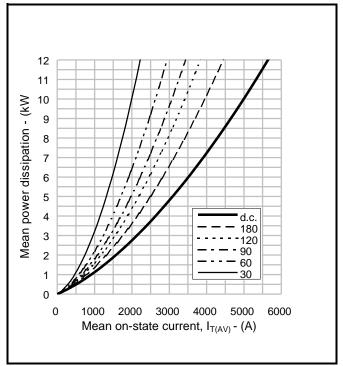
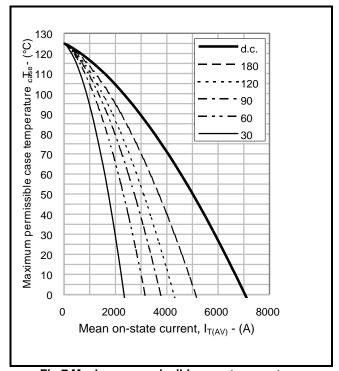
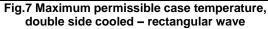


Fig.6 On-state power dissipation - rectangular wave







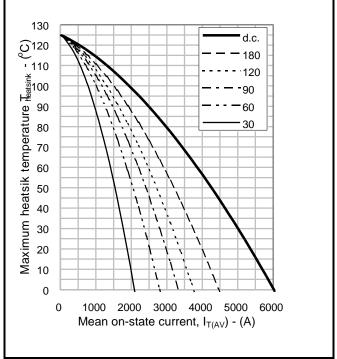
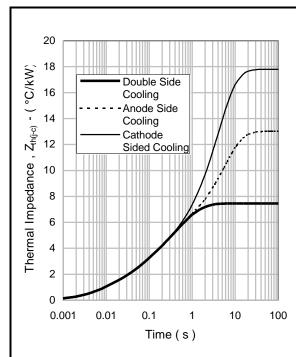


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R <sub>i</sub> (°C/kW)	0.9206	1.8299	3.4022	1.3044
	T <sub>i</sub> (s)	0.0076807	0.0579454	0.4078613	1.2085
Anode side cooled	R <sub>i</sub> (°C/kW)	0.9032	1.6719	3.0101	7.4269
	T <sub>i</sub> (s)	0.0075871	0.0536531	0.3144537	5.624
Cathode side cooled	R <sub>i</sub> (°C/kW)	0.9478	2.0661	1.6884	13.0847
	T. (s)	0.0078442	0.0645541	0.3804380	4 1447

 $Z_{th} = \sum [R_i x (1-exp. (t/t_i))]$  [1]

 $\Delta R_{\text{th(j-c)}}$  Conduction

Tables show the increments of thermal resistance  $R_{\text{th(j-c)}}$  when the device operates at conduction angles other than d.c.

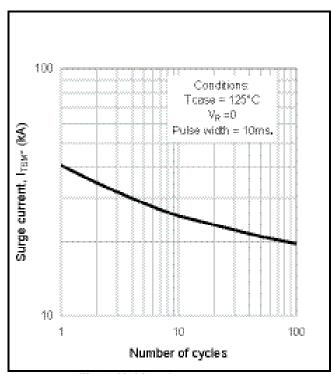
Double side cooling					
	$\Delta Z_{th}(z)$				
θ°	sine.	rect.			
180	1.34	0.88			
120	1.57	1.30			
90	1.83	1.54			
60	2.08	1.81			
30	2.27	2.11			
4.5		0.00			

	Anode Side i	Cooling	
	$\Delta Z_{th}(z)$		
θ°	sine.	rect.	
180	1.34	0.88	
120	1.57	1.30	
90	1.84	1.54	
60	2.08	1.81	
30	2.28	2.11	
4.5	0.07	0.00	

Ca	thode Sided Cooling		
	$\Delta Z_{th}$ (z)		
θ°	sine.	rect.	
180	1.33	0.88	
120	1.57	1.29	
90	1.83	1.53	
60	2.07	1.80	
30	2.26	2.10	
4.5		0.00	

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)





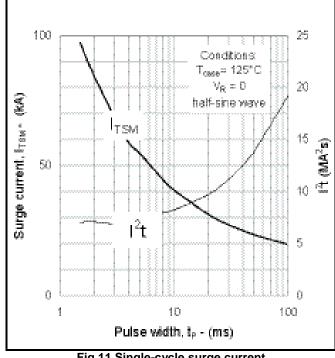
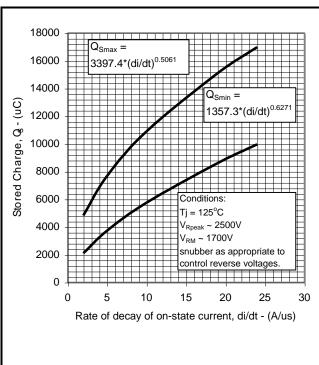


Fig.10 Multi-cycle surge current

Fig.11 Single-cycle surge current



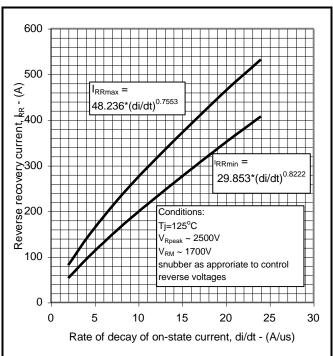


Fig. 12 Stored Charge

Fig. 13 Reverse Recovery Current

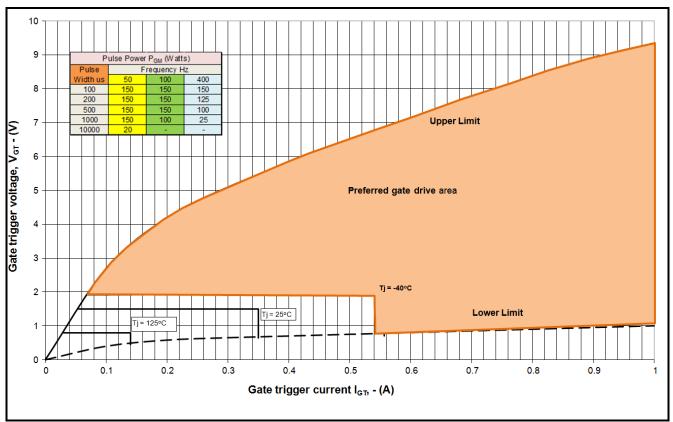


Fig14 Gate Characteristics

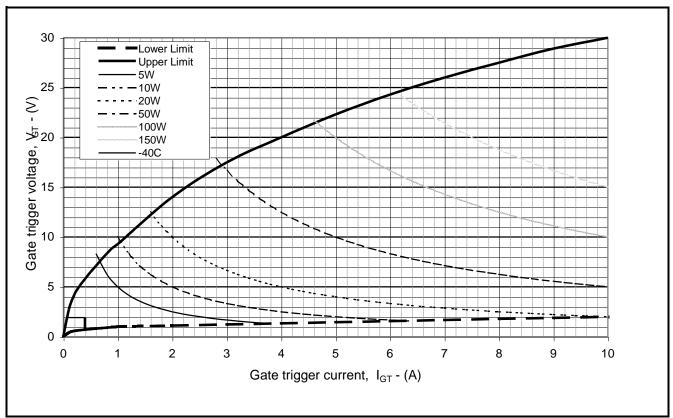


Fig. 15 Gate characteristics





#### **PACKAGE DETAILS**

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

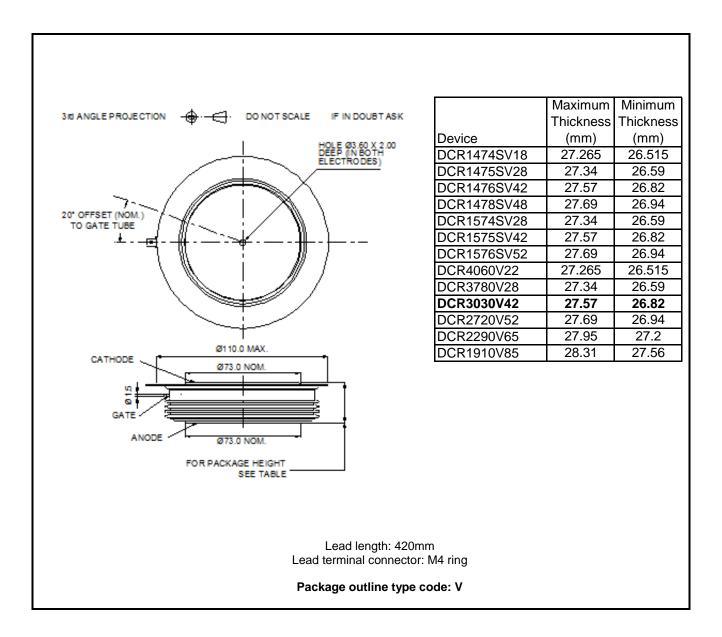


Fig.16 Package outline





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