

DCR780G30

Phase Control Thyristor

DS6045-1 April 2011 (LN28256)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR780G30 DCR780G28 DCR780G26 DCR780G24	3000 2800 2600 2400	$\begin{array}{l} T_{v_j} = -40^{\circ}C \ to \ 125^{\circ}C, \\ I_{DRM} = I_{RRM} = 60mA, \\ V_{DRM}, \ V_{RRM} \ t_p = 10ms, \\ V_{DSM} \& \ V_{RSM} = \\ V_{DRM} \& \ V_{RRM} \ +100V \\ respectively \end{array}$

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR780G30

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V _{DRM}	3000 V
I _{T(AV)}	780 A
I _{TSM}	10500 A
dV/dt*	1000 V/µs
dl/dt	200 A/µs

* Higher dV/dt selections available

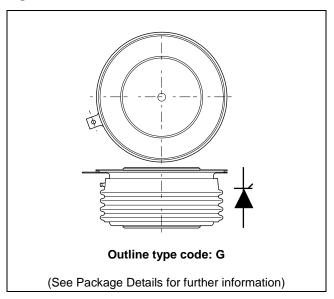


Fig. 1 Package outline



CURRENT RATINGS

 $T_{case} = 60^{\circ}C$ unless stated otherwise

Symbol	Parameter	Test Conditions		Units	
Double Si	Double Side Cooled				
I _{T(AV)}	Mean on-state current	Half wave resistive load	780	А	
I _{T(RMS)}	RMS value	-	1220	А	
Ι _Τ	Continuous (direct) on-state current	-	1100	А	

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I _{TSM}	Surge (non-repetitive) on-state current	ent 10ms half sine, $T_{case} = 125^{\circ}C$		kA
l ² t	I ² t for fusing	$V_R = 0$	0.551	MA ² s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	DC	-	0.035	°C/W
R _{th(c-h)}	Thermal resistance – case to heatsink	Double side cooled	DC	-	0.008	°C/W
T_{vj}	Virtual junction temperature	Blocking V _{DRM} / _{VRRM}		-	125	°C
T _{stg}	Storage temperature range			-40	140	°C
F _m	Clamping force			12	18	kN



DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125°C		-	60	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM} , $T_j = 125$ °C, gate open		1000	-	V/µs
dl/dt	Rate of rise of on-state current	From 67% V _{DRM} to 1000A Repetitive 50Hz		-	200	A/µs
		Gate source 30V, 10Ω ,	Non-repetitive	-	1000	A/µs
		t _r < 0.5µs, T _j = 125°C				
V _T	On-state voltage	I _T = 1500A, T _{case} = 125°C			1.90	V
V _{T(TO)}	Threshold voltage – Low level	T _{case} = 125°C		-	1.00	V
r _T	On-state slope resistance – Low level	T _{case} = 125°C		-	0.60	mΩ
t _{gd}	Delay time	V_D = 67% V_{DRM} , gate source 30V, 10 Ω t_r = 0.5µs, T_j = 25°C		-	3.0	μs
tq	Turn-off time	$T_{j} = 125^{\circ}C, V_{R} = 100V, dl/dt = 10A/\mu s,$ $dV_{DR}/dt = 20V/\mu s \text{ linear to } 67\% V_{DRM}$			400	μs
				-		
Qs	Stored charge	I _T = 1000A, tp = 1000us,T _j = 125°C, dl/dt =10A/μs,		-	2400	μC
I _{RR}	Reverse recovery current			-	125	А
١L	Latching current	T _j = 25°C,		-	1	А
I _H	Holding current	T _j = 25°C,		-	200	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V _{GT}	Gate trigger voltage	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	3	V
V _{GD}	Gate non-trigger voltage	At 40% V _{DRM} , T _{case} = 125°C	TBD	V
I _{GT}	Gate trigger current	$V_{DRM} = 5V, T_{case} = 25^{\circ}C$	300	mA
I _{GD}	Gate non-trigger current	At 40% V _{DRM} , T _{case} = 125°C	TBD	mA



CURVES

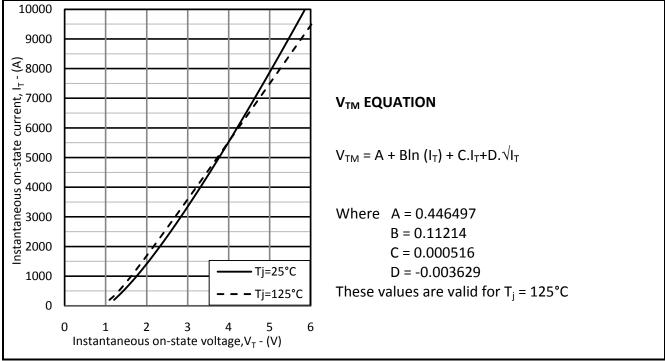


Fig.2 Maximum & minimum on-state characteristics

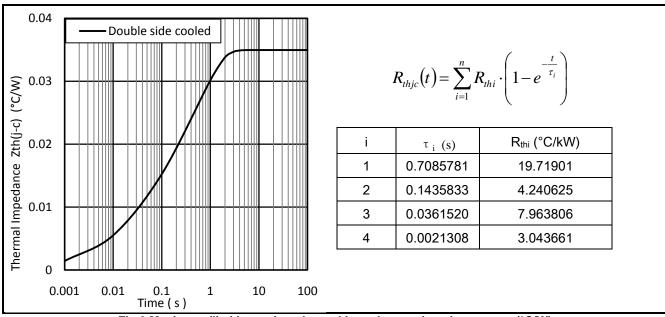
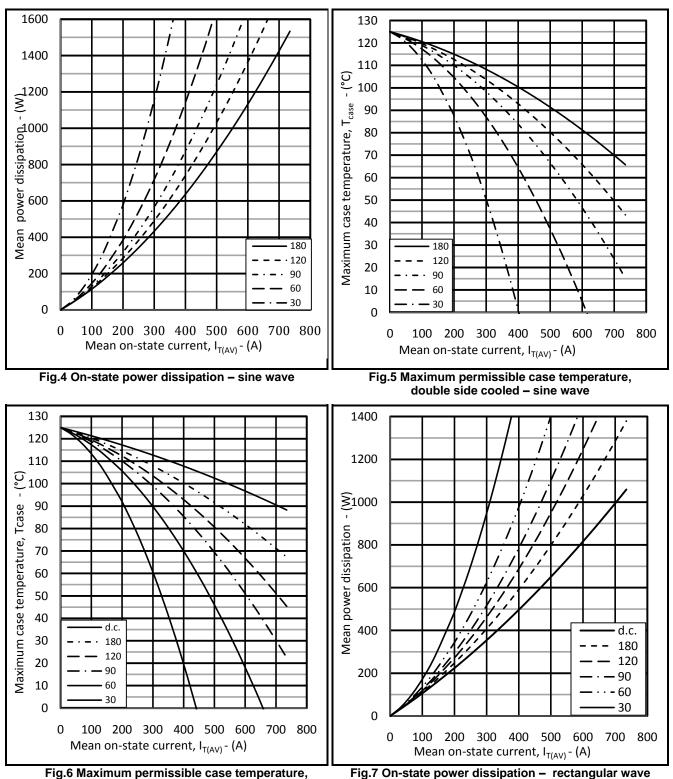


Fig.3 Maximum (limit) transient thermal impedance – junction to case (°C/W)





double side cooled - rectangular wave





DCR780G30

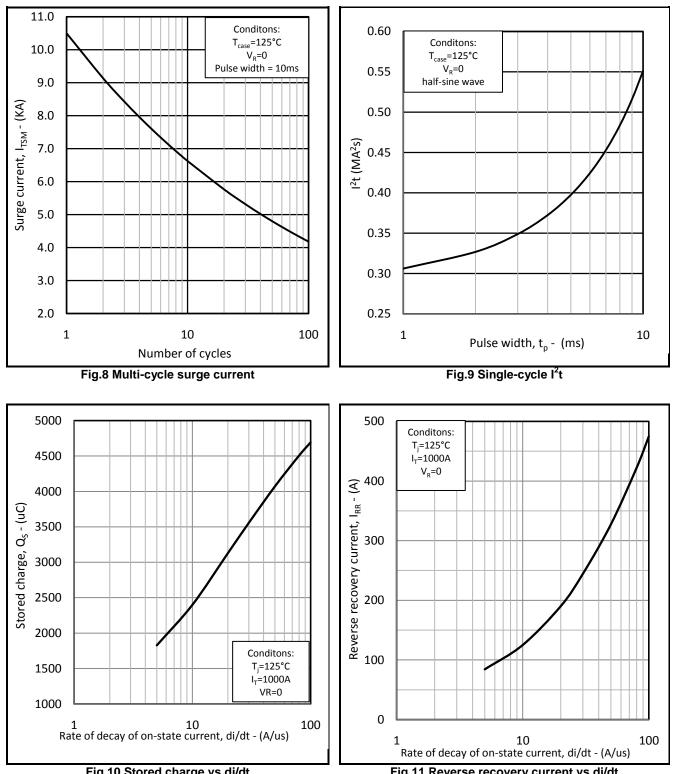


Fig.10 Stored charge vs di/dt

Fig.11 Reverse recovery current vs di/dt



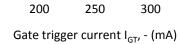


Fig.12 Gate characteristics

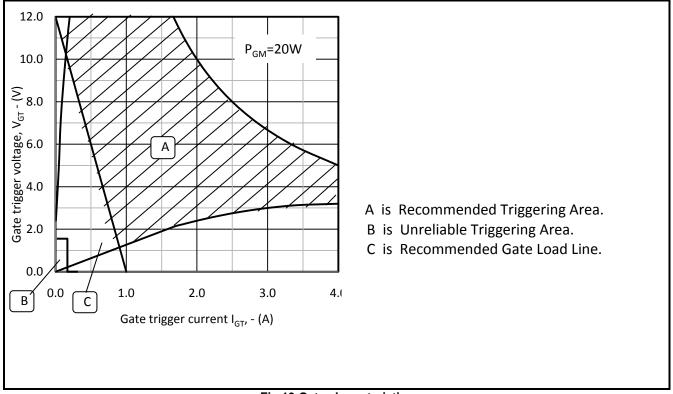


Fig.13 Gate characteristics



PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

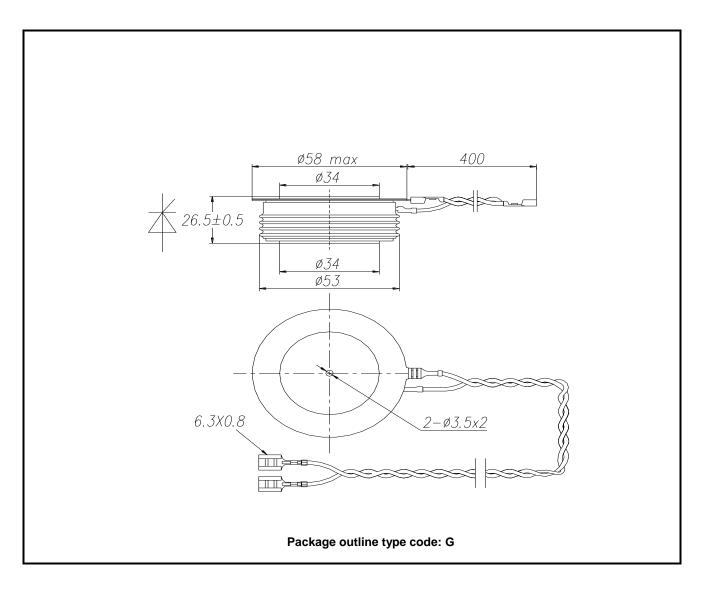


Fig.14 Package outline



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