DCR5900A28

Phase Control Thyristor

DS6151-2 September 2014 (LN 31946)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V_{DRM} and V_{RRM} V	Conditions
DCR5900A28 DCR5900A26 DCR5900A24	2800 2600 2400	T_{vj} = -40°C to 125°C, I_{DRM} = I_{RRM} = 300mA, V_{DRM}, V_{RRM} t_p = 10ms, V_{DSM} & V_{RSM} = V_{DRM} & V_{RRM} + 100V respectively

Lower voltage grades available.

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR5900A26

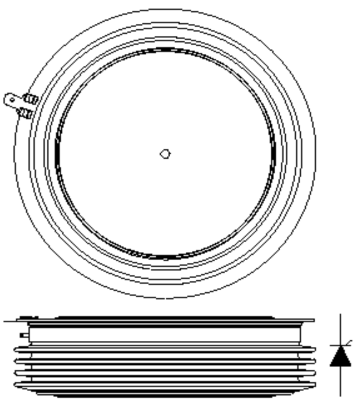
Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

j

KEY PARAMETERS

V_{DRM}	**2800V**
$I_{T(AV)}$	**5900A**
I_{TSM}	**79000A**
dV/dt*	**2000V/µs**
dI/dt	**250A/µs**

*** Higher dV/dt selections available**



Outline type code: A

(See Package Details for further information)

Fig. 1 Package outline

CURRENT RATINGS

T_{case} = 60°C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Side Cooled				
$I_{T(AV)}$	Mean on-state current	Half wave resistive load	5900	A
$I_{T(RMS)}$	RMS value	-	9277	A
I_T	Continuous (direct) on-state current	-	7715	A

SURGE RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
I_{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T_{case} = 125°C	79.0	kA
I^2t	I^2t for fusing	V_R = 0	31.2	MA^2s

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
$R_{th(j-c)}$	Thermal resistance – junction to case	Double side cooled	DC	-	0.00603	°C/W
		Single side cooled	Anode DC	-	0.01024	°C/W
			Cathode DC	-	0.01467	°C/W
$R_{th(c-h)}$	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	°C/W
		(with mounting compound)	Single side	-	0.002	°C/W
T_{vj}	Virtual junction temperature	Blocking V_{DRM} / V_{RRM}		-	125	°C
T_{stg}	Storage temperature range			-55	125	°C
F_m	Clamping force			74.0	91.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditions		Min.	Max.	Units
I_{RRM}/I_{DRM}	Peak reverse and off-state current	At V_{RRM}/V_{DRM}, T_{case} = 125°C		-	300	mA
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V_{DRM}, T_j = 125°C, gate open		-	2000	V/µs
dI/dt	Rate of rise of on-state current	From 67% V_{DRM} to 2x $I_{T(AV)}$	Repetitive 50Hz	-	250	A/µs
		Gate source 30V, 10Ω, t_r < 0.5µs, T_j = 125°C	Non-repetitive	-	500	A/µs
$V_{T(TO)}$	Threshold voltage – Low level	500 to 4000A at T_{case} = 125°C		-	0.766	V
	Threshold voltage – High level	4000 to 8000A at T_{case} = 125°C		-	0.92	V
r_T	On-state slope resistance – Low level	500A to 4000A at T_{case} = 125°C		-	0.1048	mΩ
	On-state slope resistance – High level	4000A to 8000A at T_{case} = 125°C		-	0.06	mΩ
t_{gd}	Delay time	V_D = 67% V_{DRM}, gate source 30V, 10Ω t_r = 0.5µs, T_j = 25°C		-	3	µs
t_q	Turn-off time	I_T = 5000A, T_j = 125°C, V_R = 200V, dI/dt = 5A/µs, dV_{DR}/dt = 20V/µs linear			250	µs
Q_S	Stored charge	I_T = 3000A, T_j = 125°C, dI/dt – 1A/µs, V_{Rpeak} ~1700V, V_R ~ 1100V		1520	3280	µC
I_{RR}	Reverse recovery current			32	56	A
I_L	Latching current	T_j = 25°C, V_D = 5V		-	3	A
I_H	Holding current	T_j = 25°C, R_{G-K} = ∞, I_{TM} = 500A, I_T = 5A		-	300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V_{DRM} = 5V, T_{case} = 25°C	1.5	V
V_{GD}	Gate non-trigger voltage	At 50% V_{DRM}, T_{case} = 125°C	0.4	V
I_{GT}	Gate trigger current	V_{DRM} = 5V, T_{case} = 25°C	300	mA
I_{GD}	Gate non-trigger current	At 50% V_{DRM}, T_{case} = 125°C	10	mA

CURVES

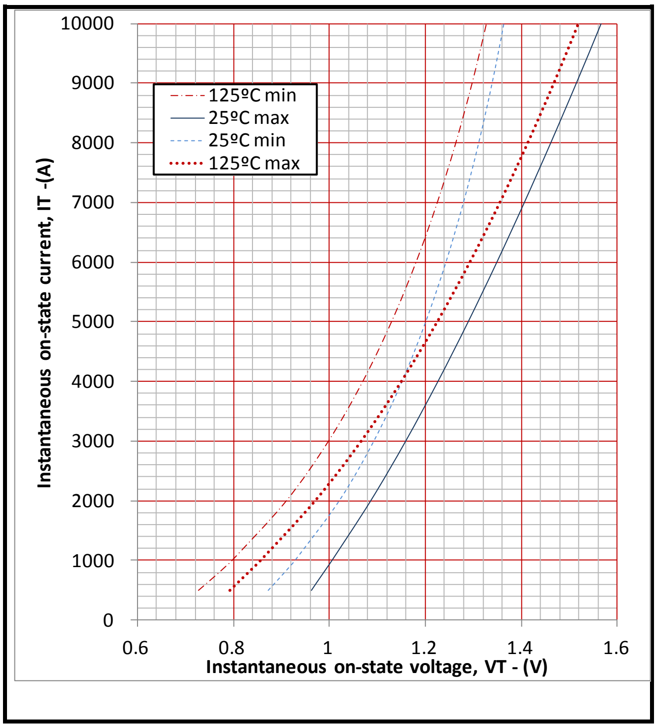


Fig.2 Maximum & minimum on-state characteristics

V_{TM} EQUATION

$V_{TM} = A + B\ln(I_T) + C.I_T + D.\sqrt{I_T}$

Where A = 1.073114
B = -0.098284
C = -0.000016
D = 0.015109

these values are valid for T_j = 125°C for I_T 500A to 8000A

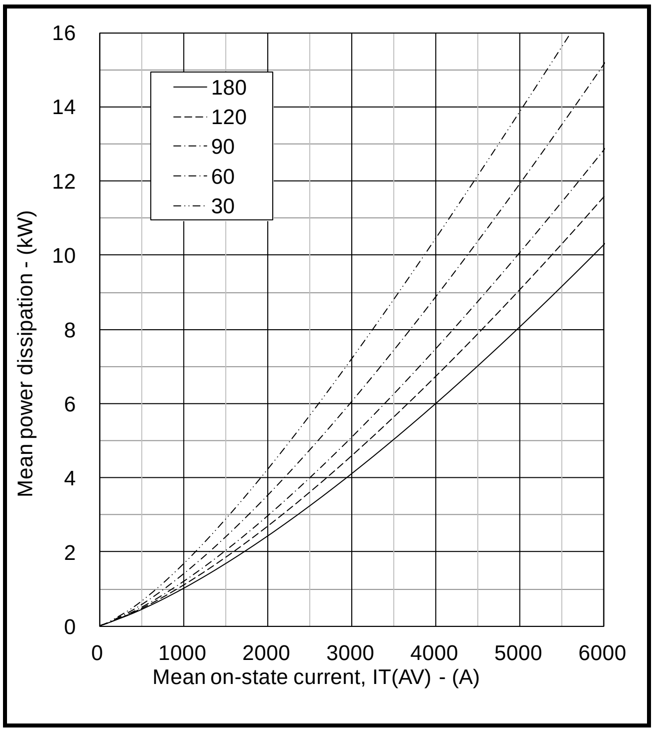


Fig.3 On-state power dissipation – sine wave

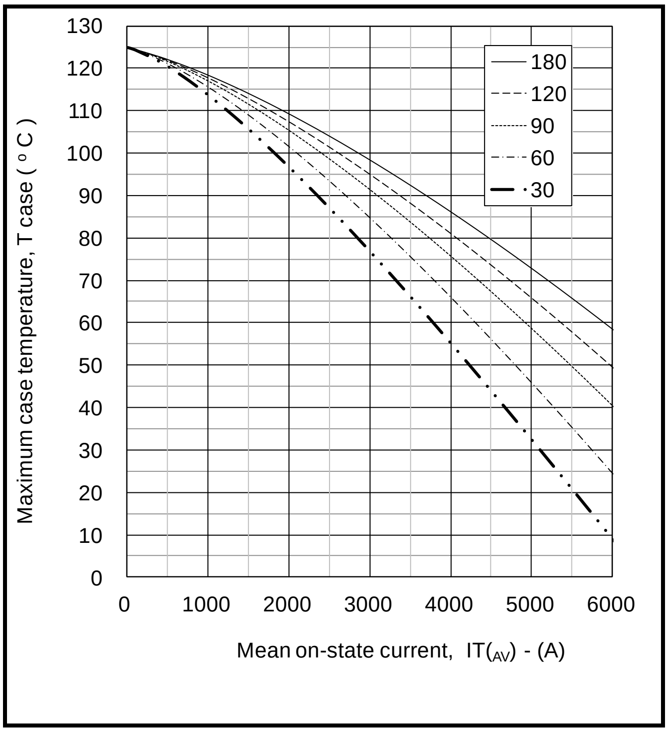


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

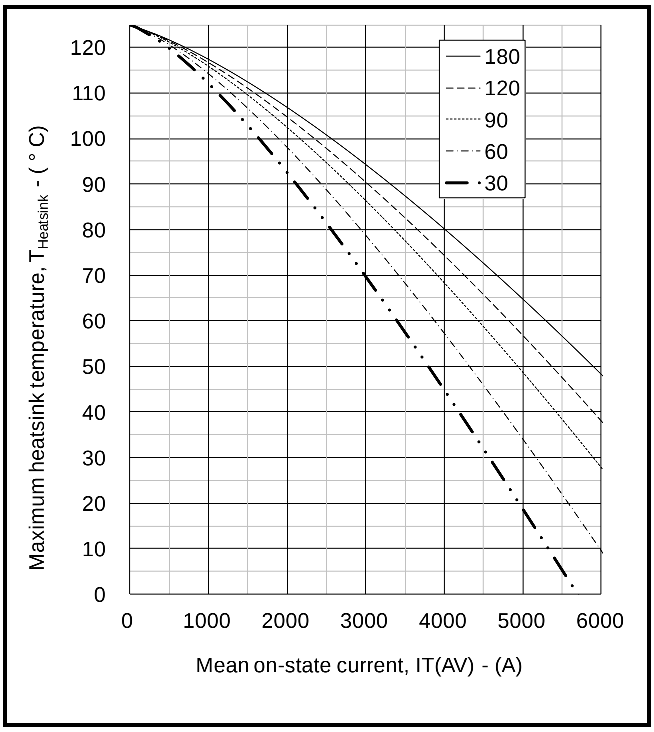


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

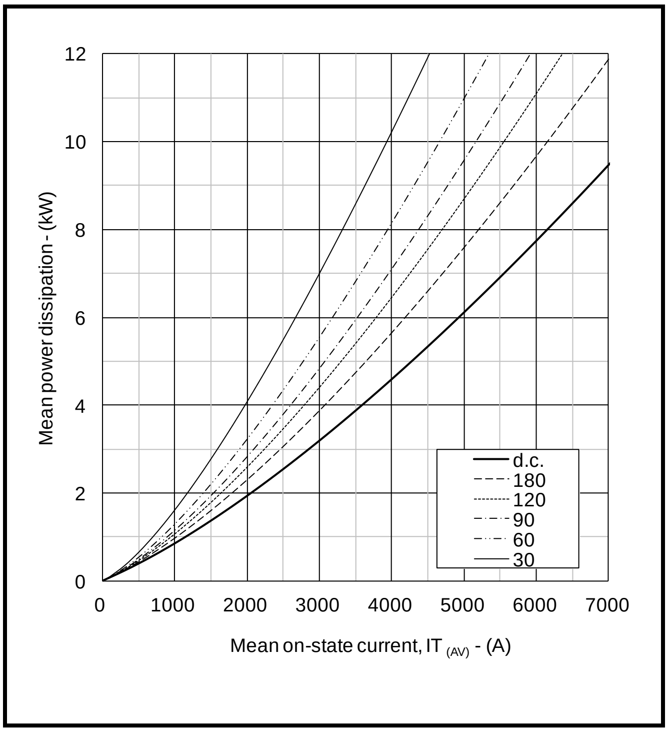


Fig.6 On-state power dissipation – rectangular wave

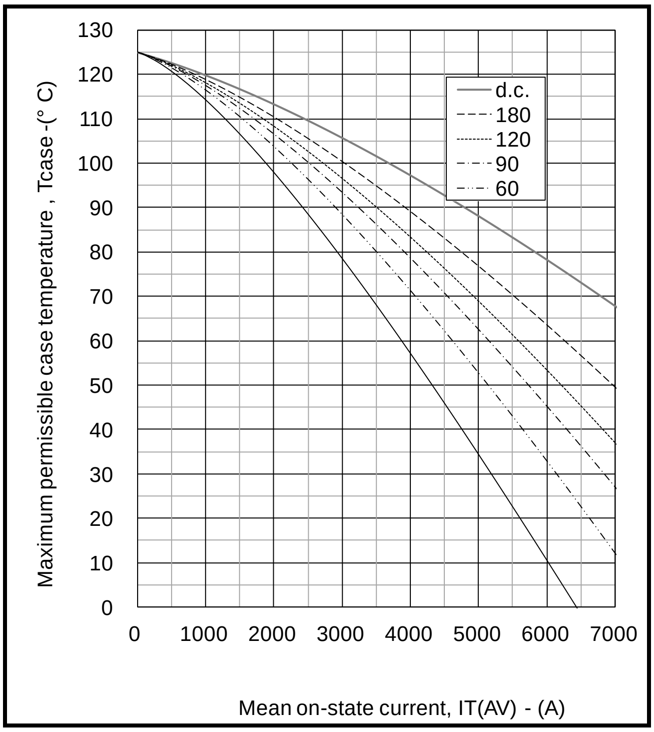


Fig.7 Maximum permissible case temperature, double side cooled – rectangular wave

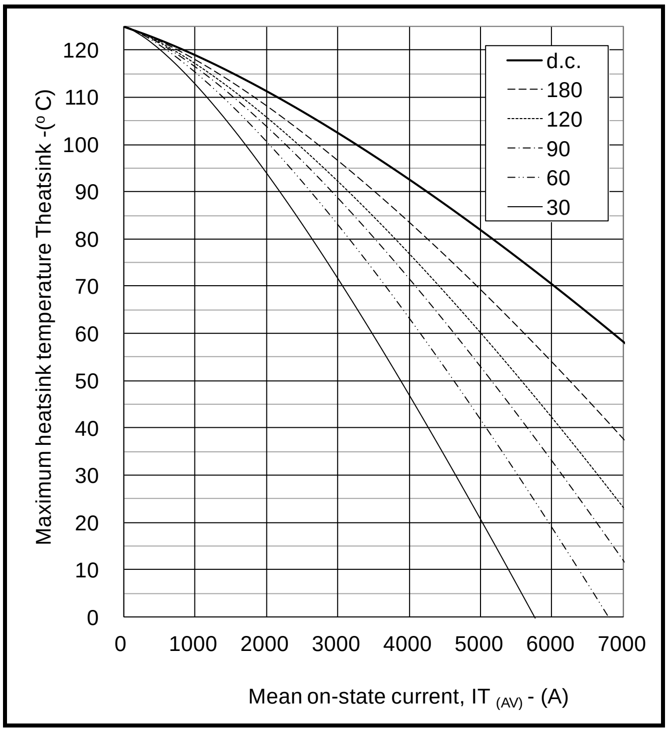
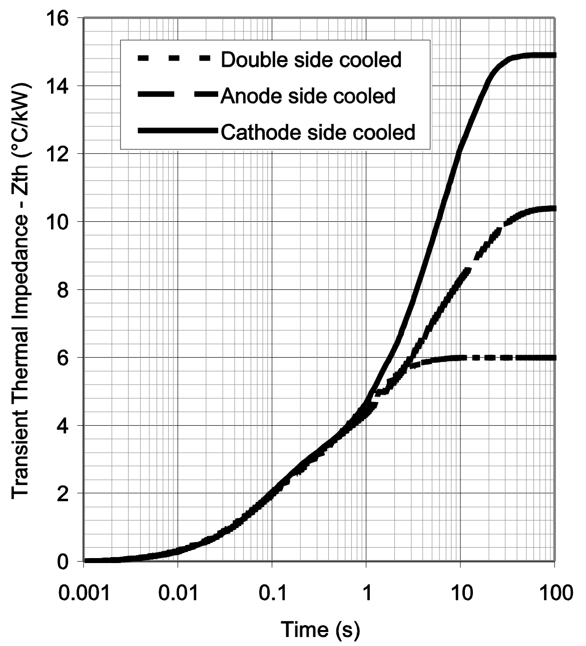


Fig.8 Maximum permissible heatsink temperature, double side cooled – rectangular wave



		1	2	3	4
Double side cooled	R_i (°C/kW)	3.01541	1.048955	0.983519	0.983519
	T_i (s)	0.703874	1.904794	0.059	0.059
Anode side cooled	R_i (°C/kW)	3.156003	4.092806	1.556555	1.623962
	T_i (s)	2.69023	13.79162	0.059	0.205916
Cathode side cooled	R_i (°C/kW)	7.077369	3.483481	1.745839	2.634274
	T_i (s)	6.648601	8.436484	1.762119	0.08069

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T / T_i))]$$

$\Delta R_{th(j-c)}$ Conduction

Tables show the increments of thermal resistance $R_{th(j-c)}$ when the device operates at conduction angles other than d.c.

Double side cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.44	0.31
120	0.49	0.43
90	0.55	0.49
60	0.60	0.55
30	0.64	0.61
15	0.66	0.64

Anode Side Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.42	0.30
120	0.47	0.41
90	0.52	0.46
60	0.57	0.52
30	0.61	0.58
15	0.62	0.61

Cathode Sided Cooling		
	ΔZ_{th} (z)	
θ°	sine.	rect.
180	0.42	0.30
120	0.47	0.41
90	0.52	0.46
60	0.57	0.52
30	0.60	0.58
15	0.62	0.60

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)

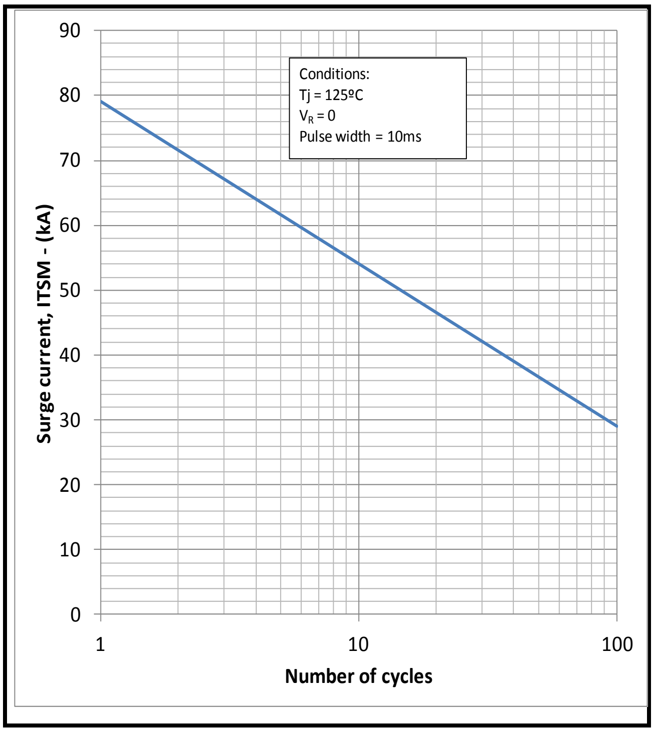


Fig.10 Multi-cycle surge current

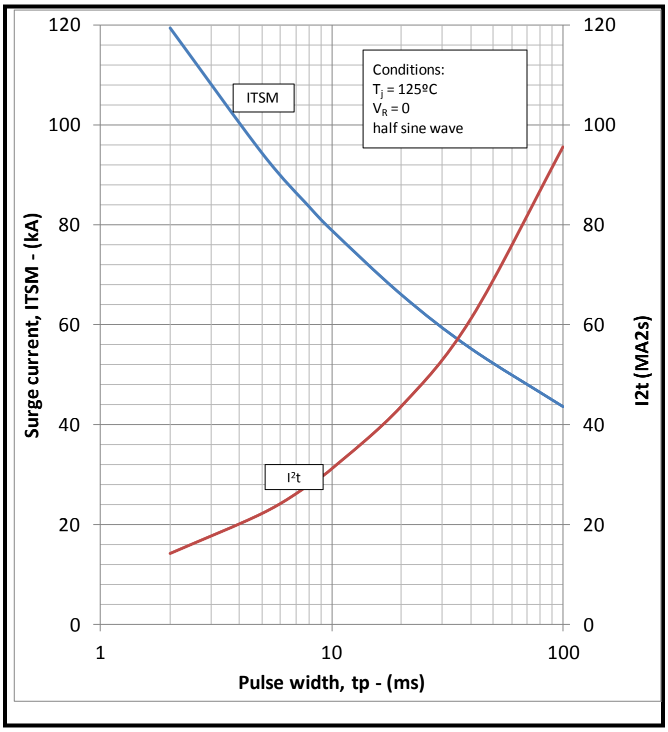


Fig.11 Single-cycle surge current

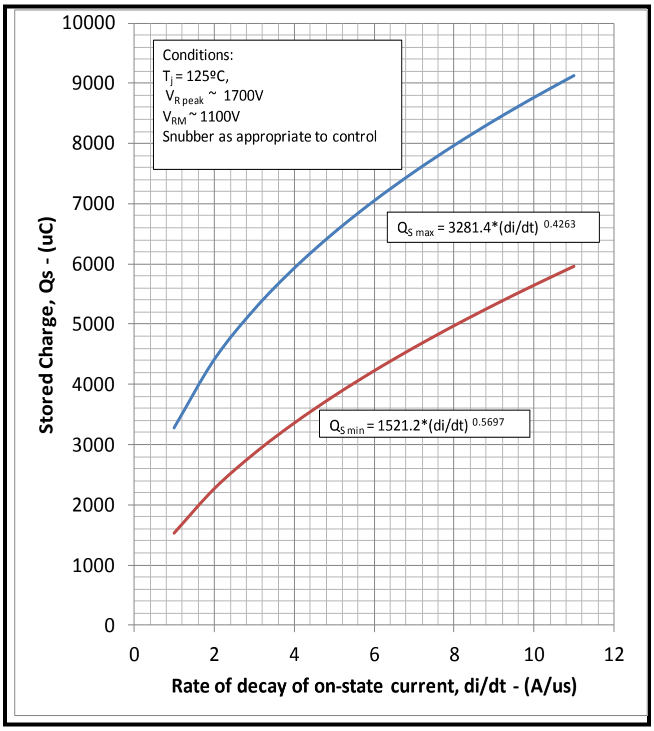


Fig.12 Stored charge

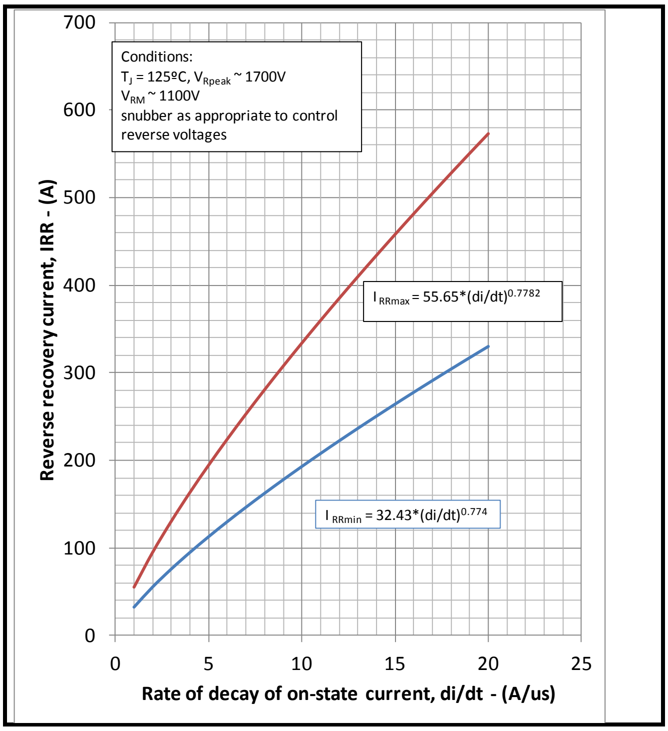


Fig.13 Reverse recovery current

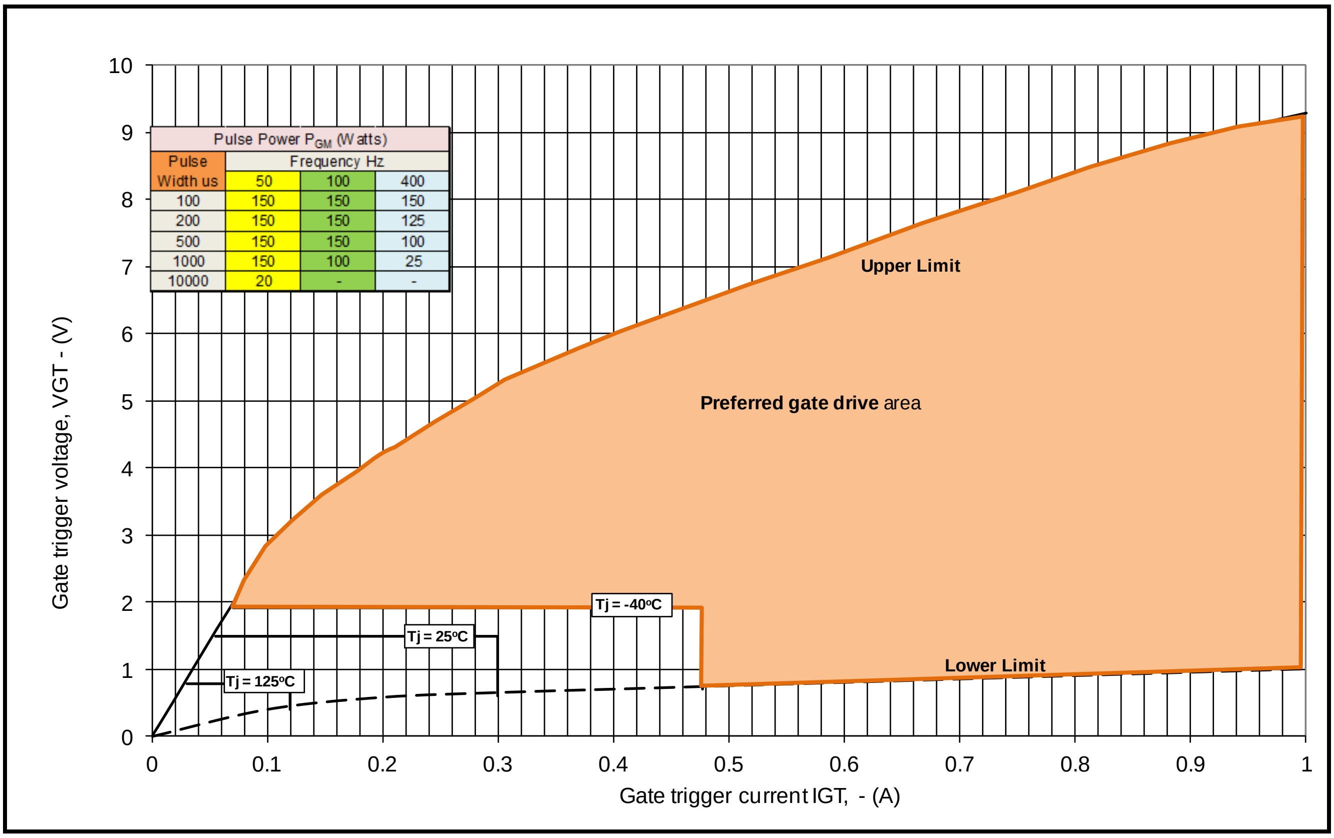


Fig14 Gate Characteristics

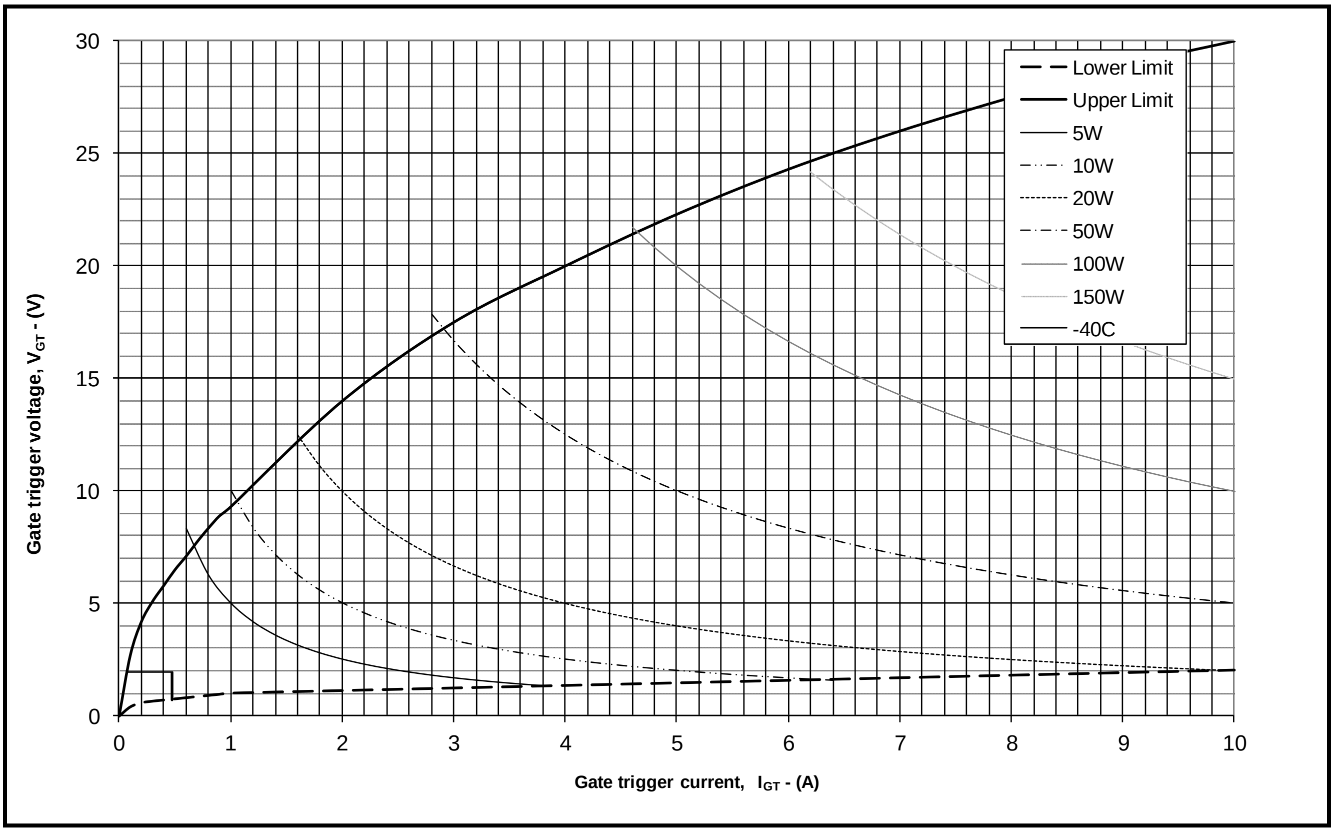
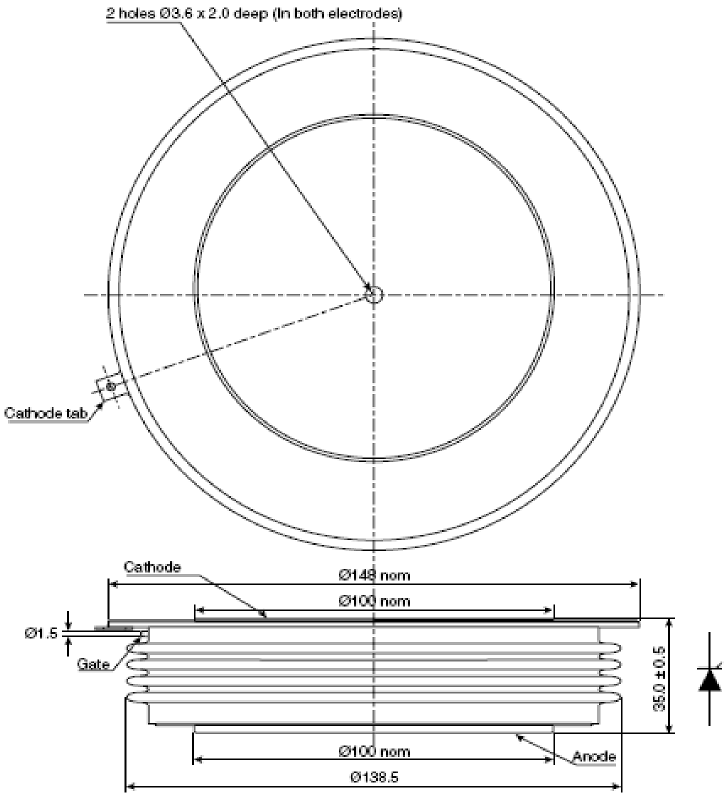


Fig. 15 Gate characteristics

PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.



Lead length: 420mm
Lead terminal connector: M4 ring

Package outline type code: A

Fig.16 Package outline

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HEADQUARTERS OPERATIONS

DYNEX SEMICONDUCTOR LIMITED
Doddington Road, Lincoln, Lincolnshire, LN6 3LF
United Kingdom.
Phone: +44 (0) 1522 500500
Fax: +44 (0) 1522 500550
Web: http://www.dynexsemi.com

CUSTOMER SERVICE

Phone: +44 (0) 1522 502753 / 502901
Fax: +44 (0) 1522 500020
e-mail: power_solutions@dynexsemi.com