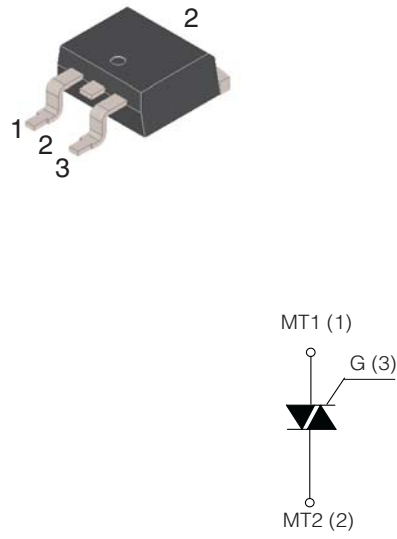



## LOGIC LEVEL TRIAC

<p><b>TO-252AA (DPAK)</b></p> 	<p><b>On-State Current</b> 8 Amp</p>	<p><b>Gate Trigger Current</b> &lt; 10 mA</p>	
	<p><b>Off-State Voltage</b> 400 V ÷ 800 V</p>		
	<p><b>FEATURES</b></p> <ul style="list-style-type: none"> <li>• Glass/passivated die junctions</li> <li>• Medium current Triac</li> <li>• Ideal for automated placement</li> <li>• Low thermal resistance</li> <li>• High surge current capability</li> <li>• Low forward voltage drop</li> <li>• Solder dip 260°C, 10s</li> <li>• Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC</li> <li>• Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C</li> </ul>		
	<p><b>MECHANICAL DATA</b></p> <ul style="list-style-type: none"> <li>• <b>Case:</b> TO-252AA (DPAK). Epoxy meets UL 94V-0 flammability rating.</li> <li>• <b>Polarity:</b> As marked on the body.</li> <li>• <b>Terminals:</b> Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.</li> </ul>		
<p><b>TYPICAL APPLICATIONS</b></p> <p>Logic level versions are designed to interface directly with low power drivers such as microcontrollers.</p>			

## Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 95^\circ C$	8	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7$ ms)	88	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20$ ms)	80	A
$I^2t$	Fusing Current	$t_p = 10$ ms, Half Cycle	32	A <sup>2</sup> s
$I_{GM}$	Peak Gate Current	20 $\mu$ s max. $T_j = 125^\circ C$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125^\circ C$	1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$ , $t_r \leq 100$ ns $f = 120$ Hz, $T_j = 125^\circ C$	50	A/ $\mu$ s
$T_j$	Operating Temperature		(-40 +125)	°C
$T_{stg}$	Storage Temperature		(-40 +150)	°C
$T_{sld}$	Soldering Temperature	10s max	260	°C

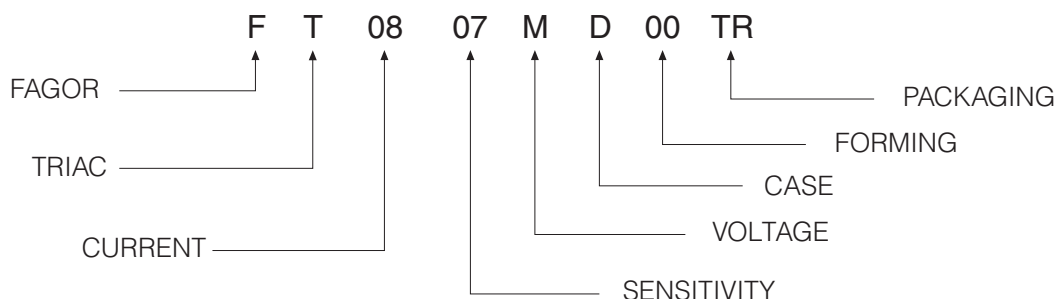
SYMBOL	PARAMETER	VOLTAGE			Unit
		D	M	N	
$V_{DRM}/V_{RRM}$	Repetitive Peak Off State Voltage	400	600	800	V

**LOGIC LEVEL TRIAC**
**Electrical Characteristics at Tamb = 25 °C**

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					07	08	
$I_{GT}^{(1)}$	Gate Trigger Current	$V_D = 12 V_{DC}, R_L = 33 \Omega, T_j = 25 \text{ }^\circ\text{C}$	Q1÷Q3	MAX	5	10	mA
			Q4	MAX	7		mA
$V_{GT}$	Gate Trigger Voltage	$V_D = 12 V_{DC}, R_L = 33 \Omega, T_j = 25 \text{ }^\circ\text{C}$	Q1÷Q3	MAX	1.3		V
			Q1÷Q4	MAX	1.3		V
$V_{GD}$	Gate Non Trigger Voltage	$V_D = V_{DRM}, R_L = 3.3 K\Omega, T_j = 125 \text{ }^\circ\text{C}$	Q1÷Q3	MIN	0.2		V
			Q1÷Q4	MIN	0.2		V
$I_H^{(2)}$	Holding Current	$I_T = 100 \text{ mA}, \text{ Gate open}, T_j = 25 \text{ }^\circ\text{C}$		MAX	15	15	mA
$I_L$	Latching Current	$I_G = 1.2 I_{GT}, T_j = 25 \text{ }^\circ\text{C}$	Q1,Q3	MAX		25	mA
			Q1,Q3,Q4	MAX	20		mA
			Q2	MAX	30	30	mA
$dV/dt^{(2)}$	Critical Rate of Voltage Rise	$V_D = 0.67 \times V_{DRM}, \text{ Gate open}$ $T_j = 125 \text{ }^\circ\text{C}$		MIN	20	40	V/ $\mu\text{s}$
$(dI/dt)_c^{(2)}$	Critical Rate of Current Rise	$(dv/dt)_c = 0.1 \text{ V}/\mu\text{s} \quad T_j = 125 \text{ }^\circ\text{C}$ $(dv/dt)_c = 10 \text{ V}/\mu\text{s} \quad T_j = 125 \text{ }^\circ\text{C}$ without snubber $T_j = 125 \text{ }^\circ\text{C}$		MIN	3.5	5.4	A/ms
				MIN	1.5	2.8	A/ms
				MIN	-	-	
$V_{TM}^{(2)}$	On-state Voltage	$I_T = 5.5 \text{ Amp}, t_p = 380 \mu\text{s}, T_j = 25 \text{ }^\circ\text{C}$		MAX	1.6		V
$V_{to}^{(2)}$	Threshold Voltage	$T_j = 125 \text{ }^\circ\text{C}$		MAX	0.85		V
$r_d^{(2)}$	Dynamic resistance	$T_j = 125 \text{ }^\circ\text{C}$		MAX	90		m $\Omega$
$I_{DRM}/I_{RRM}$	Off-State Leakage Current	$V_D = V_{DRM}, T_j = 125 \text{ }^\circ\text{C}$ $V_R = V_{RRM}, T_j = 25 \text{ }^\circ\text{C}$		MAX	1		mA
				MAX	5		$\mu\text{A}$
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle			1.8		$^\circ\text{C}/\text{W}$
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient	$S = 1 \text{ cm}^2$			70		$^\circ\text{C}/\text{W}$

(1) Minimum  $I_{GT}$  is guaranteed at 5% of  $I_{GT}$  max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

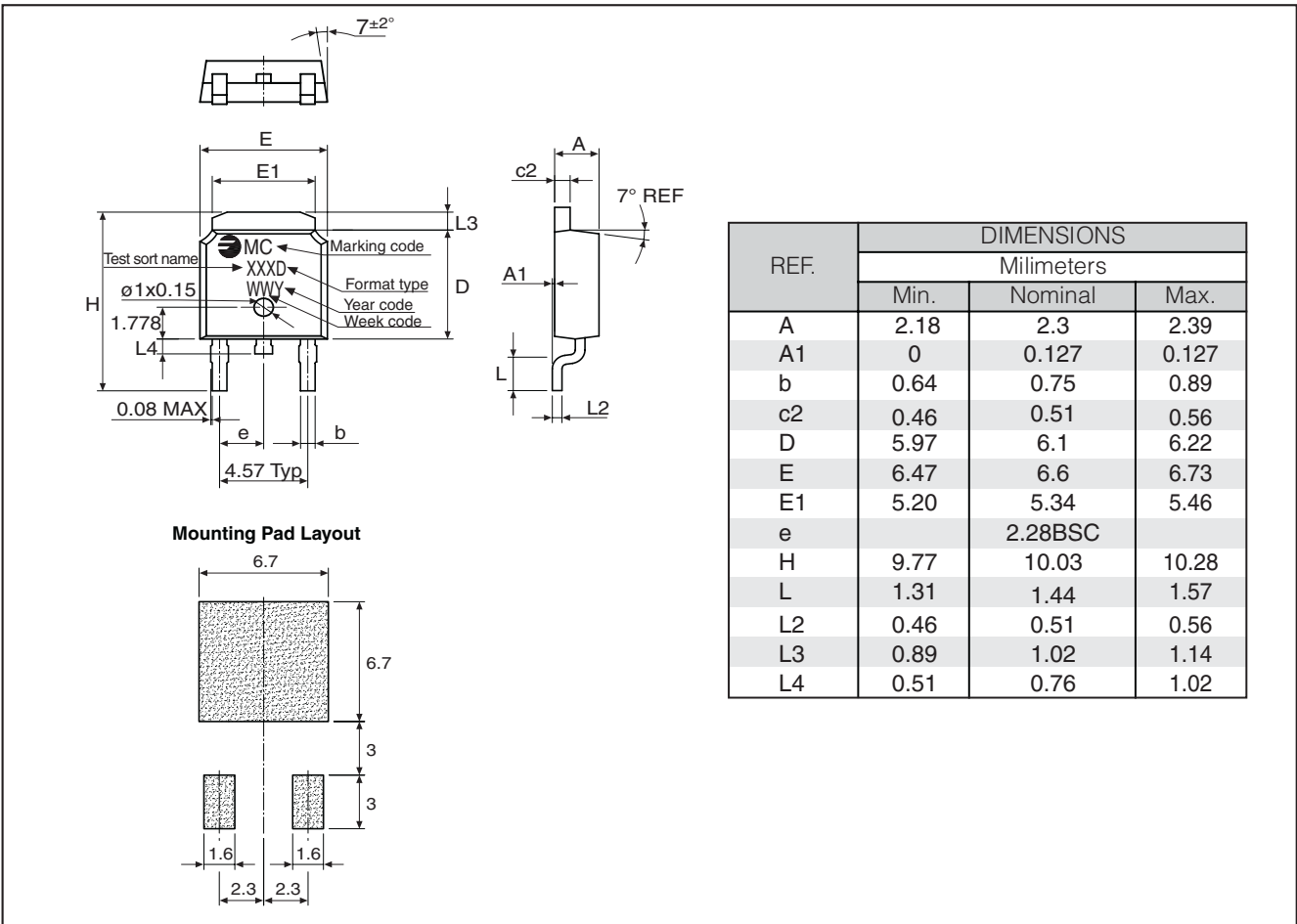
**Part Number Information**


**LOGIC LEVEL TRIAC**

**Ordering information**

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0807MD 00TR	TR	13" diameter tape and reel	2,500	0.30

**Package Outline Dimensions: (mm) TO-252AA (DPAK)**



**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

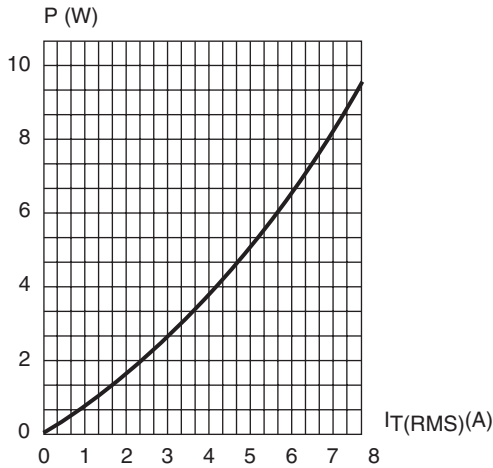


Fig. 2: RMS on-state current versus case temperature (full cycle).

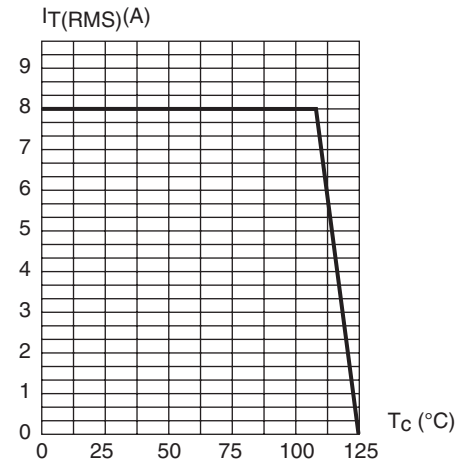


Fig. 3: Relative variation of thermal impedance versus pulse duration.

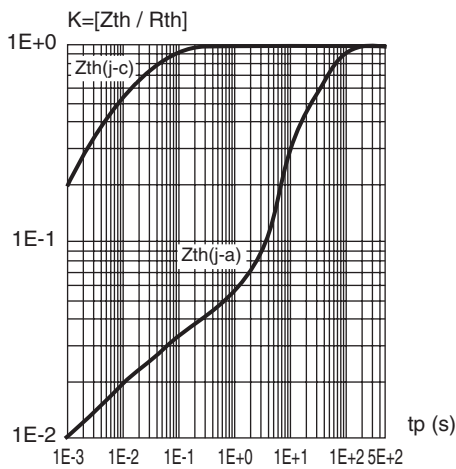


Fig. 4: On-state characteristics (maximum values)

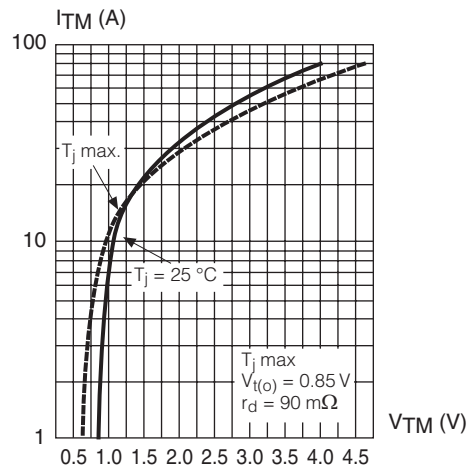


Fig. 5: Surge peak on-state current versus number of cycles

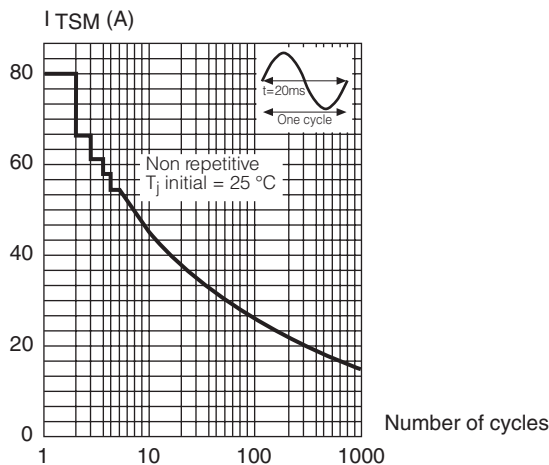
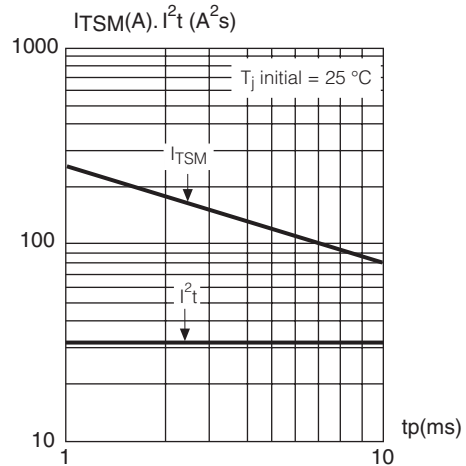


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.



**LOGIC LEVEL TRIAC**

**Ratings and Characteristics (Ta 25 °C unless otherwise noted)**

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

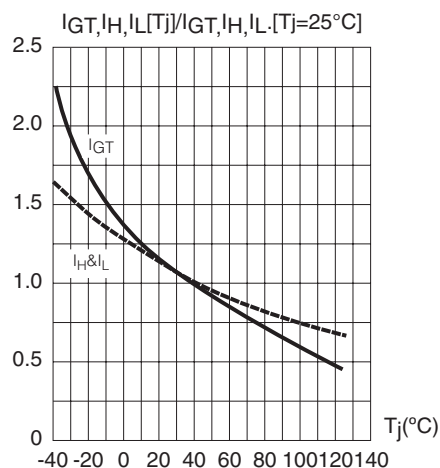


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

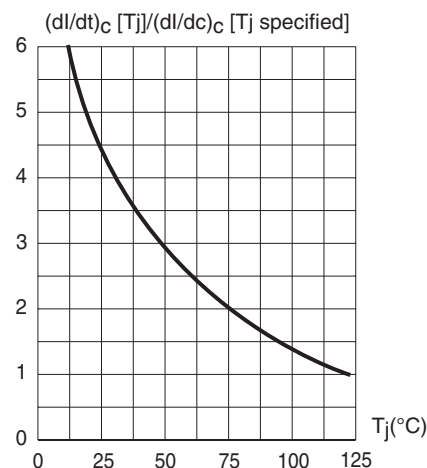
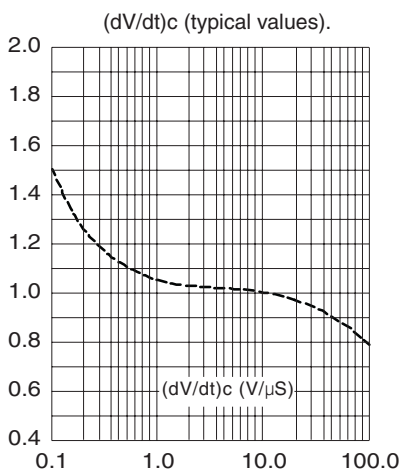


Fig. 9: Relative variation of critical rate of decrease of main current versus



**LOGIC LEVEL TRIAC****Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
14-Sep-2009	0	Original Data Sheet
24-May-2013	1	200V and 700V eliminated

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