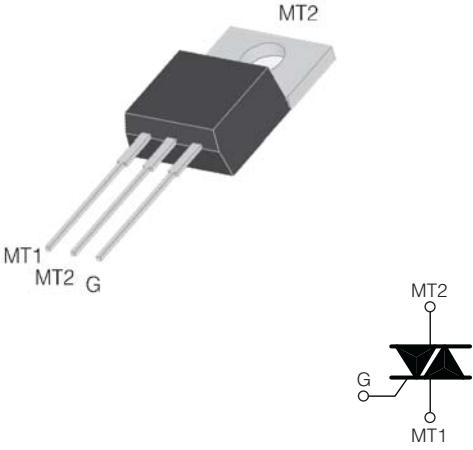


**LOGIC LEVEL TRIAC**

<p style="text-align: center;"><b>TO-220A B</b></p> 	<table style="width: 100%; border-collapse: collapse;"> <tr> <td style="width: 50%; vertical-align: top;"> <p><b>On-State Current</b> 4 Amp</p> </td> <td style="width: 50%; vertical-align: top;"> <p><b>Gate Trigger Current</b> &lt; 10 mA</p> </td> </tr> <tr> <td colspan="2" style="text-align: center; vertical-align: top;"> <p><b>Off-State Voltage</b> 200 V ÷ 800 V</p> </td> </tr> <tr> <td colspan="2" style="padding: 10px;"> <p>This series of TRIACs uses a high performance PNPN technology.</p> <p>These parts are intended for general purpose AC switching applications with highly inductive loads.</p> </td> </tr> </table>	<p><b>On-State Current</b> 4 Amp</p>	<p><b>Gate Trigger Current</b> &lt; 10 mA</p>	<p><b>Off-State Voltage</b> 200 V ÷ 800 V</p>		<p>This series of TRIACs uses a high performance PNPN technology.</p> <p>These parts are intended for general purpose AC switching applications with highly inductive loads.</p>	
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<p>This series of TRIACs uses a high performance PNPN technology.</p> <p>These parts are intended for general purpose AC switching applications with highly inductive loads.</p>							

**Absolute Maximum Ratings, according to IEC publication No. 134**

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_C = 95\text{ }^\circ\text{C}$	4	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 60 Hz ( $t = 16.7\text{ ms}$ )	33	A
$I_{TSM}$	Non-repetitive On-State Current	Full Cycle, 50 Hz ( $t = 20\text{ ms}$ )	30	A
$I^2t$	Fusing Current	$t_p = 10\text{ ms}$ , Half Cycle	4.5	$A^2s$
$I_{GM}$	Peak Gate Current	$20\text{ }\mu\text{s max.}$ $T_j = 125\text{ }^\circ\text{C}$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125\text{ }^\circ\text{C}$	1	W
$di/dt$	Critical rate of rise of on-state current	$I_G = 2x I_{GT}$ , $t_r \leq 100\text{ ns}$ $f = 120\text{ Hz}$ , $T_j = 125\text{ }^\circ\text{C}$	50	$A/\mu\text{s}$
$T_j$	Operating Temperature		$(-40 + 125)$	$^\circ\text{C}$
$T_{stg}$	Storage Temperature		$(-40 + 150)$	$^\circ\text{C}$
$T_{sld}$	Soldering Temperature	10s max	260	$^\circ\text{C}$

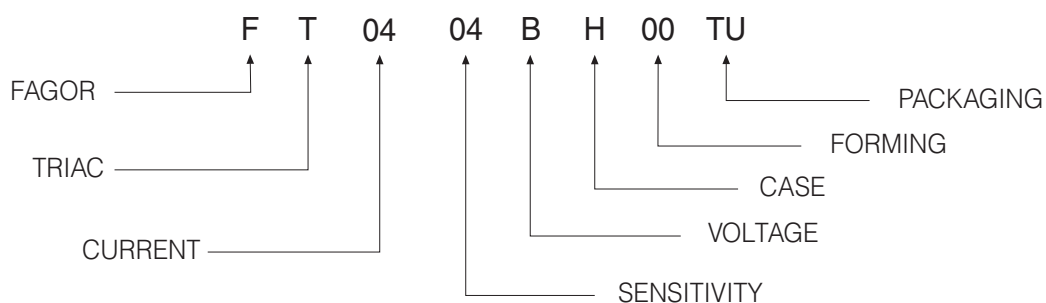
SYMBOL	PARAMETER	VOLTAGE					Unit
		B	D	M	S	N	
$V_{DRM}$	Repetitive Peak Off State Voltage	200	400	600	700	800	V
$V_{RRM}$							

**LOGIC LEVEL TRIAC**
**Electrical Characteristics**

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY					Unit
					04	05	07	08	09	
I <sub>GT</sub> <sup>(1)</sup>	Gate Trigger Current	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	5	5	5	10	10	mA
			Q4	MAX		5	7		10	mA
V <sub>GT</sub>	Gate Trigger Voltage	V <sub>D</sub> = 12 V <sub>DC</sub> , R <sub>L</sub> = 33Ω, T <sub>j</sub> = 25 °C	Q1÷Q3	MAX	1.3					V
			Q1÷Q4	MAX	1.3					V
V <sub>GD</sub>	Gate Non Trigger Voltage	V <sub>D</sub> = V <sub>DRM</sub> , R <sub>L</sub> = 3.3 KΩ, T <sub>j</sub> = 125 °C	Q1÷Q3	MIN	0.2					V
			Q1÷Q4	MIN	0.2					V
I <sub>H</sub> <sup>(2)</sup>	Holding Current	I <sub>T</sub> = 100 mA, Gate open, T <sub>j</sub> = 25 °C		MAX	10	10	15	15	20	mA
I <sub>L</sub>	Latching Current	I <sub>G</sub> = 1.2 I <sub>GT</sub> , T <sub>j</sub> = 25 °C	Q1,Q3	MAX	10			25		mA
			Q1,Q3,Q4	MAX		10	20		20	mA
			Q2	MAX	20	20	30	30	25	mA
dV/dt <sup>(2)</sup>	Critical Rate of Voltage Rise	V <sub>D</sub> = 0.67 x V <sub>DRM</sub> , Gate open T <sub>j</sub> = 125 °C		MIN	20	20	20	40	40	V/μs
(dI/dt) <sub>c</sub> <sup>(2)</sup>	Critical Rate of Current Rise	(dv/dt) <sub>c</sub> = 0.1 V/μs T <sub>j</sub> = 125 °C (dv/dt) <sub>c</sub> = 10 V/μs T <sub>j</sub> = 125 °C without snubber T <sub>j</sub> = 125 °C		MIN	1.8	1.8	1.8	2.7	2.5	A/ms
				MIN	0.9	0.9	0.9	2.0	1.5	A/ms
				MIN	-	-	-	-	-	
V <sub>TM</sub> <sup>(2)</sup>	On-state Voltage	I <sub>T</sub> = 5.5 Amp, tp = 380 μs, T <sub>j</sub> = 25 °C		MAX	1.6					V
V <sub>t(o)</sub> <sup>(2)</sup>	Threshold Voltage	T <sub>j</sub> = 125 °C		MAX	0.9					V
r <sub>d</sub> <sup>(2)</sup>	Dynamic resistance	T <sub>j</sub> = 125 °C		MAX	120					mΩ
I <sub>DRM</sub> /I <sub>RRM</sub>	Off-State Leakage Current	V <sub>D</sub> = V <sub>DRM</sub> , T <sub>j</sub> = 125 °C		MAX	0.5					mA
		V <sub>R</sub> = V <sub>RRM</sub> , T <sub>j</sub> = 25 °C		MAX	5					μA
R <sub>th(j-c)</sub>	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.0					°C/W
R <sub>th(j-a)</sub>	Thermal Resistance Junction-Ambient	S = 1 cm <sup>2</sup>			60					°C/W

(1) Minimum I<sub>GT</sub> is guaranteed at 5% of I<sub>GT</sub> max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

**PART NUMBER INFORMATION**


### LOGIC LEVEL TRIAC

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

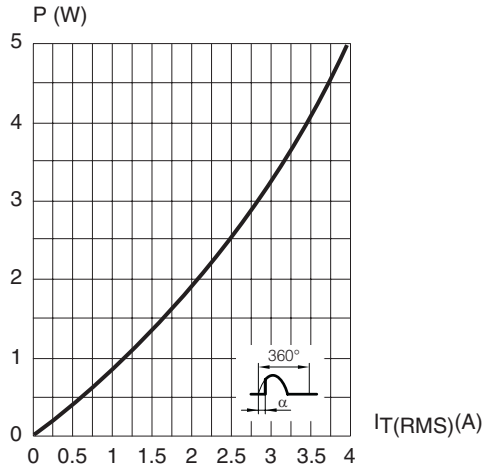


Fig. 2: RMS on-state current versus case temperature (full cycle).

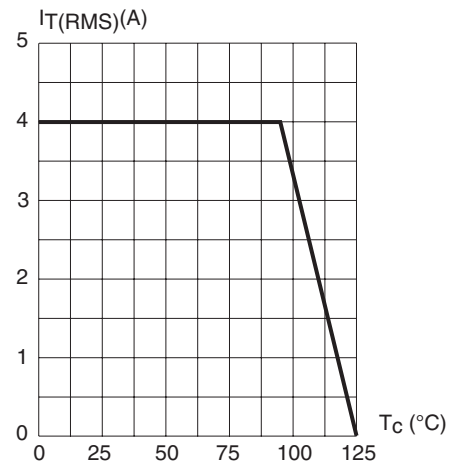


Fig. 3: Relative variation of thermal impedance versus pulse duration.

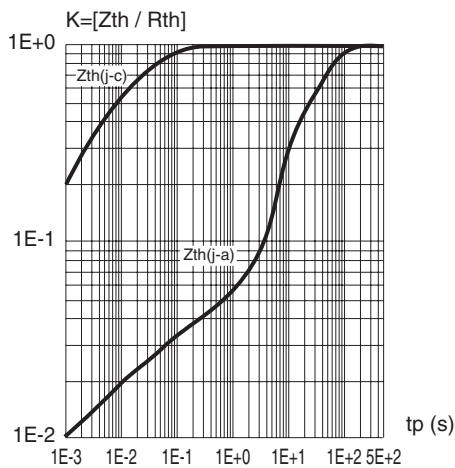


Fig. 4: On-state characteristics (maximum values)

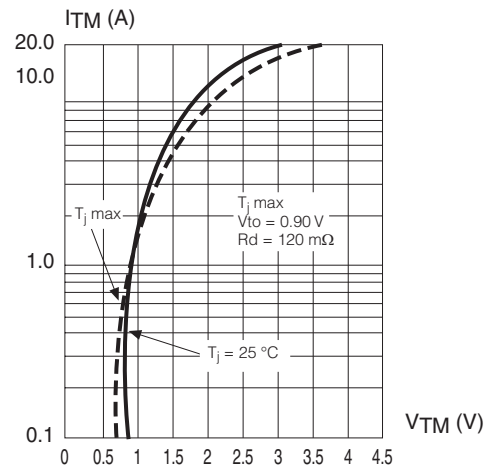


Fig. 5: Surge peak on-state current versus number of cycles

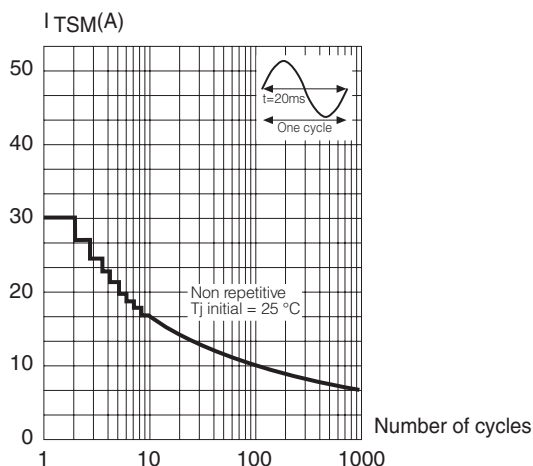
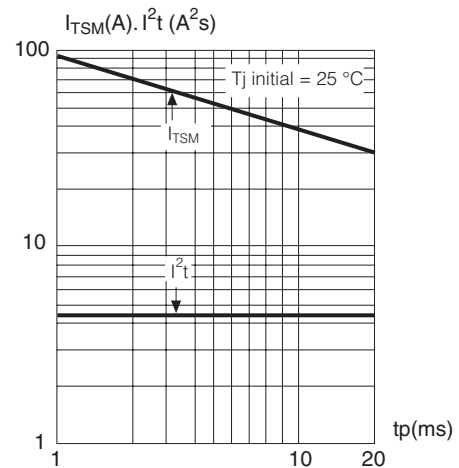


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width:  $t_p < 10 \text{ ms}$ , and corresponding value of  $I^2t$ .



### LOGIC LEVEL TRIAC

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

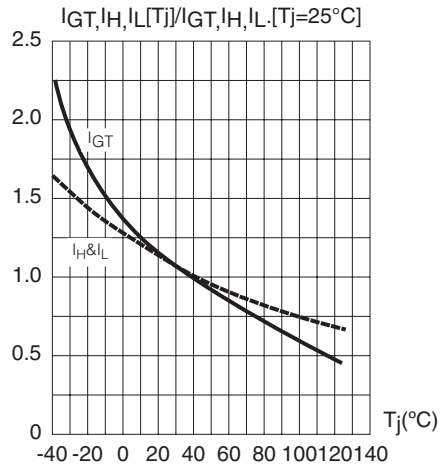


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

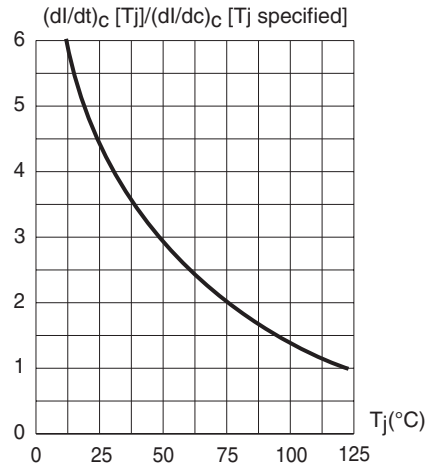
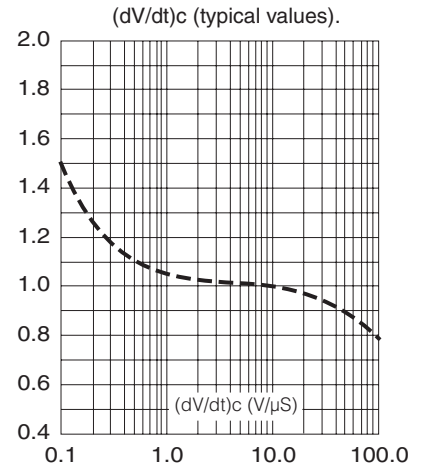
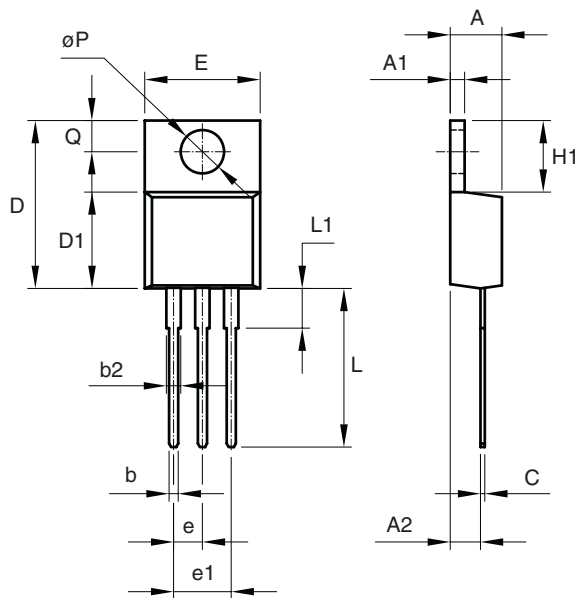


Fig. 9: Relative variation of critical rate of decrease of main current versus



### PACKAGE MECHANICAL DATA

### TO-220AB



REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	4.47	4.67
A1	1.17	1.37
A2	2.52	2.82
b	0.71	0.91
b2	1.17	1.37
c	0.31	0.53
D	14.65	15.35
D1	8.50	8.90
E	10.01	10.36
e	2.51	2.57
e1	4.98	5.18
H1	6.15	6.45
L	13.40	13.96
L1	3.56	3.96
P	3.735	3.935
Q	2.59	2.89

**Mounting Torque**

**1 N.m**

(\*) Limiting values and life support applications, see Web page.