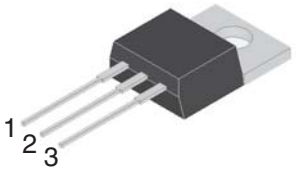
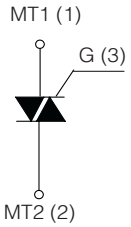
INSULATED LOGIC LEVEL TRIAC

INSULATED TO-220AB





On-State Current
12 Amp

Gate Trigger Current
≤ 10 mA (08)
≤ 5 mA (04)

Off-State Voltage
200 V ÷ 800 V

FEATURES

- Glass/passivated die junctions
- Provides voltage insulated tab (rated at 2500V RMS)
- Medium current Triac
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C
- Certified compliance of UL 1557 Standard for Electrically Isolated Semiconductors. Fille reference E320541, Vol. 3

Pb

e3

RoHS COMPLIANT

MECHANICAL DATA

- **Case:** INSULATED TO-220AB. Epoxy meets UL 94V-0 flammability rating.
- **Polarity:** As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

TYPICAL APPLICATIONS

Logic level versions are designed to interface directly with low power drivers such as microcontrollers.

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, T_C = 90 °C	12	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz (t = 16.7 ms)	125	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz (t = 20 ms)	120	A
I^2t	Fusing Current	tp = 10 ms, Half Cycle	72	A^2s
I_{GM}	Peak Gate Current	20 µs max. T_j = 125 °C	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	T_j = 125 °C	1	W
dI/dt	Critical rate of rise of on-state current	I_G = 2x I_{GT}, t_r ≤100ns f = 120 Hz, T_j = 125 °C	50	A/µs
T_j	Operating Temperature		(-40 +125)	°C
T_{stg}	Storage Temperature		(-40 +125)	°C
T_{sld}	Soldering Temperature	10s max	260	°C
V_{iso}	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

SYMBOL	PARAMETER	VOLTAGE				Unit
		B	D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	800	V

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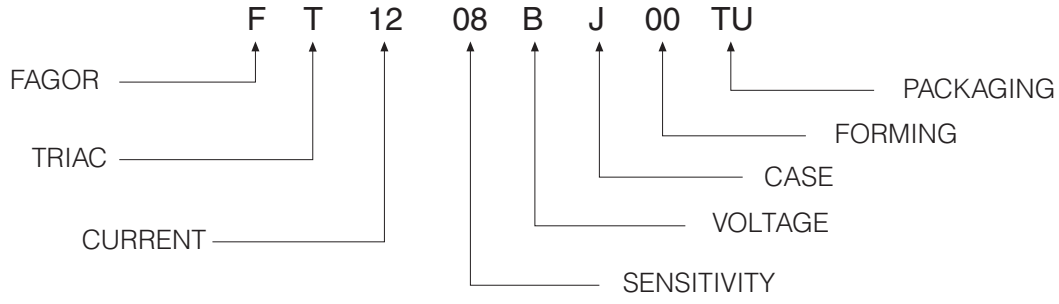
Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY		Unit
					04	08	
I_{GT} (1)	Gate Trigger Current	V_D = 12 V_{DC}, R_L = 33Ω, T_j = 25 °C	Q1÷Q3	MAX	5	10	mA
			Q4	MAX	-	-	mA
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC}, R_L = 33Ω, T_j = 25 °C	Q1÷Q3	MAX	1.3	1.3	V
			Q1÷Q4	MAX	-	-	V
V_{GD}	Gate Non Trigger Voltage	V_D = V_{DRM}, R_L = 3.3 KΩ, T_j = 125 °C	Q1÷Q3	MIN	0.2	0.2	V
			Q1÷Q4	MIN	-	-	V
I_H (2)	Holding Current	I_T = 100 mA, Gate open, T_j = 25 °C		MAX	15		mA
I_L	Latching Current	I_G = 1.2 I_{GT}, T_j = 25 °C	Q1,Q3	MAX	10	25	mA
			Q2	MAX	15	30	mA
dV/dt (2)	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM}, Gate open T_j = 125 °C		MIN	20	40	V/µs
(dI/dt)c (2)	Critical Rate of Current Rise	(dv/dt)c = 0.1 V/µs T_j = 125 °C		MIN	3.5	6.5	A/ms
		(dv/dt)c = 10 V/µs T_j = 125 °C		MIN	1	2.9	A/ms
V_{TM} (2)	On-state Voltage	I_T = 17 Amp, tp = 380 µs, T_j = 25 °C		MAX	1.55		V
$V_{t(o)}$ (2)	Threshold Voltage	T_j = 125 °C		MAX	0.85		V
r_d (2)	Dynamic resistance	T_j = 125 °C		MAX	35		mΩ
I_{DRM}/I_{RRM}	Off-State Leakage Current	V_D = V_{DRM}, T_j = 125 °C		MAX	1		mA
		V_R = V_{RRM}, T_j = 25 °C		MAX	5		µA
$R_{th(j-c)}$	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.3		°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Ambient				60		°C/W

(1) Minimum I_{GT} is guaranted at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

Part Number Information

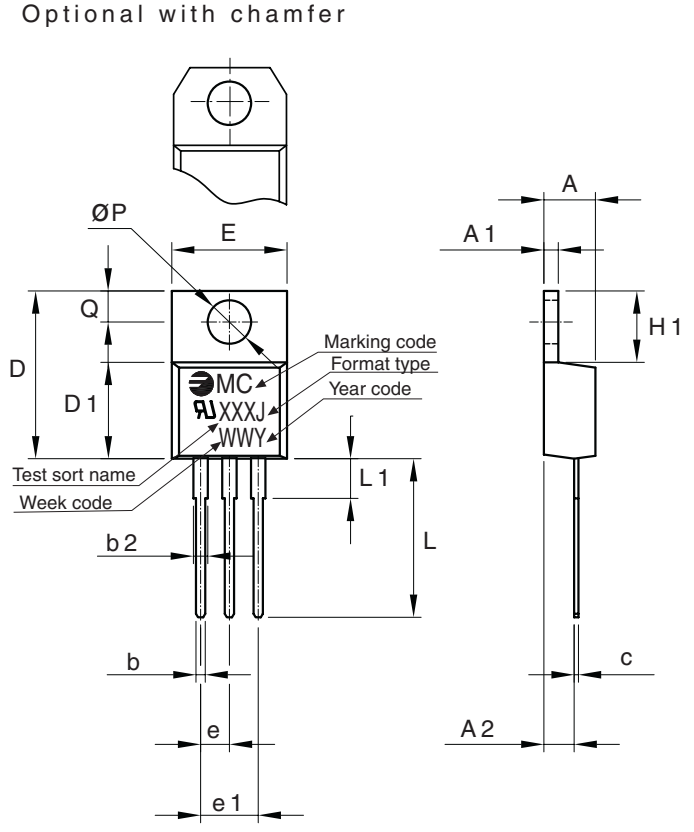


INSULATED LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT1208MJ 00TU	TU	TUBE	1000	2.30

Package Outline Dimensions: (mm) INSULATED TO-220AB



REF.	DIMENSIONS Milimeters	
	Min.	Max.
A	4.32	4.62
A1	1.21	1.29
A2	2.40	2.70
b	0.80	0.83
b2	1.40	--
c	0.42	0.48
D	15.5	15.68
D1	9.26	9.42
E	10.08	10.24
e	2.54	2.54
e1	5.08	5.08
H1	6.24	6.26
L	12.81	13.81
L1	3.28	4.17
P	3.70	3.80
Q	2.75	2.85

Mounting Torque	**0.8 N.m**

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Ratings and Characteristics (Ta 25 ºC unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

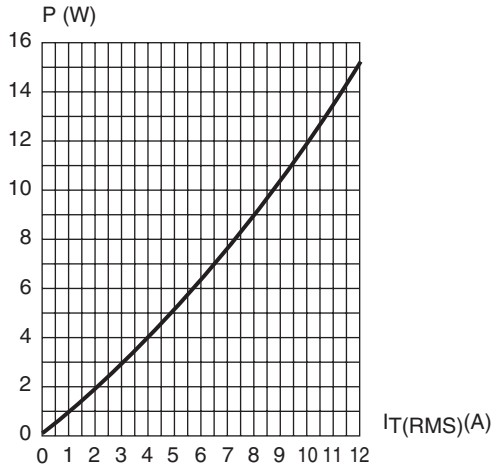


Fig. 2: RMS on-state current versus case temperature (full cycle).

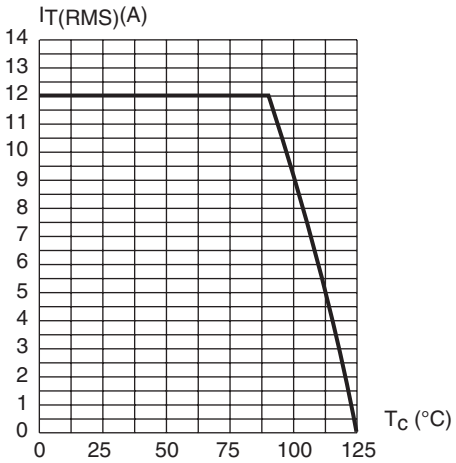


Fig. 3: Relative variation of thermal impedance versus pulse duration.

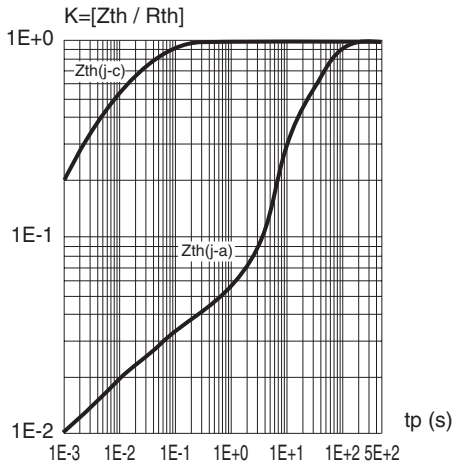


Fig. 4: On-state characteristics (maximum values)

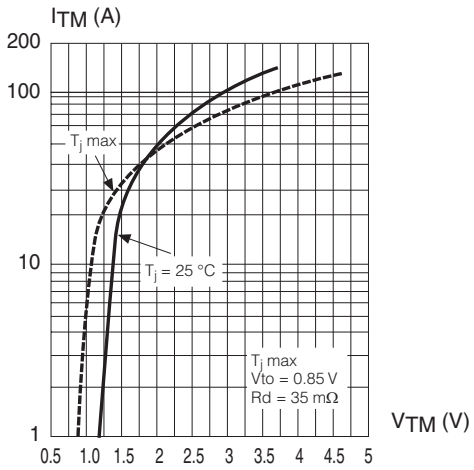


Fig. 5: Surge peak on-state current versus number of cycles

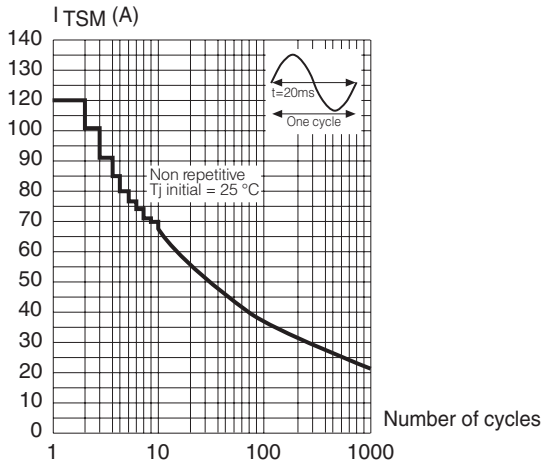
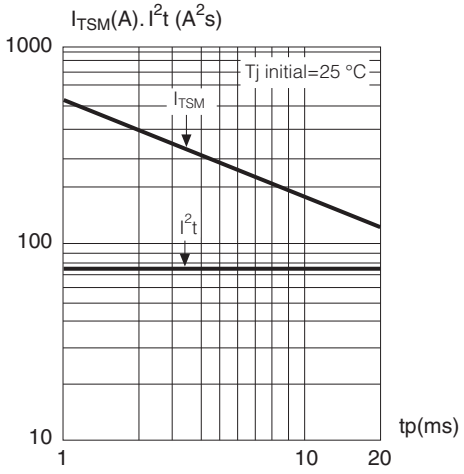


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 20 ms, and corresponding value of I^2t.



Ratings and Characteristics (Ta 25 ºC unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

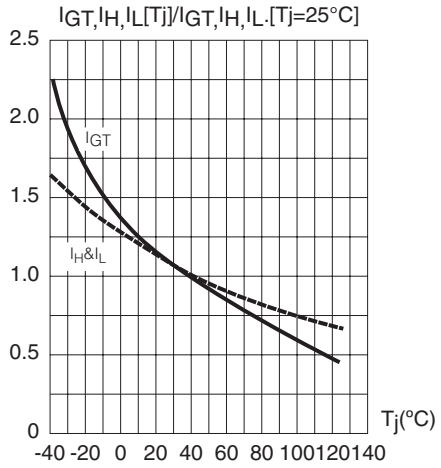


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

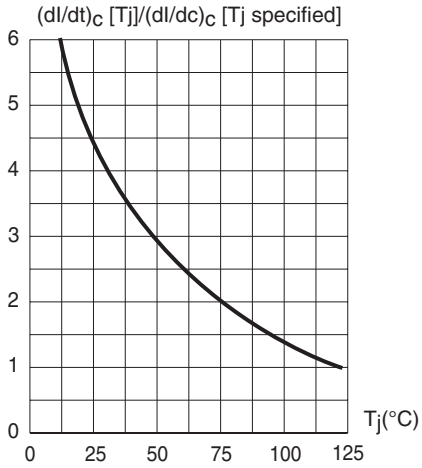
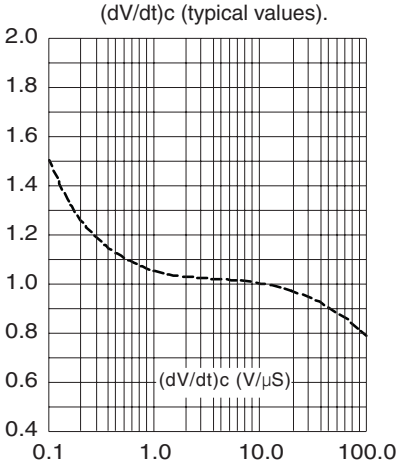


Fig. 9: Relative variation of critical rate of decrease of main current versus (dV/dt)c (typical values).



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