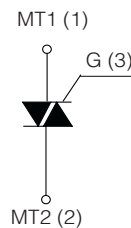
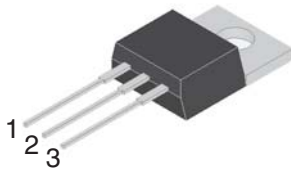


INSULATED LOGIC LEVEL TRIAC

INSULATED TO-220AB



On-State Current 8 Amp	Gate Trigger Current ≤ 10 mA (08) & (09) ≤ 5 mA (04)
Off-State Voltage 200 V ÷ 800 V	

FEATURES

- Glass/passivated die junctions
- Provides voltage insulated tab (rated at 2500V RMS)
- Medium current Triac
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C
- Certified compliance of UL 1557 Standard for Electrically Isolated Semiconductors. Fille reference E320541, Vol. 3



RoHS
COMPLIANT

MECHANICAL DATA

- **Case:** INSULATED TO-220AB. Epoxy meets UL 94V-0 flammability rating.
- **Polarity:** As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

TYPICAL APPLICATIONS

Logic level versions are designed to interface directly with low power drivers such as microcontrollers.

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	RMS On-state Current (full sine wave)	All Conduction Angle, $T_c = 100\text{ }^\circ\text{C}$	8	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 60 Hz ($t = 16.7\text{ ms}$)	84	A
I_{TSM}	Non-repetitive On-State Current	Full Cycle, 50 Hz ($t = 20\text{ ms}$)	80	A
I^2t	Fusing Current	$t_p = 10\text{ ms}$, Half Cycle	36	A^2s
I_{GM}	Peak Gate Current	$20\text{ }\mu\text{s max.}$ $T_j = 125\text{ }^\circ\text{C}$	4	A
$P_{G(AV)}$	Average Gate Power Dissipation	$T_j = 125\text{ }^\circ\text{C}$	1	W
di/dt	Critical rate of rise of on-state current	$I_G = 2 \times I_{GT}$, $t_r \leq 100\text{ ns}$ $f = 120\text{ Hz}$, $T_j = 125\text{ }^\circ\text{C}$	50	A/ μs
T_j	Operating Temperature		(-40 +125)	$^\circ\text{C}$
T_{sta}	Storage Temperature		(-40 +125)	$^\circ\text{C}$
T_{sld}	Soldering Temperature	10s max	260	$^\circ\text{C}$
V_{iso}	R.M.S. isolation voltage 50/60 Hz sinusoidal waveform		2.500	Vac

SYMBOL	PARAMETER	VOLTAGE				Unit
		B	D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	200	400	600	800	V

INSULATED LOGIC LEVEL TRIAC

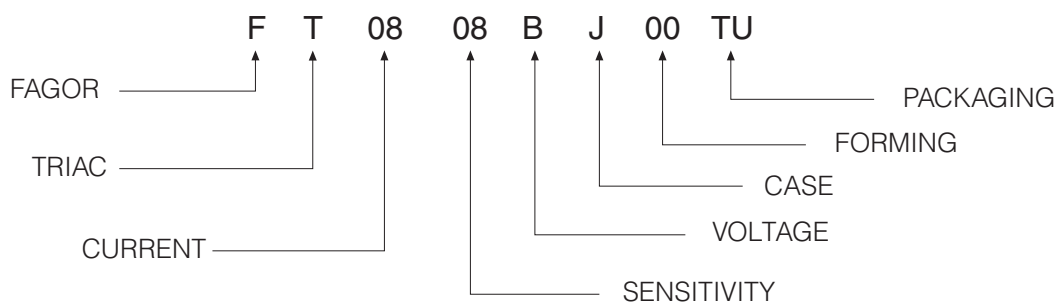
Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS	Quadrant		SENSITIVITY			Unit
					04	08	09	
I _{GT} ⁽¹⁾	Gate Trigger Current	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	5	10	10	mA
			Q4	MAX	-	-	10	mA
V _{GT}	Gate Trigger Voltage	V _D = 12 V _{DC} , R _L = 33Ω, T _j = 25 °C	Q1÷Q3	MAX	1.3	1.3	-	V
			Q1÷Q4	MAX	-	-	1.3	V
V _{GD}	Gate Non Trigger Voltage	V _D = V _{DRM} , R _L = 3.3 KΩ, T _j = 125 °C	Q1÷Q3	MIN	0.2	0.2	-	V
			Q1÷Q4	MIN	-	-	0.2	V
I _H ⁽²⁾	Holding Current	I _T = 100 mA, Gate open, T _j = 25 °C		MAX	10	15	20	mA
I _L	Latching Current	I _G = 1.2 I _{GT} , T _j = 25 °C	Q1,Q3	MAX	10	25	-	mA
			Q2	MAX	15	30	25	mA
dV/dt ⁽²⁾	Critical Rate of Voltage Rise	V _D = 0.67 x V _{DRM} , Gate open T _j = 125 °C		MIN	20	40	50	V/μs
(dI/dt) _c ⁽²⁾	Critical Rate of Current Rise	(dv/dt) _c = 0.1 V/μs T _j = 125 °C (dv/dt) _c = 10 V/μs T _j = 125 °C		MIN	3.5	5.4	3.5	A/ms
				MIN	1.5	2.98	1.8	A/ms
V _{TM} ⁽²⁾	On-state Voltage	I _T = 11 Amp, t _p = 380 μs, T _j = 25 °C		MAX	1.55			V
V _{t(o)} ⁽²⁾	Threshold Voltage	T _j = 125 °C		MAX	0.85			V
r _d ⁽²⁾	Dynamic resistance	T _j = 125 °C		MAX	50			mΩ
I _{DRM} /I _{RRM}	Off-State Leakage Current	V _D = V _{DRM} , T _j = 125 °C V _R = V _{RRM} , T _j = 25 °C		MAX	1			mA
				MAX	5			μA
R _{th(j-c)}	Thermal Resistance Junction-Case	for AC 360° conduction angle			2.5			°C/W
R _{th(j-a)}	Thermal Resistance Junction-Ambient				60			°C/W

(1) Minimum I_{GT} is guaranteed at 5% of I_{GT} max.

(2) For either polarity of electrode MT2 voltage with reference to electrode MT1.

Part Number Information



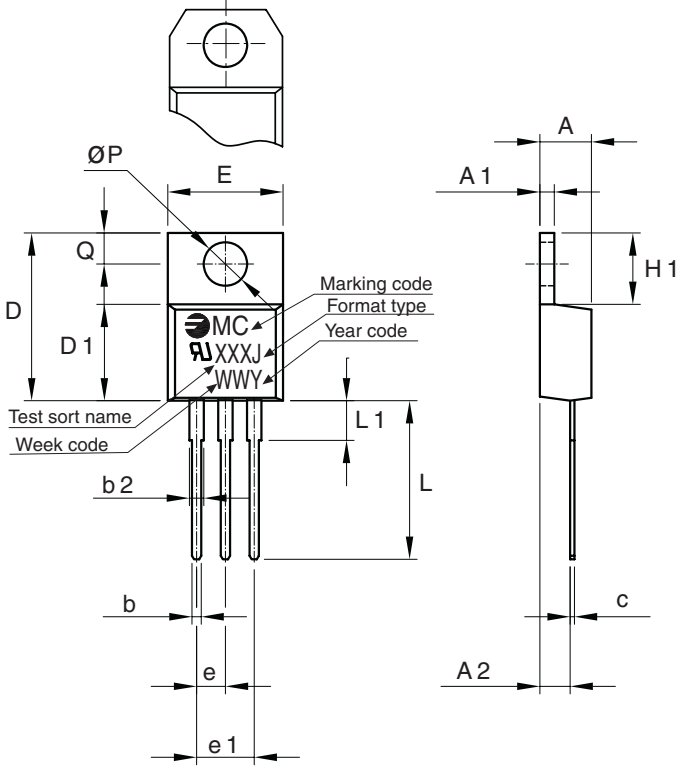
INSULATED LOGIC LEVEL TRIAC

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FT0808MJ 00TU	TU	TUBE	1000	2.30

Package Outline Dimensions: (mm) INSULATED TO-220AB

Optional with chamfer



The drawing shows a top view and a side view of the TO-220AB package. The top view includes dimensions: $\varnothing P$ (lead diameter), E (lead spacing), D (total width), Q (lead height), $D1$ (body width), L (total length), $L1$ (lead length), b (lead width), $b2$ (lead thickness), e (lead pitch), and $e1$ (lead offset). The side view shows dimensions: A (total height), $A1$ (lead height), $A2$ (body height), $H1$ (lead thickness), and c (lead diameter). Marking details include: MC (Marking code), XXXJ (Format type), WWY (Year code), and Test sort name/Week code.

REF.	DIMENSIONS	
	Millimeters	
	Min.	Max.
A	4.32	4.62
A1	1.21	1.29
A2	2.40	2.70
b	0.80	0.83
b2	1.40	--
c	0.42	0.48
D	15.5	15.68
D1	9.26	9.42
E	10.08	10.24
e	2.54	2.54
e1	5.08	5.08
H1	6.24	6.26
L	12.81	13.81
L1	3.28	4.17
P	3.70	3.80
Q	2.75	2.85

Mounting Torque	0.8 N.m
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INSULATED LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 1: Maximum power dissipation versus RMS on-state current (full cycle).

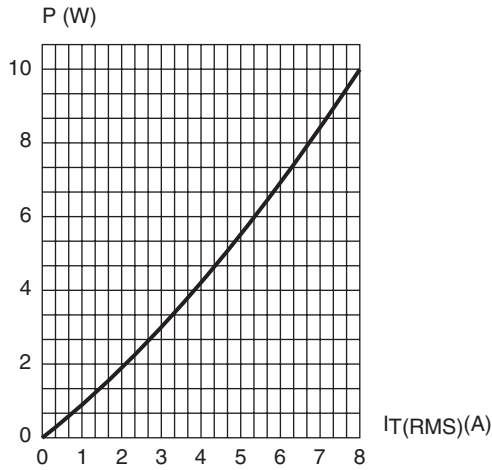


Fig. 2: RMS on-state current versus case temperature (full cycle).

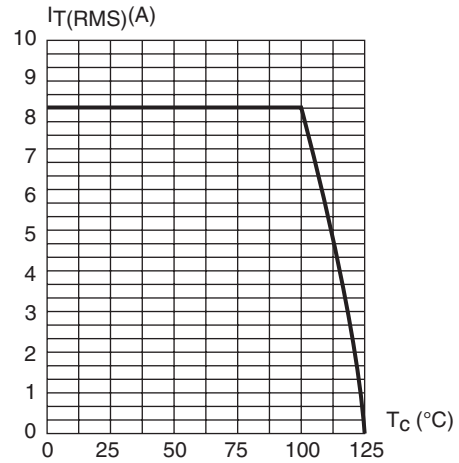


Fig. 3: Relative variation of thermal impedance versus pulse duration.

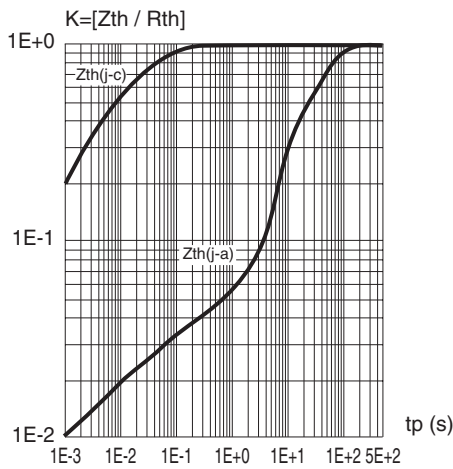


Fig. 4: On-state characteristics (maximum values)

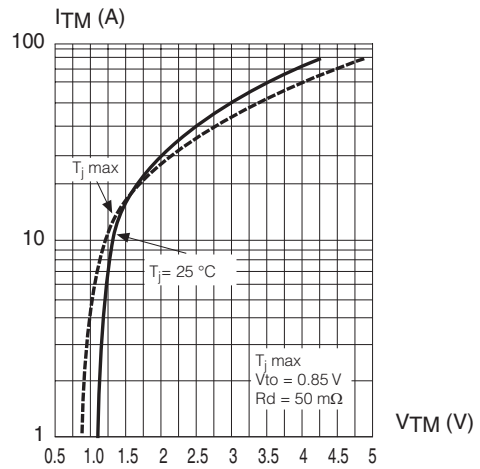


Fig. 5: Surge peak on-state current versus number of cycles

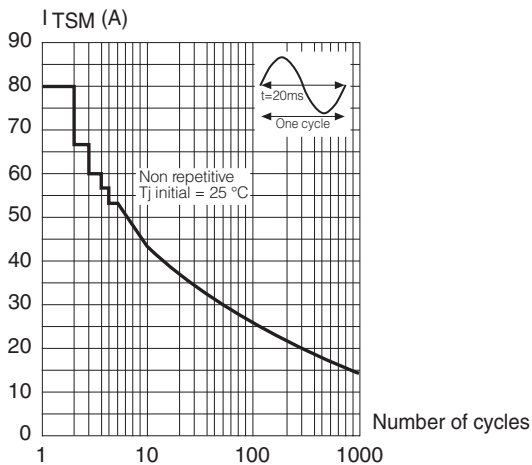
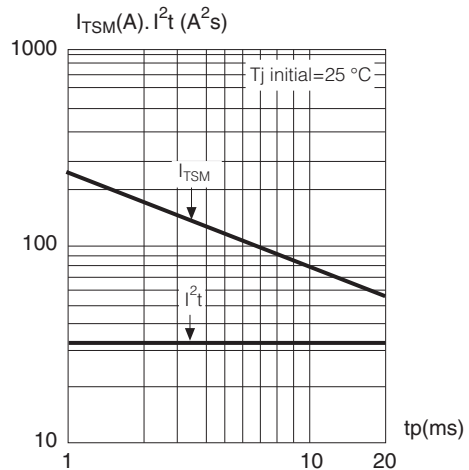


Fig. 6: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I²t.



INSULATED LOGIC LEVEL TRIAC

Ratings and Characteristics (Ta 25 °C unless otherwise noted)

Fig. 7: Relative variation of gate trigger current, holding current and latching versus junction temperature (typical values)

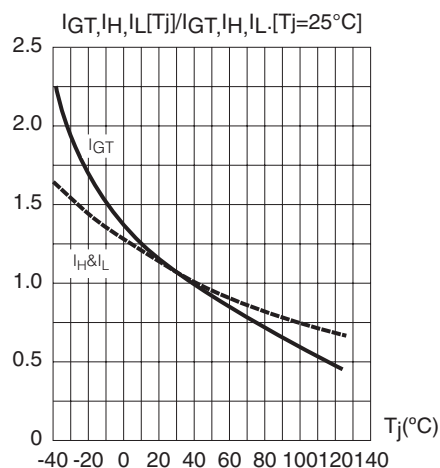


Fig. 8: Relative variation of critical rate of decrease of main current versus junction temperature

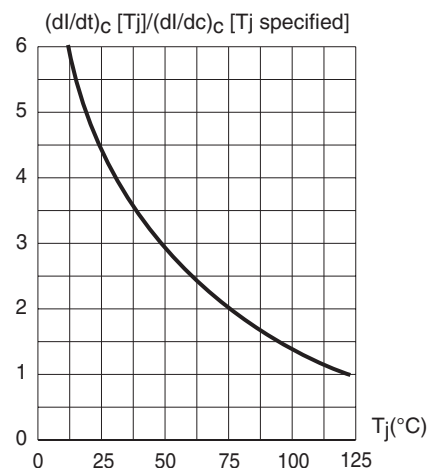
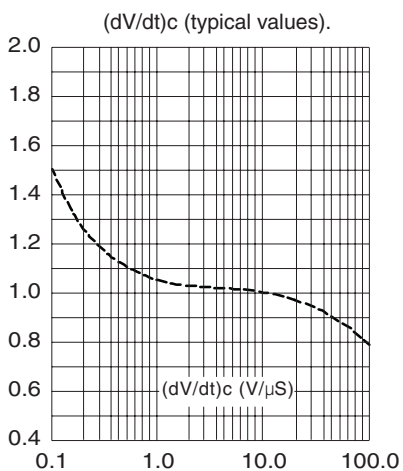


Fig. 9: Relative variation of critical rate of decrease of main current versus $(dV/dt)_c$ (typical values).



INSULATED LOGIC LEVEL TRIAC

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