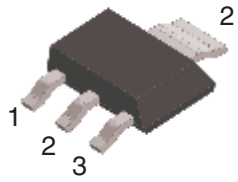
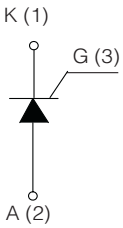
SENSITIVE GATE SCR

TO-261AA (SOT-223)





On-State Current 1.25 Amp

Gate Trigger Current < 200 µA

Off-State Voltage 400 V ÷ 800 V

FEATURES

- Glass/passivated die junctions
- Low current SCR
- Low thermal resistance
- High surge current capability
- Low forward voltage drop
- Solder dip 260°C, 10s
- Component in accordance to RoHS 2011/65/EU and WEEE 2002/96/EC
- Meets MSL level 3, per J-STD-020, LF maximum peak of 260° C

RoHS COMPLIANT

MECHANICAL DATA

- **Case:** TO-261AA (SOT-223). Epoxy meets UL 94V-0 flammability rating.
- **Polarity:** As marked on the body.
- **Terminals:** Matte tin plated leads, solderable per MIL-STD-750 Method 2026, J-STD-002 and JESD22-B102. Consumer grade, meets JESD 201 class 1A whisker test.

TYPICAL APPLICATIONS

Thanks to highly sensitive triggering levels, the FS02xxxN SCR series is suitable for all applications where available gate current is limited, such as ground fault circuit interruptors, pilot circuits in solid state relays, stand-by mode power supplies, smoke and alarm detectors.

Maximun Ratings and Electrical Characteristics at 25°C

SYMBOL	PARAMETER	CONDITIONS	Value	Unit
$I_{T(RMS)}$	On-state Current	180 ° Conduction Angle, T_C = 115 °C	1.25	A
$I_{T(AV)}$	Average On-state Current	Half Cycle, Θ = 180 °, T_C = 115 °C	0.8	A
I_{TSM}	Non-repetitive On-State Current	Half Cycle, 60 Hz	25	A
I_{TSM}	Non-repetitive On-State Current	Halfl Cycle, 50 Hz	22.5	A
I^2t	Fusing Current	tp = 10 ms, Half Cycle	2.5	A^2s
I_{GM}	Peak Gate Current	20 µs max.	1.2	A
P_{GM}	Peak Gate Dissipation	20 µs max.	3	W
$P_{G(AV)}$	Gate Dissipation	20ms max.	0.2	W
T_j	Operating Temperature		(-40 to +125)	°C
T_{stg}	Storage Temperature		(-40 to +150)	°C
T_{sld}	Soldering Temperature	10s max.	260	°C

SYMBOL	PARAMETER	CONDITIONS	VOLTAGE			Unit
			D	M	N	
V_{DRM}/V_{RRM}	Repetitive Peak Off State Voltage	R_{GK} = 1 kΩ	400	600	800	V

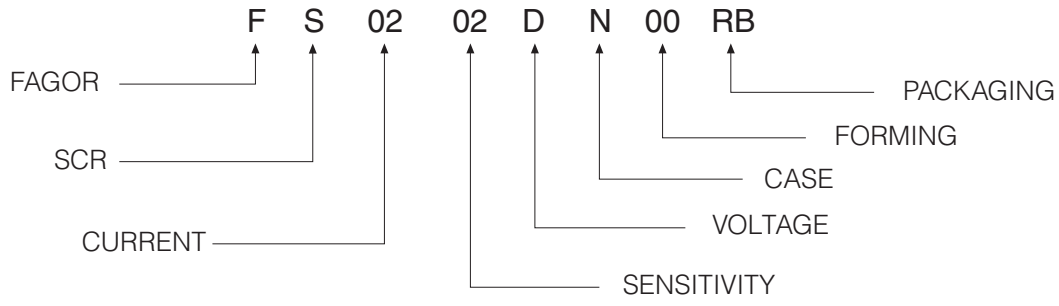
SENSITIVE GATE SCR

Electrical Characteristics at Tamb = 25 °C

SYMBOL	PARAMETER	CONDITIONS		SENSITIVITY				Unit
				01	02	03	04	
I_{GT}	Gate Trigger Current	V_D = 12 V_{DC}, R_L = 140Ω. T_j = 25 °C	MIN MAX	1 20	 200	20 200	15 50	µA
V_{GT}	Gate Trigger Voltage	V_D = 12 V_{DC}, R_L = 140Ω, T_j = 25 °C	MAX	0.8				V
V_{GD}	Gate Non Trigger Voltage	V_D = V_{DRM}, R_L = 3.3kΩ R_{GK} = 220Ω T_j = 125 °C	MIN	0.1				V
V_{RGM}	Reverse Gate Voltage	I_{RG} = 10µA,	MIN	8				V
I_H	Holding Current	I_T = 50 mA, R_{GK} = 1 kΩ T_j = 25 °C	MAX	5	5	7	5	mA
I_L	Latching Current	I_G = 1 mA, R_{GK} = 1 kΩ	MAX	6	6	7	6	mA
dV / dt	Critical Rate of Voltage Rise	V_D = 0.67 x V_{DRM}, R_{GK} = 1 kΩ, T_j = 125 °C	MIN	15	10	30	30	V/µs
dI / dt	Critical Rate of Current Rise	I_G = 2 x I_{GT} tr ≤ 100 ns, f = 60 Hz, T_j = 125 °C	MIN	50				A/µs
V_{TM}	On-state Voltage	at I_T = 2.5 Amp, tp = 380 µs, T_j = 25 °C	MAX	1.45		2	1.45	V
V_{t0}	Threshold Voltage	T_j = 125 °C	MAX	0.90				V
r_d	Dynamic resistance	T_j = 125 °C	MAX	150				mΩ
I_{DRM} / I_{RRM}	Off-State Leakage Current	V_D = V_{DRM}, R_{GK} = 1kΩ T_j = 125 °C V_R = V_{RRM}, T_j = 25 °C	MAX MAX	500 5				µA µA
$R_{th(j-l)}$	Thermal Resistance Junction-Leads for DC			25				°C/W
$R_{th(j-a)}$	Thermal Resistance Junction-Amb for DC	$S^{(1)}$ = 5 cm^2		60				°C/W

(1) S: Cooper surface under tab.

Part Number Information

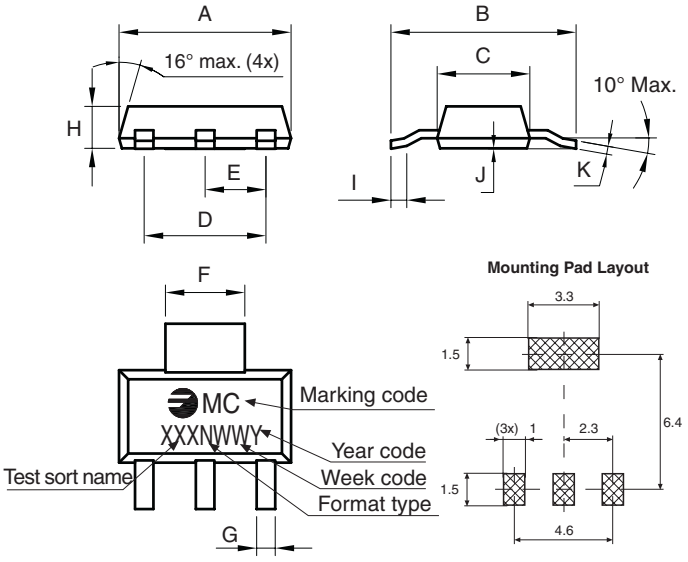


SENSITIVE GATE SCR

Ordering information

PREFERRED P/N	PACKAGE CODE	DELIVERY MODE	BASE QUANTITY	UNIT WEIGHT (g)
FS0202DN 00RS	RS	REEL	1,000	0.116
FS0202DN 00RB	RB	REEL	2,500	0.116

Package Outline Dimensions: (mm) TO-261AA (SOT-223)



REF.	DIMENSIONS		
	Milimeters		
	Min.	Nominal	Max.
A	6.30	6.50	6.70
B	6.70	7.00	7.30
C	3.30	3.50	3.70
D	-	4.60	-
E	-	2.30	-
F	2.95	3.00	3.15
G	0.65	0.70	0.85
H	1.50	1.60	1.70
I	0.50	0.60	0.70
J	-	0.02	0.05
K	0.25	0.30	0.35

Ratings and Characteristics (Ta 25 ºC unless otherwise noted)

Fig. 1: Maximum average power dissipation versus average on-state current

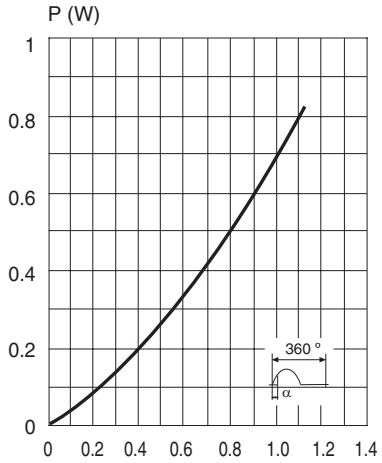


Fig. 2: Average and D.C. on-state current versus case temperature

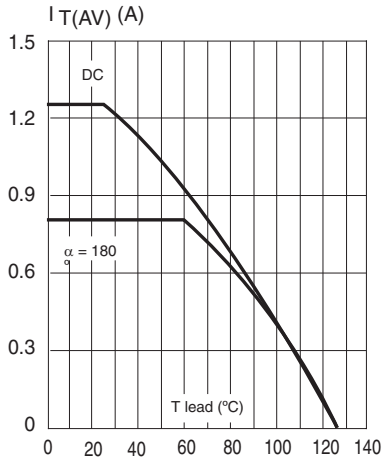


Fig. 3: Relative variation of thermal impedance junction to case versus pulse duration

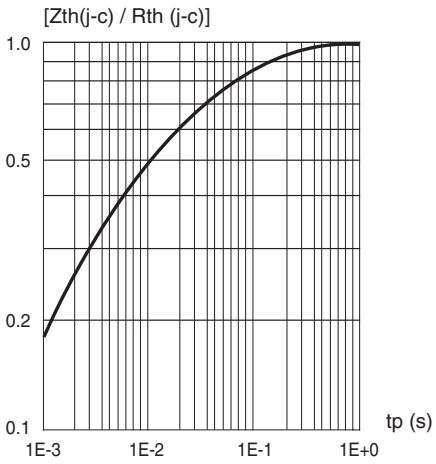


Fig. 4: Relative variation of gate trigger current, holding and latching current versus junction temperature

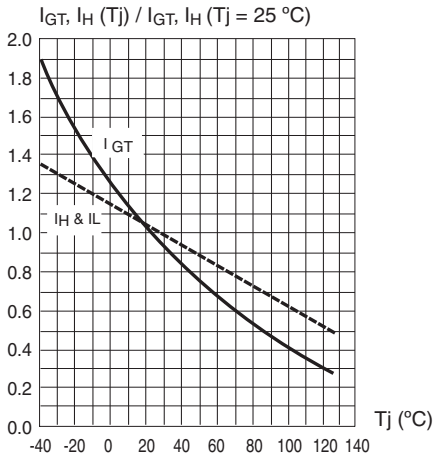


Fig. 5: Relative variation of holding current versus gate-cathode resistance (typical values).

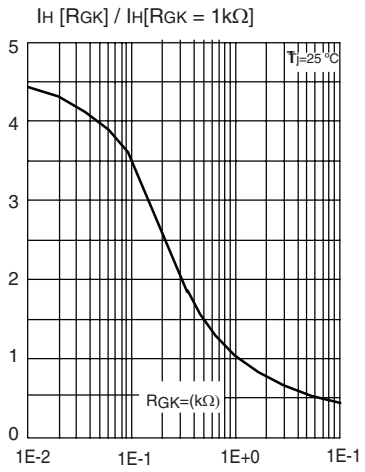


Fig. 6: Relative variation of dV/dt immunity versus gate-cathode resistance (typical values).

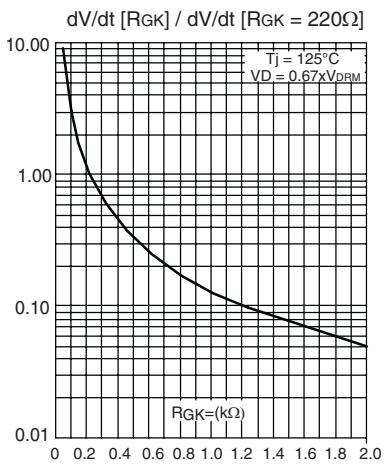


Fig. 7: Relative variation of dV/dt immunity versus gate-cathode capacitance (typical values).

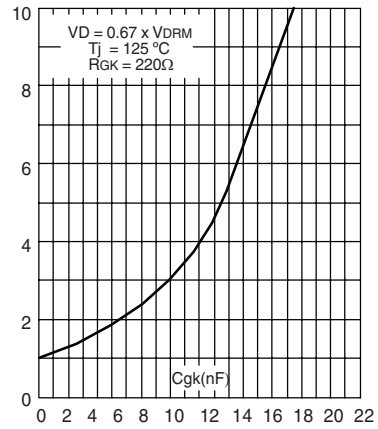


Fig. 8: Non repetitive surge peak on-state current versus number of cycles.

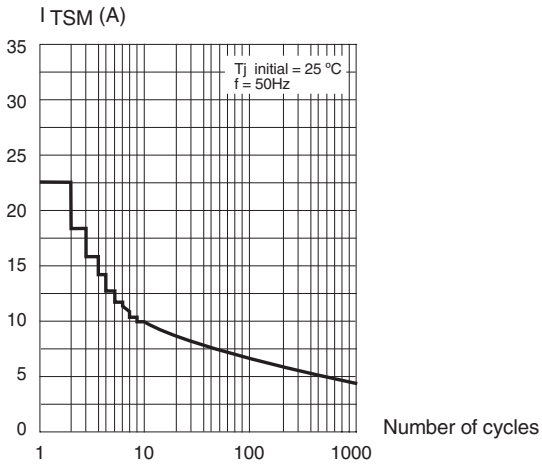


Fig. 9: Non repetitive surge peak on-state current for a sinusoidal pulse with width: tp < 10 ms, and corresponding value of I^2t.

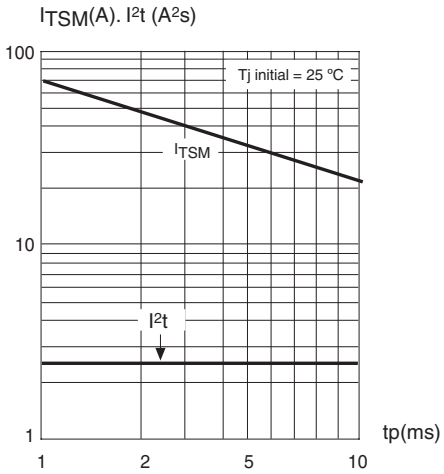
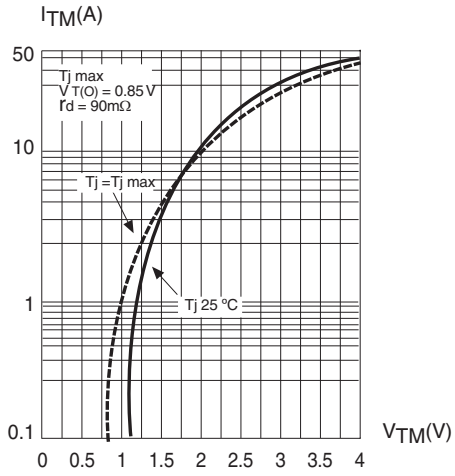


Fig. 10: On-state characteristics (maximum values)



Revision History

Date	Revision	Description of Changes
14-Sep-2011	0	Original Data Sheet
27-May-2013	1	200V and 700V eliminated

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