

# NSBC114EDXV6T1, NSBC114EDXV6T5

## Dual Bias Resistor Transistors

### NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. These digital transistors are designed to replace a single device and its external resistor bias network. The BRT eliminates these individual components by integrating them into a single device. In the NSBC114EDXV6T1 series, two BRT devices are housed in the SOT-563 package which is ideal for low power surface mount applications where board space is at a premium.

#### Features

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- Lead-Free Solder Plating
- These are Pb-Free Devices
- NSV Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable

#### MAXIMUM RATINGS

( $T_A = 25^\circ\text{C}$  unless otherwise noted, common for  $Q_1$  and  $Q_2$ )

Rating	Symbol	Value	Unit
Collector-Base Voltage	$V_{CBO}$	50	Vdc
Collector-Emitter Voltage	$V_{CEO}$	50	Vdc
Collector Current	$I_C$	100	mAdc

#### THERMAL CHARACTERISTICS

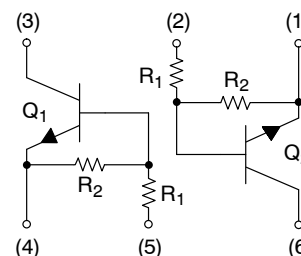
Characteristic (One Junction Heated)	Symbol	Max	Unit
Total Device Dissipation; $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	357 (Note 1) 2.9 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	350 (Note 1)	$^\circ\text{C}/\text{W}$
Characteristic (Both Junctions Heated)	Symbol	Max	Unit
Total Device Dissipation; $T_A = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	500 (Note 1) 4.0 (Note 1)	mW mW/ $^\circ\text{C}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	250 (Note 1)	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 to +150	$^\circ\text{C}$

1. FR-4 @ Minimum Pad



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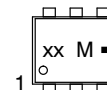


NSBC114EDXV6T1

#### MARKING DIAGRAM



SOT-563  
CASE 463A



- xx = Device Code (Refer to Page 2)
- M = Date Code
- = Pb-Free Package

#### ORDERING INFORMATION

Device	Package	Shipping†
NSBC1xxxDXV6T1	SOT-563	4000/Tape & Reel
NSBC1xxxDXV6T1G	SOT-563	4000/Tape & Reel
NSVBC1xxxDXV6T1G	SOT-563	4000/Tape & Reel
NSBC1xxxDXV6T5	SOT-563	8000/Tape & Reel
NSBC1xxxDXV6T5G	SOT-563	8000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

#### DEVICE MARKING INFORMATION

See specific marking information in the device marking table on page 2 of this data sheet.

# NSBC114EDXV6T1, NSBC114EDXV6T5

## DEVICE MARKING, ORDERING, AND RESISTOR VALUES

Device†	Package*	Marking	R1 (kΩ)	R2 (kΩ)
NSBC114EDXV6T1	SOT-563	7A	10	10
NSBC124EDXV6T1 / NSVBC124EDXV6T1G	SOT-563	7B	22	22
NSBC144EDXV6T1	SOT-563	7C	47	47
NSBC114YDXV6T1	SOT-563	7D	10	47
NSBC114TDXV6T1 (Note 2)	SOT-563	7E	10	∞
NSBC143TDXV6T1 (Notes 2)	SOT-563	7F	4.7	∞
NSBC113EDXV6T1 (Note 2)	SOT-563	7G	1.0	1.0
NSBC123EDXV6T1 (Notes 2)	SOT-563	7H	2.2	2.2
NSBC143EDXV6T1 (Notes 2)	SOT-563	7J	4.7	4.7
NSBC143ZDXV6T1 (Notes 2)	SOT-563	7K	4.7	47
NSBC124XDXV6T1 (Notes 2)	SOT-563	7L	22	47
NSBC123JDXV6T1 (Note 2)	SOT-563	7M	2.2	47
NSBC115EDXV6T1 (Notes 2)	SOT-563	7N	100	100
NSBC144WDXV6T1 (Notes 2)	SOT-563	7P	47	22

†The "G" suffix indicates Pb-Free package available.

\*This package is inherently Pb-Free.

2. New resistor combinations. Updated curves to follow in subsequent data sheets.

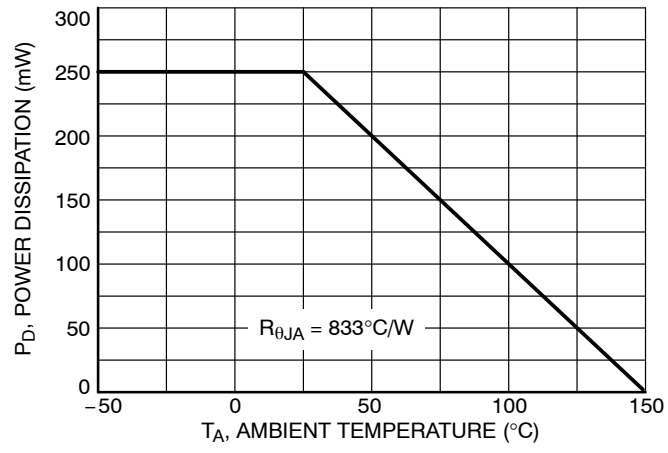
## ELECTRICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ unless otherwise noted, common for $Q_1$ and $Q_2$ )

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector-Base Cutoff Current ( $V_{CB} = 50\text{ V}$ , $I_E = 0$ )	$I_{CBO}$	-	-	100	nAdc
Collector-Emitter Cutoff Current ( $V_{CE} = 50\text{ V}$ , $I_B = 0$ )	$I_{CEO}$	-	-	500	nAdc
Emitter-Base Cutoff Current ( $V_{EB} = 6.0\text{ V}$ , $I_C = 0$ )	$I_{EBO}$	-	-	0.5	mAdc
	NSBC114EDXV6T1	-	-	0.2	
	NSBC124EDXV6T1 / NSVBC124EDXV6T1G	-	-	0.1	
	NSBC144EDXV6T1	-	-	0.2	
	NSBC114YDXV6T1	-	-	0.9	
	NSBC114TDXV6T1	-	-	1.9	
	NSBC143TDXV6T1	-	-	4.3	
	NSBC113EDXV6T1	-	-	2.3	
	NSBC123EDXV6T1	-	-	1.5	
	NSBC143EDXV6T1	-	-	0.18	
	NSBC143ZDXV6T1	-	-	0.13	
	NSBC124XDXV6T1	-	-	0.2	
	NSBC123JDXV6T1	-	-	0.05	
	NSBC115EDXV6T1	-	-	0.13	
	NSBC144WDXV6T1	-	-		
Collector-Base Breakdown Voltage ( $I_C = 10\ \mu\text{A}$ , $I_E = 0$ )	$V_{(BR)CBO}$	50	-	-	Vdc
Collector-Emitter Breakdown Voltage (Note 3) ( $I_C = 2.0\text{ mA}$ , $I_B = 0$ )	$V_{(BR)CEO}$	50	-	-	Vdc

3. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty Cycle < 2.0%



# NSBC114EDXV6T1, NSBC114EDXV6T5



**Figure 1. Derating Curve**

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC114EDXV6T1

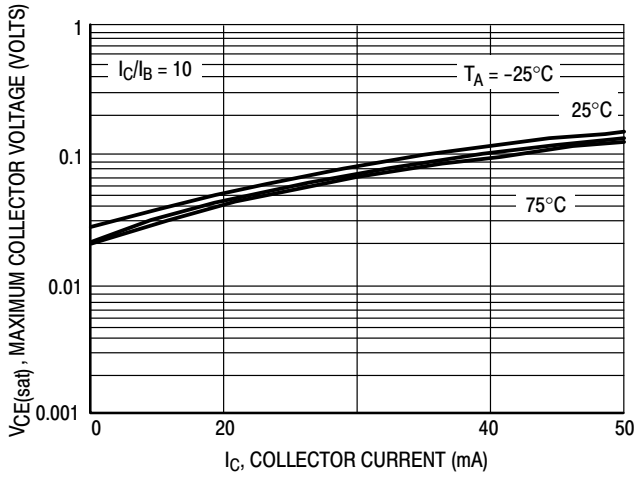


Figure 2.  $V_{CE(sat)}$  versus  $I_C$

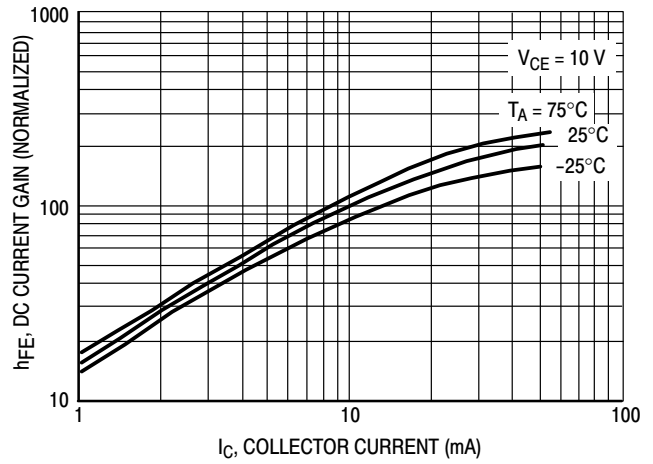


Figure 3. DC Current Gain

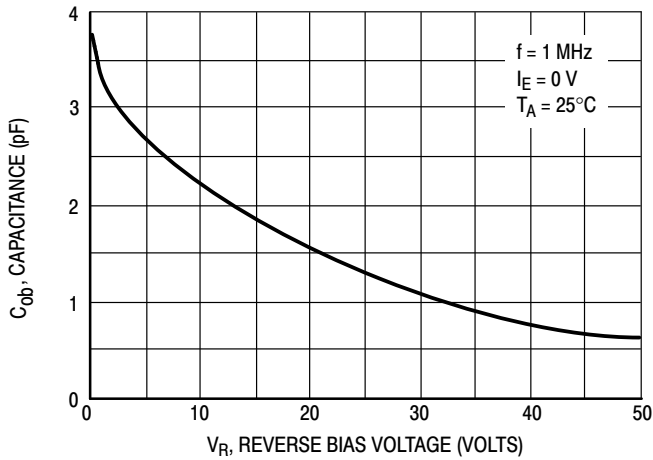


Figure 4. Output Capacitance

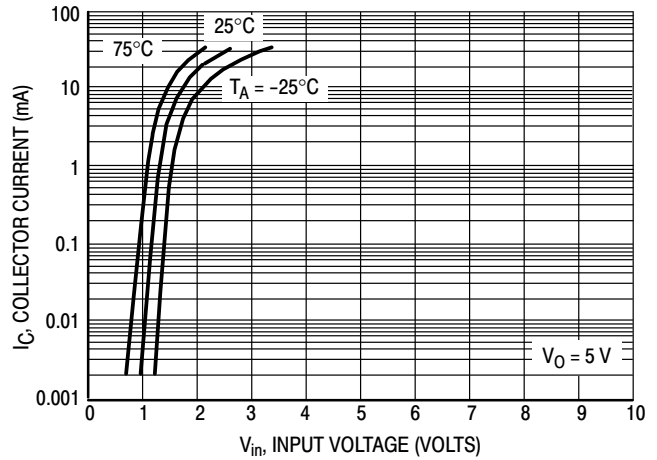


Figure 5. Output Current versus Input Voltage

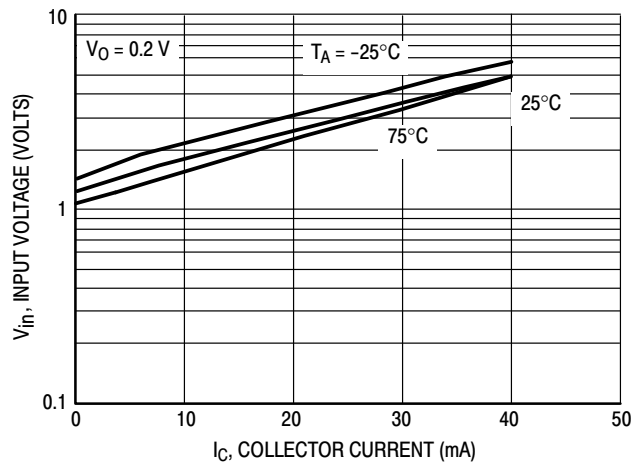


Figure 6. Input Voltage versus Output Current

# NSBC114EDXV6T1, NSBC114EDXV6T5

## TYPICAL ELECTRICAL CHARACTERISTICS — NSBC124EDXV6T1 / NSVBC124EDXV6T1G

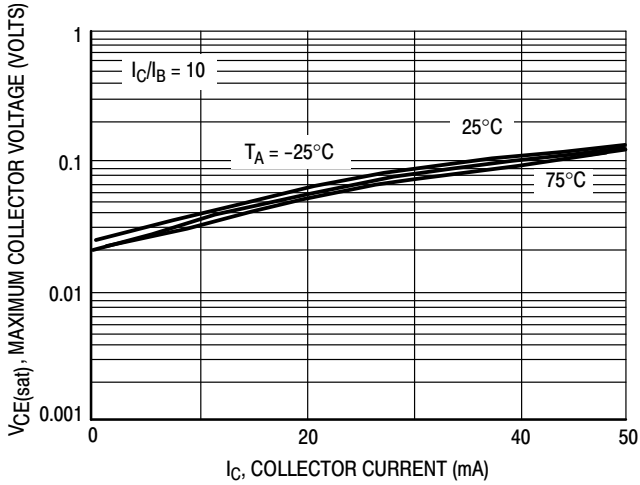


Figure 7.  $V_{CE(sat)}$  versus  $I_C$

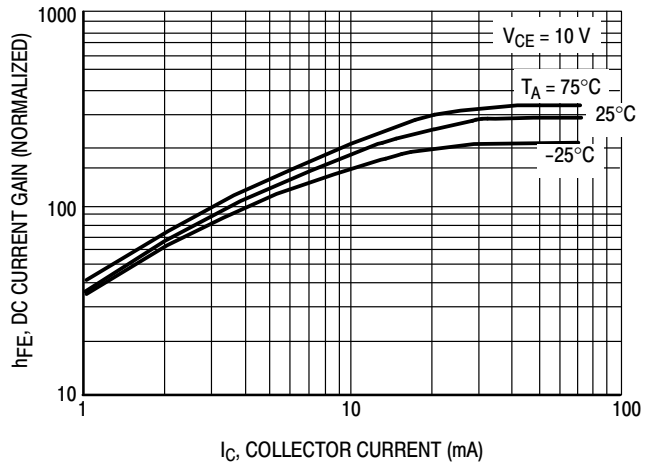


Figure 8. DC Current Gain

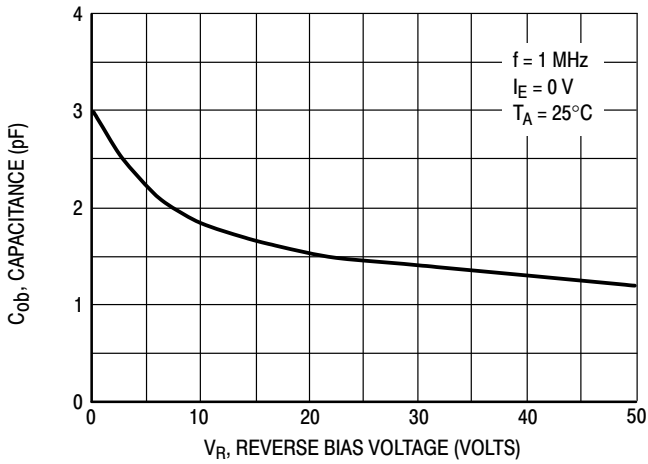


Figure 9. Output Capacitance

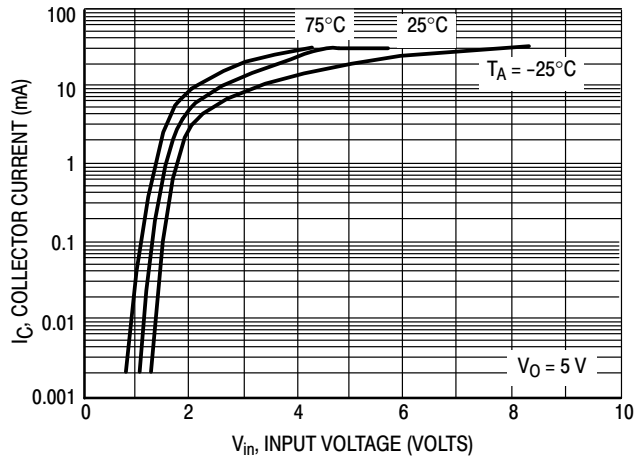


Figure 10. Output Current versus Input Voltage

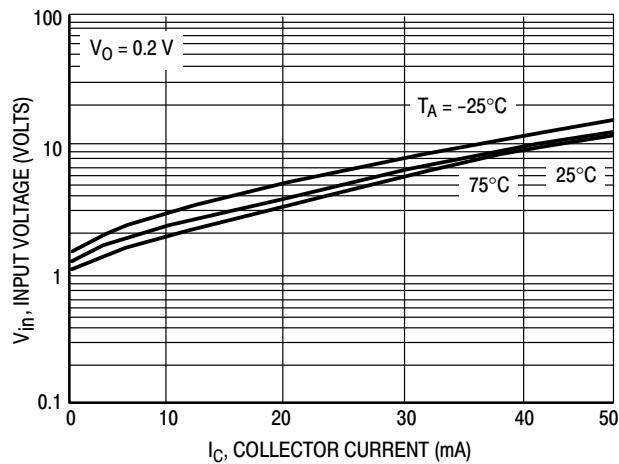


Figure 11. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC144EDXV6T1

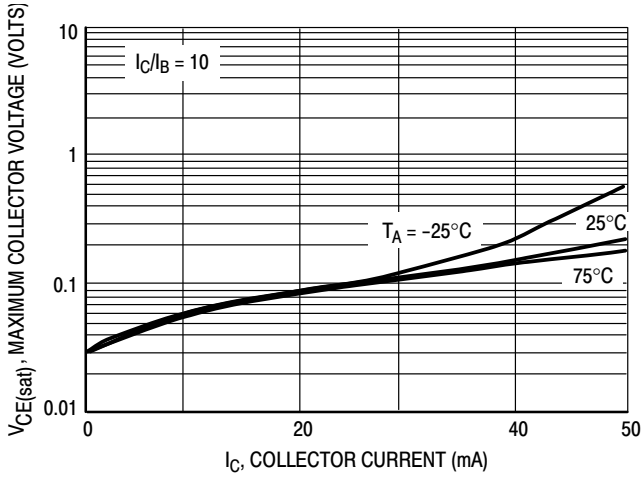


Figure 12.  $V_{CE(sat)}$  versus  $I_C$

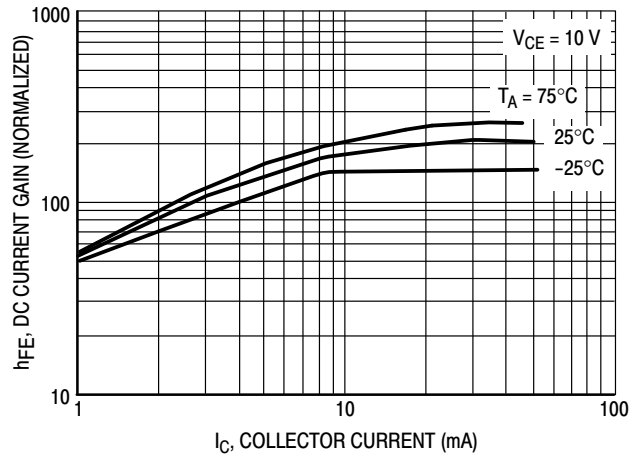


Figure 13. DC Current Gain

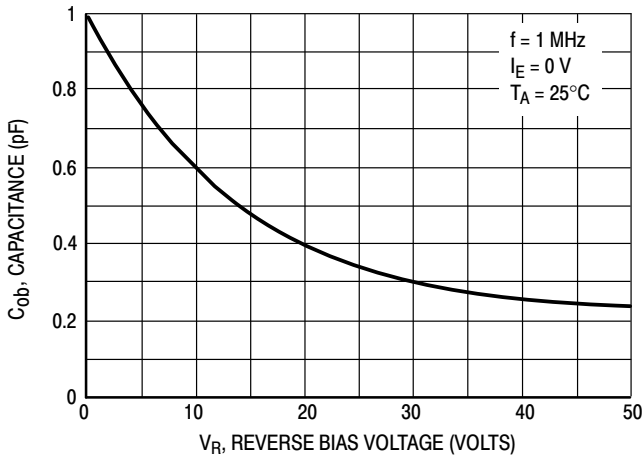


Figure 14. Output Capacitance

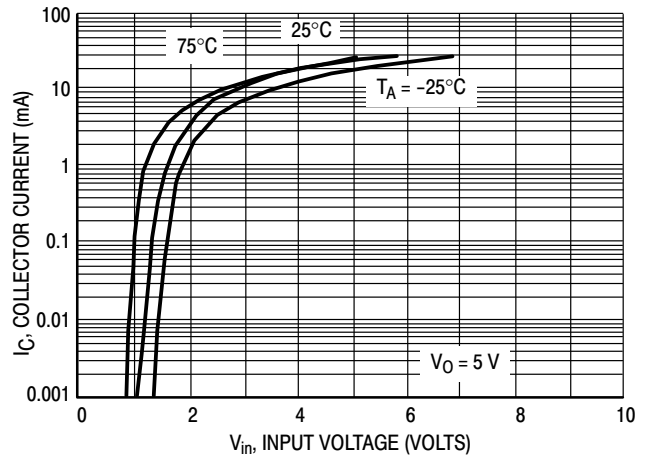


Figure 15. Output Current versus Input Voltage

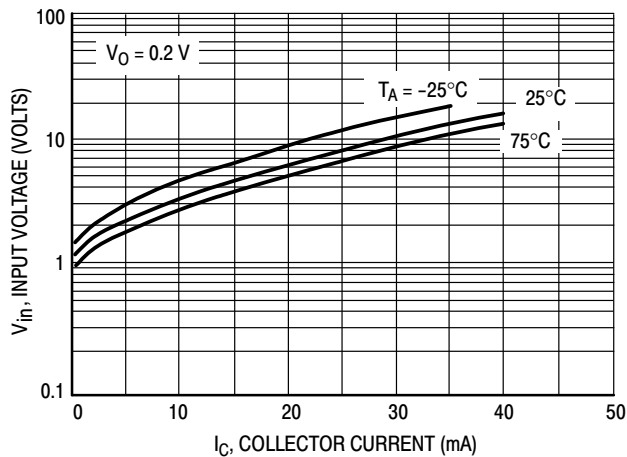


Figure 16. Input Voltage versus Output Current

TYPICAL ELECTRICAL CHARACTERISTICS — NSBC114YDXV6T1

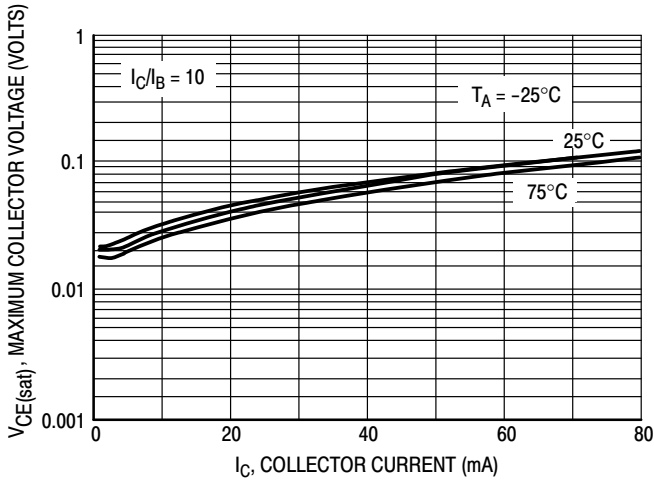


Figure 17.  $V_{CE(sat)}$  versus  $I_C$

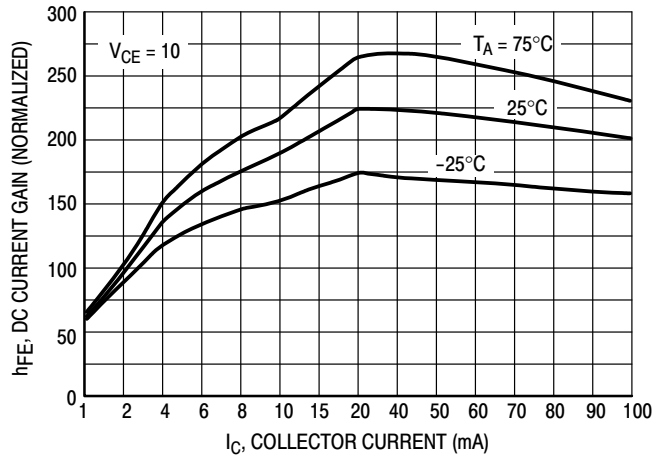


Figure 18. DC Current Gain

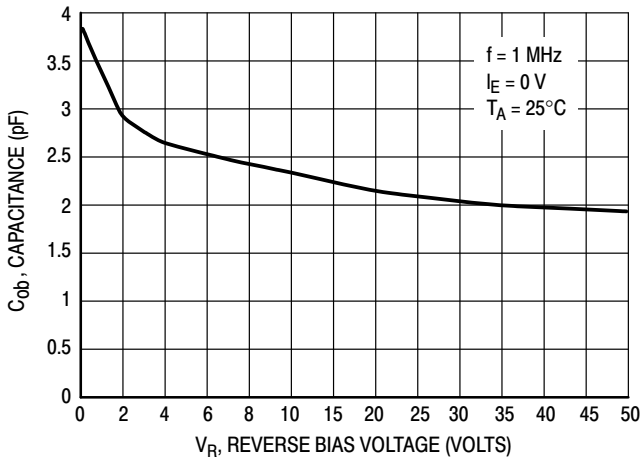


Figure 19. Output Capacitance

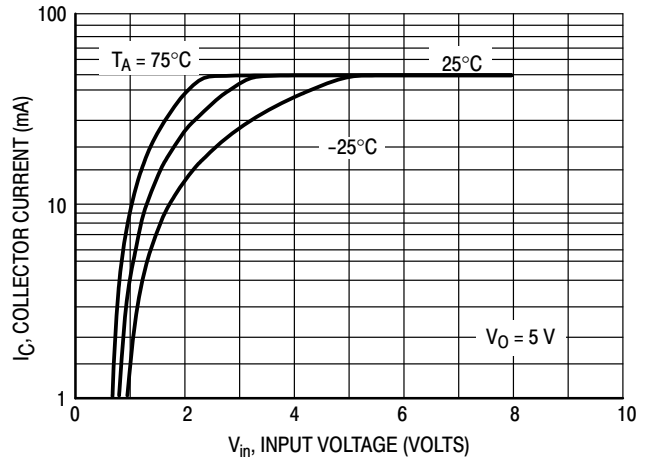


Figure 20. Output Current versus Input Voltage

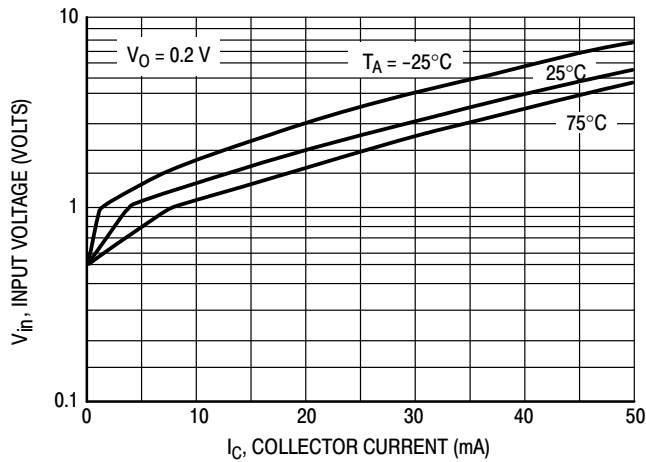


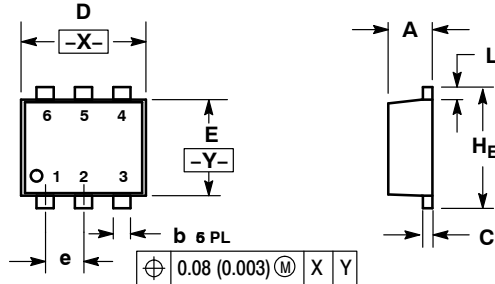
Figure 21. Input Voltage versus Output Current



# NSBC114EDXV6T1, NSBC114EDXV6T5

## PACKAGE DIMENSIONS

SOT-563, 6 LEAD  
CASE 463A  
ISSUE F

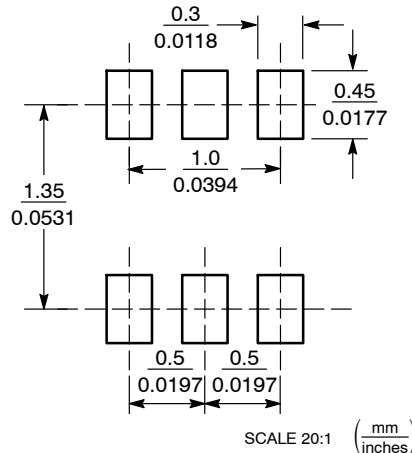


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H <sub>E</sub>	1.50	1.60	1.70	0.059	0.062	0.066

### SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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