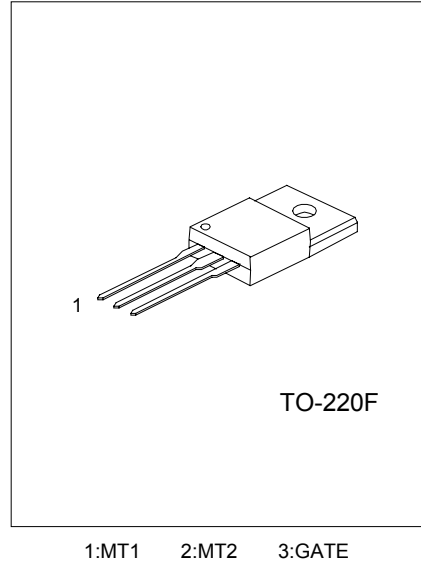
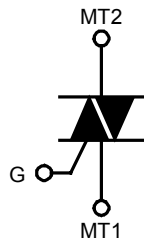


TRIACS

DESCRIPTION

Glass passivated , sensitive gate triacs in a full plastic envelope, intended for use in general purpose bidirectional switching and phase control applications, where high sensitivity is required in all four quadrants.

SYMBOL



ABSOLUTE MAXIMUM RATINGS ( T<sub>j</sub>=25°C)

PARAMETER	SYMBOL	RATING	UNIT
Repetitive Peak Off-State Voltages UT138FE-5 UT138FE-6 UT138FE-8	V <sub>DRM</sub>	500* 600* 800	V
RMS On-state Current (Full sine wave; T <sub>hs</sub> ≤ 56°C)	I <sub>T(RMS)</sub>	12	A
Non-repetitive Peak. On-State Current (Full sine wave, T <sub>j</sub> =125°C prior to surge, with reapplied V <sub>DRM(max)</sub> )	I <sub>TSM</sub>	90 100	A
		t=20ms t=16.7ms	
I <sup>2</sup> t For Fusing (t=10ms)	I <sup>2</sup> t	40	A <sup>2</sup> s
Repetitive Rate of Rise of On-state Current after Triggering (I <sub>TM</sub> =20A, I <sub>G</sub> =0.2A, dI <sub>G</sub> /dt=0.2A/μs)	dI <sub>T</sub> /dt	50 50 50 10	A/μs
		T2+ G+ T2+ G- T2- G- T2- G+	
Peak Gate Voltage	V <sub>GM</sub>	5	V
Peak Gate Current	I <sub>GM</sub>	2	A
Peak Gate Power	P <sub>GM</sub>	5	W
Average Gate Power (over any 20 ms period)	P <sub>G(AV)</sub>	0.5	W
Operating Junction Temperature	T <sub>j</sub>	125	°C
Storage Temperature	T <sub>stg</sub>	-40~150	°C

\*Although not recommended, off-state voltages up to 800V may be applied without damage, but the triac may switch to the on-state. The rate of rise of current should not exceed 15A/μs.

ISOLATION LIMITING VALUE & CHARACTERISTIC ( $T_{HS}=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Repetitive peak voltage from all three terminals to external heatsink (R.H. $\leq 65\%$ , clean and dustfree)	Visol			1500	V
Capacitance from MT2 to external heatsink (f=1MHz)	Cisol		12		pF

## THERMAL RESISTANCES

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Thermal Resistance, Junction to heatsink (full or half cycle) with heatsink compound without heatsink compound	Rthj-hs			4.0 5.5	K/W
Thermal Resistance, Junction to Ambient In free air	Rthj-a		55		K/W

STATIC CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Gate Trigger Current	IGT	$V_D=12\text{V}$ , $I_T=0.1\text{A}$ T2+ G+ T2+ G- T2- G- T2- G+		2.5 4.0 5.0 11	10 10 10 25	mA
Latching Current	IL	$V_D=12\text{V}$ , $I_{GT}=0.1\text{A}$ T2+ G+ T2+ G- T2- G- T2- G+		3.2 16 4.0 5.5	30 40 30 40	mA
Holding Current	IH	$V_D=12\text{V}$ , $I_{GT}=0.1\text{A}$		4.0	30	mA
On-State Voltage	$V_T$	$I_T=15\text{A}$		1.4	1.65	V
Gate Trigger Voltage	$V_{GT}$	$V_D=12\text{V}$ , $I_T=0.1\text{A}$ $V_D=400\text{V}$ , $I_T=0.1\text{A}$ , $T_J=125^{\circ}\text{C}$	0.25	0.7	1.5	V
Off-state Leakage Current	$I_D$	$V_D=V_{DRM(max)}$ , $T_J=125^{\circ}\text{C}$		0.1	0.5	mA

DYNAMIC CHARACTERISTICS ( $T_J=25^{\circ}\text{C}$ , unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Critical Rate Of Rise Of Off-State Voltage	$dV_D/dt$	$V_{DM}=67\% V_{DRM(max)}$ , $T_J=125^{\circ}\text{C}$ Exponential waveform, Gate open circuit		50		V/ $\mu\text{s}$
Gate Controlled Turn-on Time	tgt	$I_{TM}=16\text{A}$ , $V_D=V_{DRM(max)}$ , $I_G=0.1\text{A}$ , $dI_G/dt=5\text{A}/\mu\text{s}$		2		$\mu\text{s}$

TYPICAL CHARACTERISTICS

Figure 1. Maximum on-state Dissipation,  $P_{tot}$  vs rms On-state Current,  $I_T(RMS)$ , Where  $\alpha$  = conduction Angle.

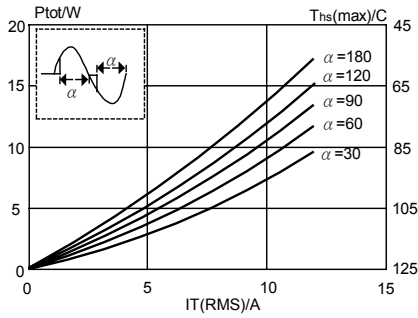


Figure 4. Maximum Permissible RMS Current  $I_T(RMS)$  vs heatsink Temperature  $T_{hs}$

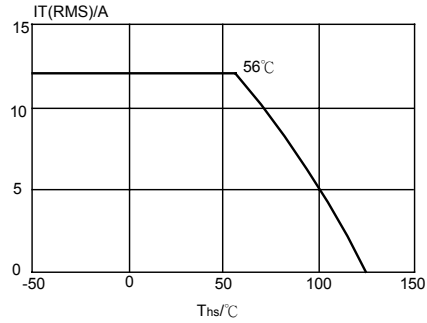


Figure 2. Maximum Permissible Non-repetitive Peak On-state Current  $I_{TSM}$ , vs Pulse Width  $t_p$ , for Sinusoidal Currents,  $t_p \leq 20ms$

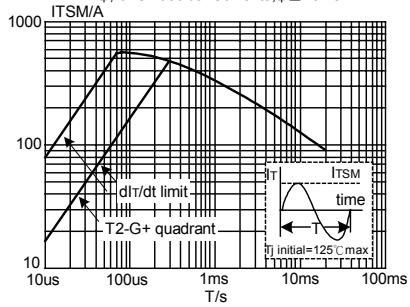


Figure 5. Maximum Permissible Repetitive rms on-state Current  $I_T(RMS)$ , vs Surge Duration, for Sinusoidal Currents,  $f=50Hz; T_{hs} \leq 56^\circ C$

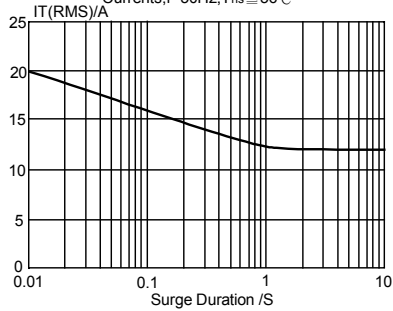


Figure 3. Maximum Permissible Non-Repetitive peak on-state Current  $I_{TSM}$ , vs Number of Cycles, for Sinusoidal Currents,  $f=50Hz$

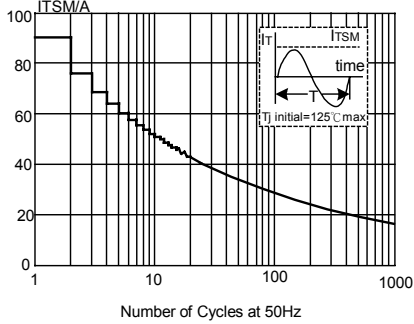
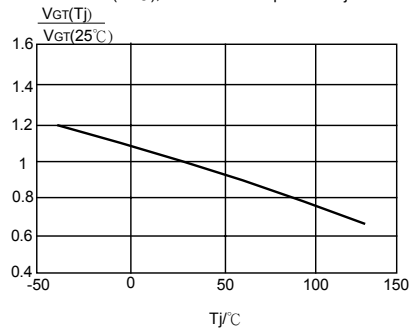
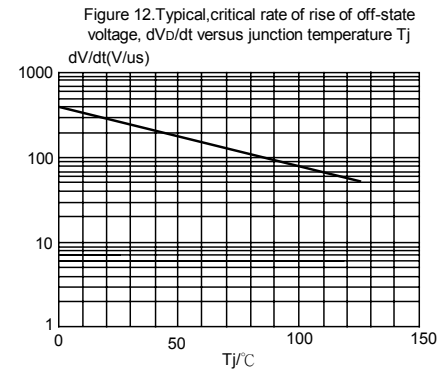
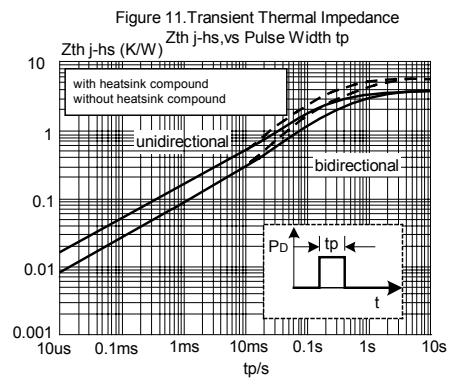
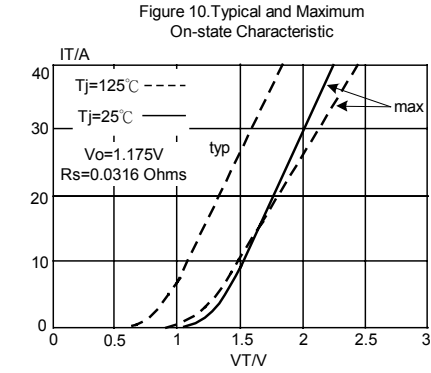
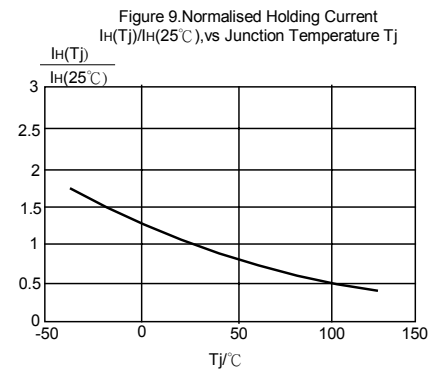
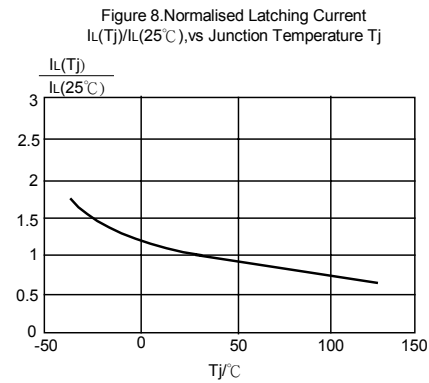
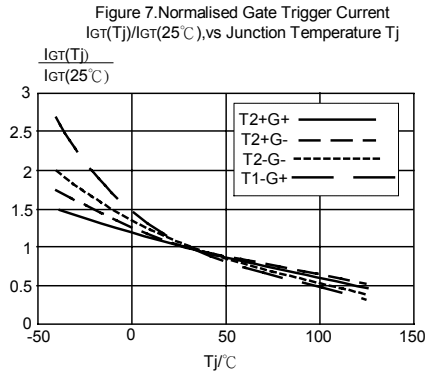


Figure 6. Normalised Gate Trigger Voltage  $V_{GT}(T_j)/V_{GT}(25^\circ C)$ , vs Junction Temperature  $T_j$





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