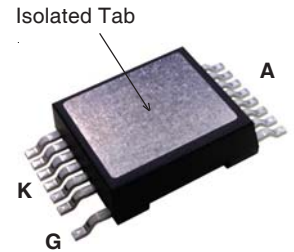
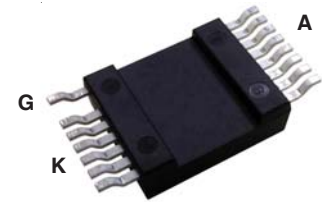


# 1500V MOS Gated Thyristor

## MMJX1H40N150

$$V_{DM} = 1500V$$

(Electrically Isolated Tab)



Symbol	Test Conditions	Maximum Ratings	
$V_{DM}$	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	1500	V
$V_{GK}$	Continuous	$\pm 30$	V
$V_{GK}$	Transient	$\pm 40$	V
$I_{TSM}$	$T_C = 25^\circ\text{C}, 1\mu\text{s}$	15.5	kA
	$T_C = 25^\circ\text{C}, 10\mu\text{s}$	6.4	kA
$P_D$	$T_C = 25^\circ\text{C}$	320	W
$T_J$		-55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		-55 ... +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062 in.) from Case for 10s	260	$^\circ\text{C}$
$V_{ISOL}$	50/60Hz, 1 minute	2500	V~
$F_C$	Mounting Force	50..200/11..45	N/lb
<b>Weight</b>		5	g

G = Gate                      K = Cathode  
A = Anode

### Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 2500V~ Electrical Isolation
- Very High Current Capability

### Advantages

- High Power Density
- Low Gate Drive Requirement

### Applications

- Capacitive Discharge Circuits
- Ignition Circuits
- Solid State Surge Protection

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{BR}$	$I_A = 250\mu\text{A}, V_{GK} = 0V$	1500		V
$V_{GK(th)}$	$I_A = 250\mu\text{A}, V_{AK} = V_{GK}$	2.5		5.0 V
$V_T$	$I_T = 1000A, V_{GK} = 15V$		4.75	6.0 V
$r_T$	$I_T > I_L, V_{GK} = 15V$		1.20	m $\Omega$
$V_{BO}$	$V_{GK} = 15V$		5.25	V
$I_D$	$V_{AK} = 1500V, V_{GK} = 0V$ $T_J = 125^\circ\text{C}$			15 $\mu\text{A}$
				1.5 mA
$I_L$			250	A
$I_H$			200	A
$I_{GKS}$	$V_{AK} = 0V, V_{GK} = \pm 30V$			$\pm 200$ nA

Symbol Test Conditions ( $T_J = 25^\circ\text{C}$ Unless Otherwise Specified)	Characteristic Values		
	Min.	Typ.	Max.
$C_{iks}$ $C_{oks}$ $C_{rks}$	$V_{AK} = 25\text{V}, V_{GK} = 0\text{V}, f = 1\text{MHz}$	2825	pF
		164	pF
		50	pF
$Q_{g(on)}$ $Q_{gk}$ $Q_{ga}$	$I_C = 40\text{A}, V_{GK} = 15\text{V}, V_{AK} = 600\text{V}$	99	nC
		22	nC
		36	nC
$t_{ri}$ $t_d$	<b>Capacitive Discharge, <math>T_J = 25^\circ\text{C}</math></b> $I_A = 2000\text{A}, V_{GK} = 15\text{V}, R_G = 1\Omega$ $V_{AK} = 1000\text{V}, L < 20\text{nH}, \text{Notes 2 \& 3}$	100	ns
		50	ns
$t_{ri}$ $t_d$	<b>Capacitive Discharge, <math>T_J = 125^\circ\text{C}</math></b> $I_A = 2000\text{A}, V_{GK} = 15\text{V}, R_G = 1\Omega$ $V_{AK} = 1000\text{V}, L < 20\text{nH}, \text{Notes 2 \& 3}$	100	ns
		50	ns
$R_{thJC}$			0.39 $^\circ\text{C/W}$
$R_{thCS}$		0.12	$^\circ\text{C/W}$
$R_{thJA}$		30	$^\circ\text{C/W}$

**Notes:**

1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .
2. It is recommended to use a gate driver capable of supplying more than 4Amps and  $\geq 15\text{V}$  gate voltage.
3. Refer to fig. 8 & 9.

**PRELIMINARY TECHNICAL INFORMATION**

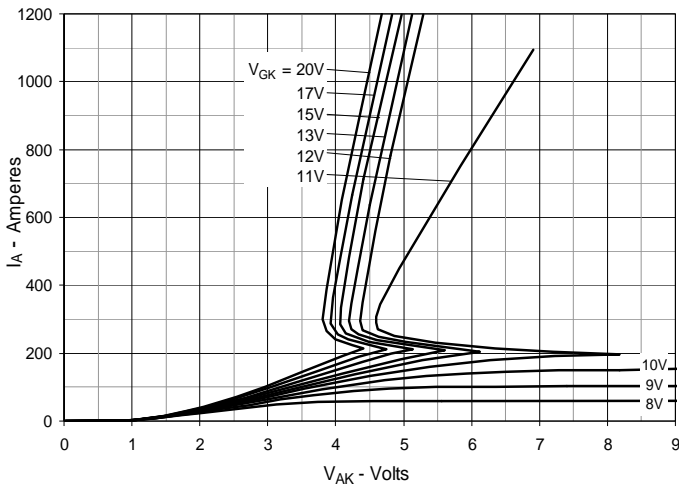
The product presented herein is under development. The Technical Specifications offered are derived from a subjective evaluation of the design, based upon prior knowledge and experience, and constitute a "considered reflection" of the anticipated result. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

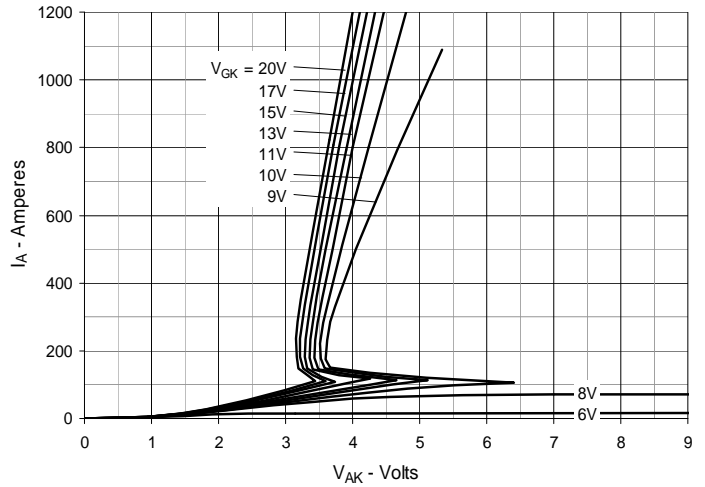
IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

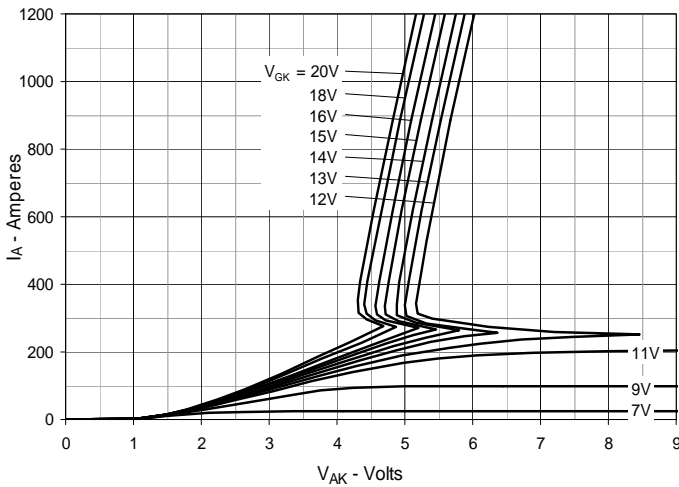
**Fig. 1. Extended Output Characteristics @  $T_J = 25^\circ\text{C}$**



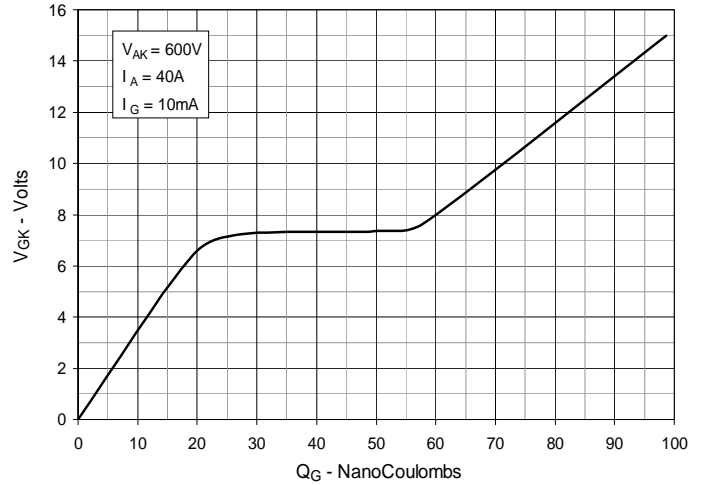
**Fig. 2. Extended Output Characteristics @  $T_J = 125^\circ\text{C}$**



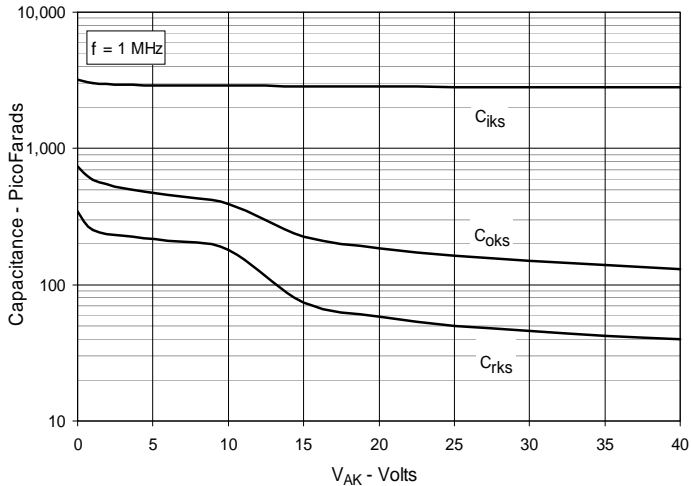
**Fig. 3. Extended Output Characteristics @  $T_J = -40^\circ\text{C}$**



**Fig. 4. Gate Charge**



**Fig. 5. Capacitance**



**Fig. 6. Maximum Transient Thermal Impedance**

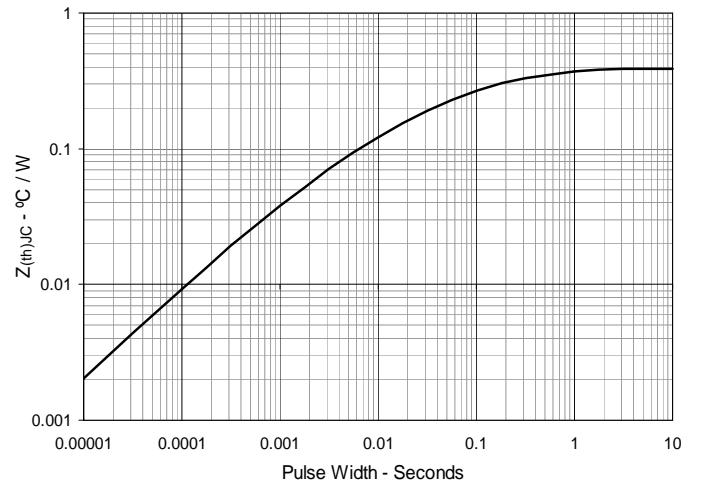
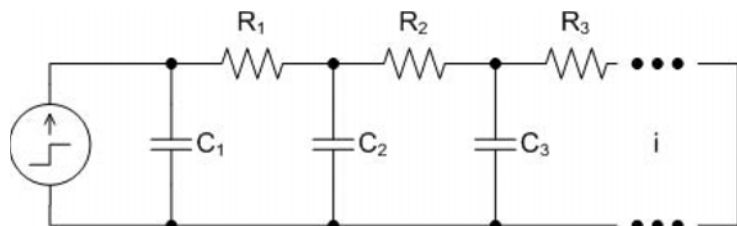


Fig. 7. Cauer Thermal Network



i	Ri ( $\Omega$ )	Ci (F)
1	0.014083	0.0078555
2	0.068078	0.0196550
3	0.133430	0.1199600
4	0.121939	2.5000000

Fig. 8. Capacitive Discharge

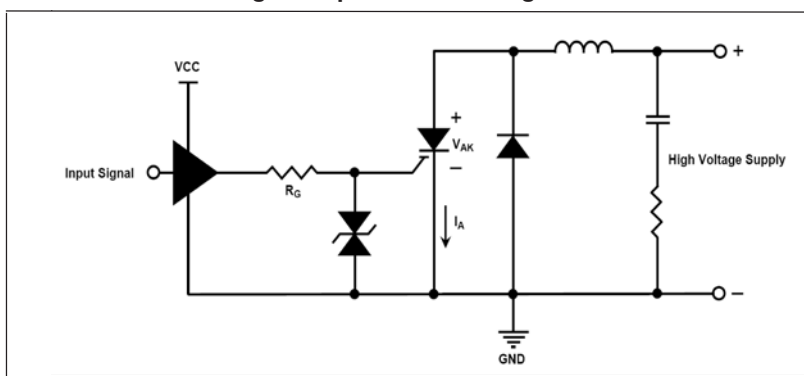
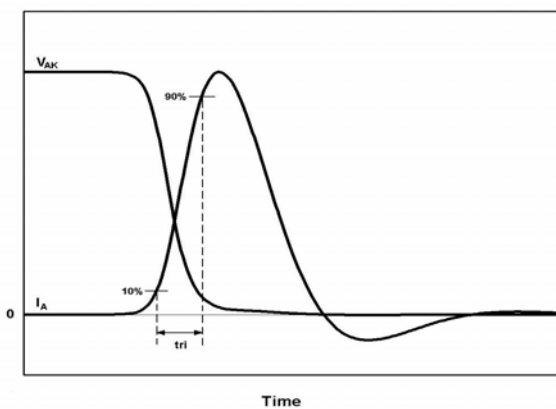
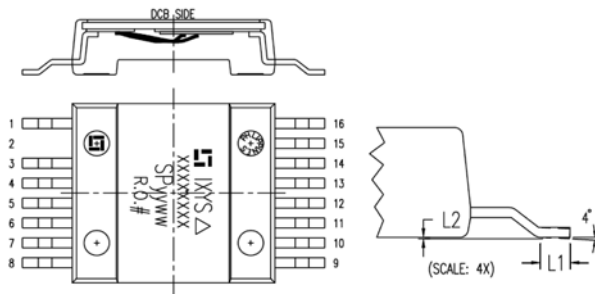
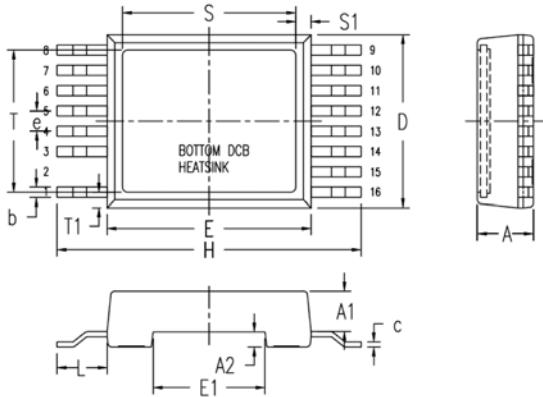


Fig. 9. Capacitive Discharge Waveform





SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.209	.224	5.30	5.70
A1	.154	.161	3.90	4.10
A2	.055	.063	1.40	1.60
b	.035	.045	0.90	1.15
c	.018	.026	0.45	0.65
D	.661	.677	16.80	17.20
E	.780	.795	19.80	20.20
E1	.425	.441	10.80	11.20
e	.079 BSC		2.00 BSC	
H	1.161	1.185	29.50	30.10
L	.181	.209	4.60	5.30
L1	.051	.067	1.30	1.70
L2	.000	.006	0.00	0.15
S	.661	.677	16.80	17.20
S1	.051	.067	1.30	1.70
T	.543	.559	13.80	14.20
T1	.051	.067	1.30	1.70

**NOTE:**

1. ALL LEADS ARE MATTE PURE TIN PLATED.
2. CU SURFACE OF BOTTOM DCB IS PRE-NI PLATED UNLESS OTHERWISE.
3. CU SURFACE OF BOTTOM DCB IS ELECTRICALLY ISOLATED 2,500V AC FROM ALL OTHER LEADS.
4. UNLESS OTHER SPECIFIED, PIN OUT ARE AS FOLLOWS.  
 PIN #1 - GATE  
 PIN #3 - GATE  
 PIN #4 THROUGH #8 - K = Cathode  
 PIN #9 THROUGH #16 - A = Anode