# BTA201-800ER

## 3Q Hi-Com Triac

**11 June 2014** **Product data sheet**

## 1. General description

Planar passivated high commutation three quadrant triac in a SOT54 (TO-92) plastic package. This "series ER" triac balances the requirements of commutation performance and gate sensitivity and is intended for interfacing with low power drivers and logic ICs including microcontrollers. It has reverse pinning to that of the standard triac in this package.

## 2. Features and benefits

- 3Q technology for improved noise immunity
- Direct triggering from low power drivers and logic ICs
- High commutation capability with sensitive gate
- High immunity to false turn-on by dV/dt
- High voltage capability
- Planar passivated for voltage ruggedness and reliability
- Reverse pinning version (ER)
- Sensitive gate for easy logic level triggering
- Triggering in three quadrants only

## 3. Applications

- General purpose motor control
- Small loads in washing machines
- Solenoid drivers

## 4. Quick reference data

**Table 1. Quick reference data**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | - | 800 | V |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)}$ = 25 °C; $t_p$ = 20 ms; Fig. 4; Fig. 5 | | - | - | 12.5 | A |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq$ 54 °C; Fig. 1; Fig. 2; Fig. 3 | | - | - | 1 | A |
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |

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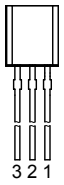
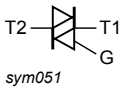
| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |

## 5. Pinning information

**Table 2. Pinning information**

| Pin | Symbol | Description | Simplified outline | Graphic symbol |
|---|---|---|---|---|
| 1 | T1 | main terminal 1 |  TO-92 (SOT54) |  |
| 2 | G | gate | | |
| 3 | T2 | main terminal 2 | | |

## 6. Ordering information

**Table 3. Ordering information**

| Type number | Package | | |
|---|---|---|---|
| | Name | Description | Version |
| BTA201-800ER | TO-92 | plastic single-ended leaded (through hole) package; 3 leads | SOT54 |

# 7. Limiting values

**Table 4. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{DRM}$ | repetitive peak off-state voltage | | | - | 800 | V |
| $I_{T(RMS)}$ | RMS on-state current | full sine wave; $T_{lead} \leq 54$ °C; Fig. 1; Fig. 2; Fig. 3 | | - | 1 | A |
| $I_{TSM}$ | non-repetitive peak on-state current | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 16.8$ ms | | - | 13.7 | A |
| | | full sine wave; $T_{j(init)} = 25$ °C; $t_p = 20$ ms; Fig. 4; Fig. 5 | | - | 12.5 | A |
| $I^2t$ | $I^2t$ for fusing | $t_p = 10$ ms; SIN | | - | 0.78 | $A^2s$ |
| $dI_T/dt$ | rate of rise of on-state current | $I_T$ 1.5 A; $I_G$ 0.2 A; $dI_G/dt = 0.2$ A/µs | | - | 100 | A/µs |
| $I_{GM}$ | peak gate current | | | - | 2 | A |
| $P_{GM}$ | peak gate power | | | - | 5 | W |
| $P_{G(AV)}$ | average gate power | over any 20 ms period | | - | 0.1 | W |
| $T_j$ | junction temperature | | | -40 | 125 | °C |

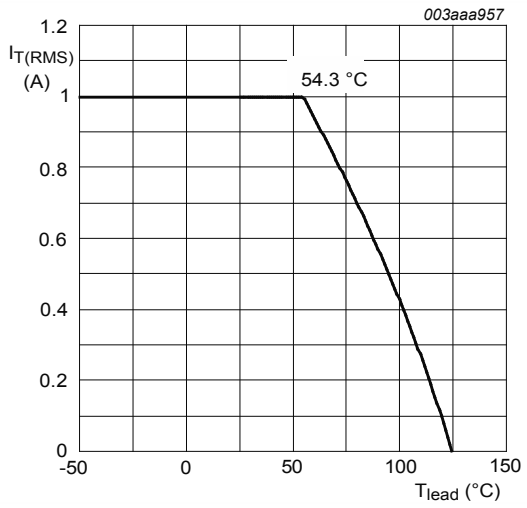
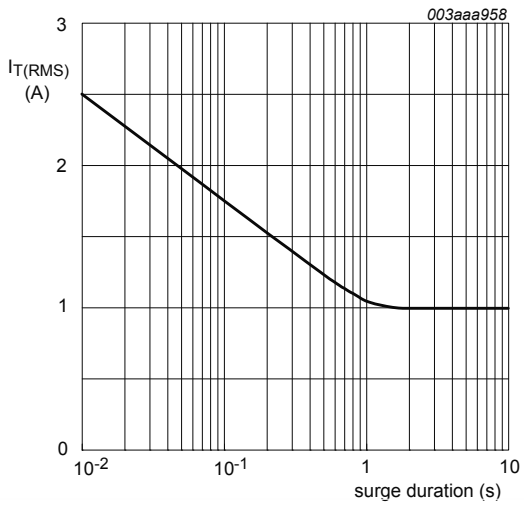
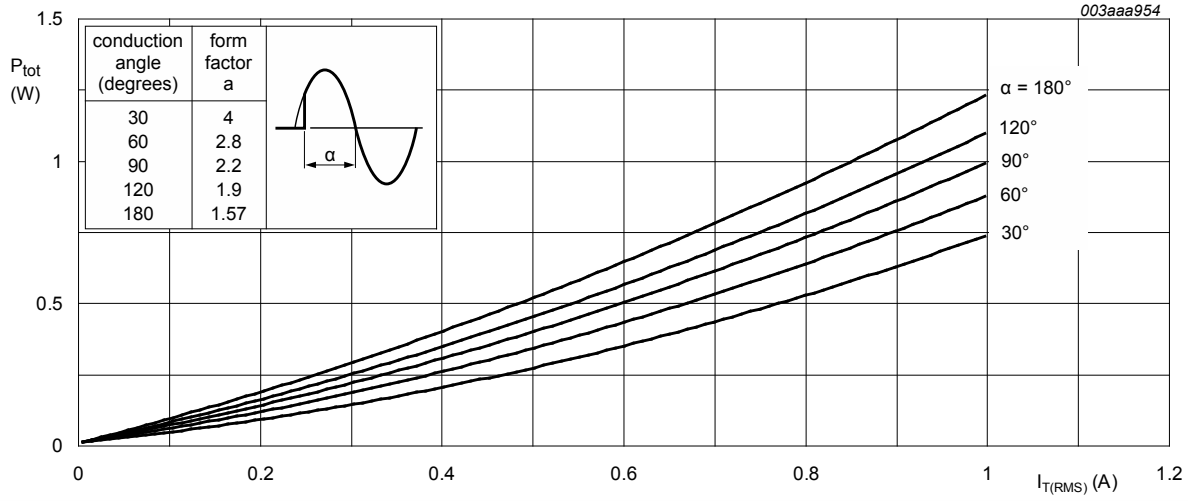



**Fig. 1. RMS on-state current as a function of lead temperature; maximum values**




f = 50 Hz; $T_{lead}$ = 54 °C

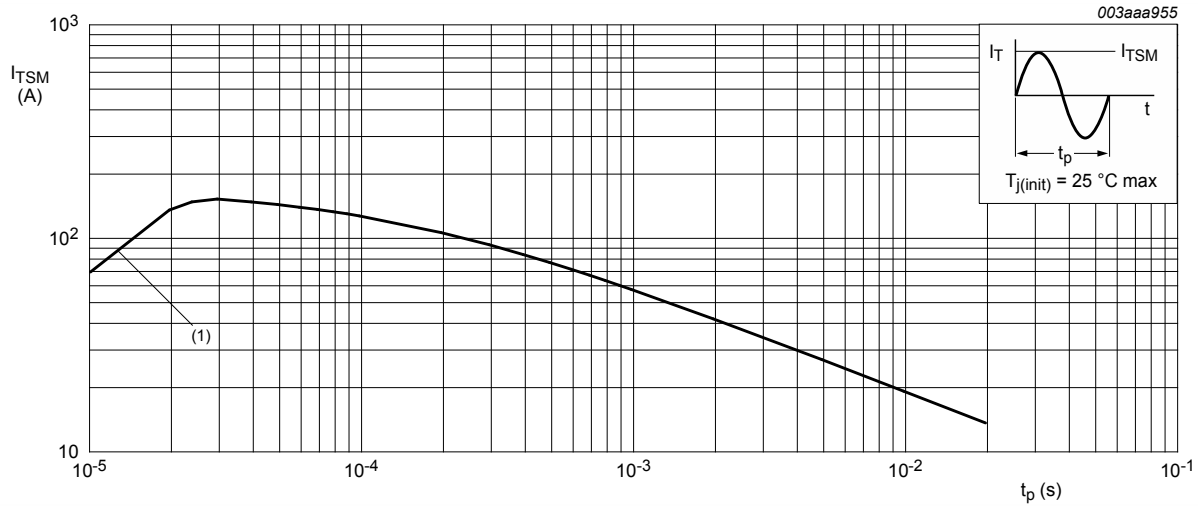
**Fig. 2. RMS on-state current as a function of surge duration; maximum values**




α = conduction angle

a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

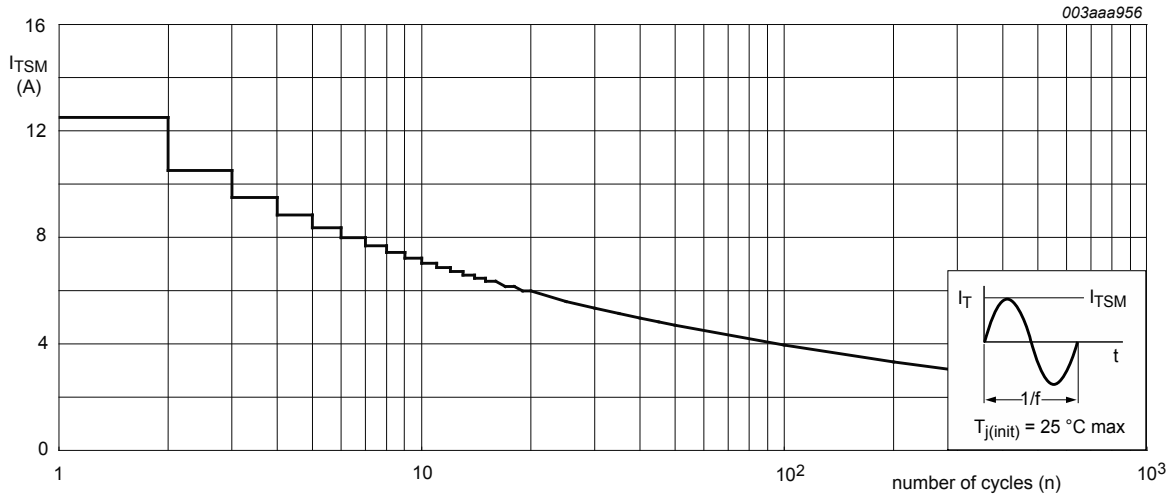
**Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values**




$t_p \leq 20$ ms

(1) $dI_T/dt$ limit

**Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values**



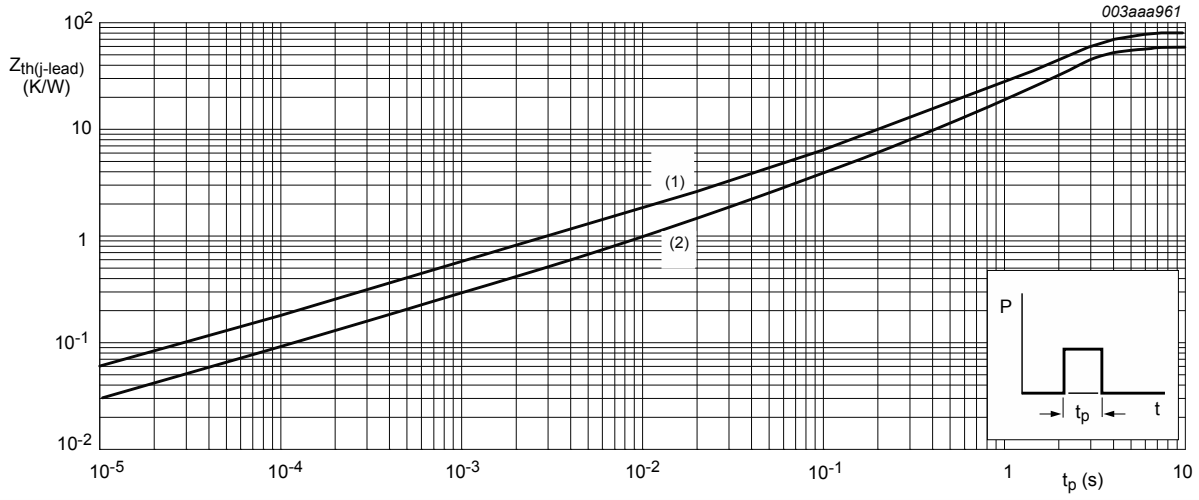

f = 50 Hz

**Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values**

# 8. Thermal characteristics

**Table 5. Thermal characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $R_{th(j\text{-}lead)}$ | thermal resistance from junction to lead | full cycle; Fig. 6 | | - | - | 60 | K/W |
| | | half cycle; Fig. 6 | | - | - | 80 | K/W |
| $R_{th(j\text{-}a)}$ | thermal resistance from junction to ambient | | | - | 150 | - | K/W |



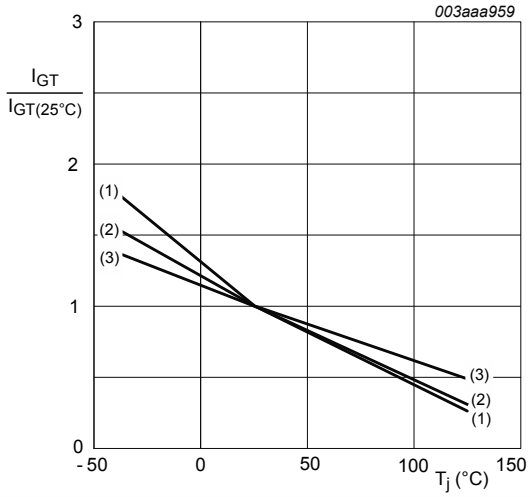

(1) Unidirectional (half cycle)
(2) Bidirectional (full cycle)

**Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width**

# 9. Characteristics

**Table 6. Characteristics**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Static characteristics** | | | | | | | |
| $I_{GT}$ | gate trigger current | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |
| | | $V_D$ = 12 V; $I_T$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 7 | | 1 | - | 10 | mA |
| $I_L$ | latching current | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G+; $T_j$ = 25 °C; Fig. 8 | | - | - | 12 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2+ G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 20 | mA |
| | | $V_D$ = 12 V; $I_G$ = 0.1 A; T2- G-; $T_j$ = 25 °C; Fig. 8 | | - | - | 12 | mA |
| $I_H$ | holding current | $V_D$ = 12 V; $T_j$ = 25 °C; Fig. 9 | | - | - | 12 | mA |
| $V_T$ | on-state voltage | $I_T$ = 1.4 A; $T_j$ = 25 °C; Fig. 10 | | - | 1.2 | 1.5 | V |
| $V_{GT}$ | gate trigger voltage | $V_D$ = 12 V; $I_T$ = 0.1 A; $T_j$ = 25 °C; Fig. 11 | | - | 0.7 | 1 | V |
| | | $V_D$ = 400 V; $I_T$ = 0.1 A; $T_j$ = 125 °C; Fig. 11 | | 0.2 | 0.3 | - | V |
| $I_D$ | off-state current | $V_D$ = 800 V; $T_j$ = 125 °C | | - | 0.1 | 0.5 | mA |
| **Dynamic characteristics** | | | | | | | |
| $dV_D/dt$ | rate of rise of off-state voltage | $V_{DM}$ = 536 V; $T_j$ = 125 °C; ($V_{DM}$ = 67% of $V_{DRM}$); exponential waveform; gate open circuit; Fig. 12 | | 600 | - | - | V/µs |
| $dI_{com}/dt$ | rate of change of commutating current | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 20 V/s; (snubberless condition); gate open circuit | | 2.5 | - | - | A/ms |
| | | $V_D$ = 400 V; $T_j$ = 125 °C; $I_{T(RMS)}$ = 1 A; $dV_{com}/dt$ = 10 V/µs; gate open circuit | | 3.5 | - | - | A/ms |




(1) T2- G-
(2) T2+ G-
(3) T2+ G+

**Fig. 7. Normalized gate trigger current as a function of junction temperature**

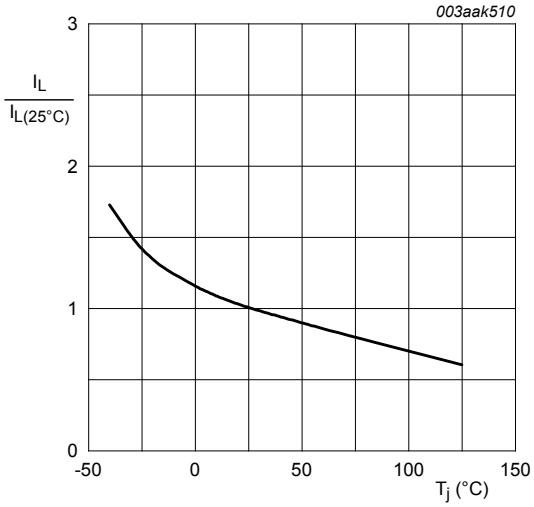



**Fig. 8. Normalized latching current as a function of junction temperature**

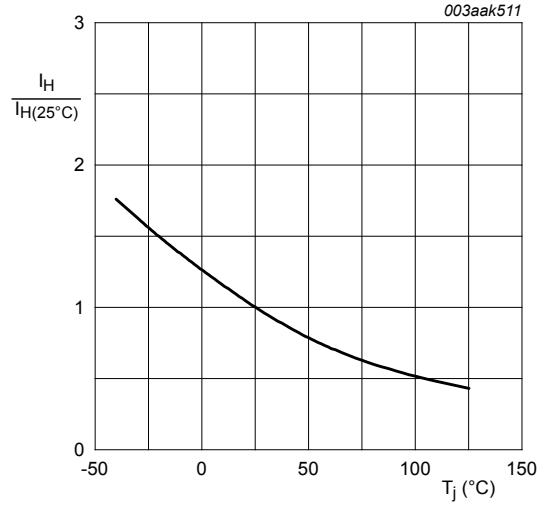
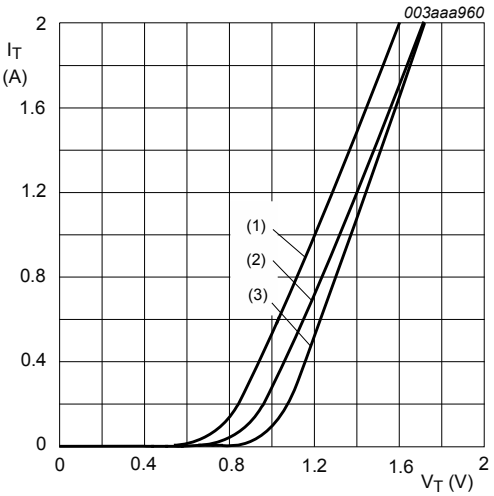



**Fig. 9. Normalized holding current as a function of junction temperature**




$V_o$ = 1.02 V; $R_s$ = 0.358 Ω
(1) $T_j$ = 125 °C; typical values
(2) $T_j$ = 125 °C; maximum values
(3) $T_j$ = 25 °C; maximum values

**Fig. 10. On-state current as a function of on-state voltage**

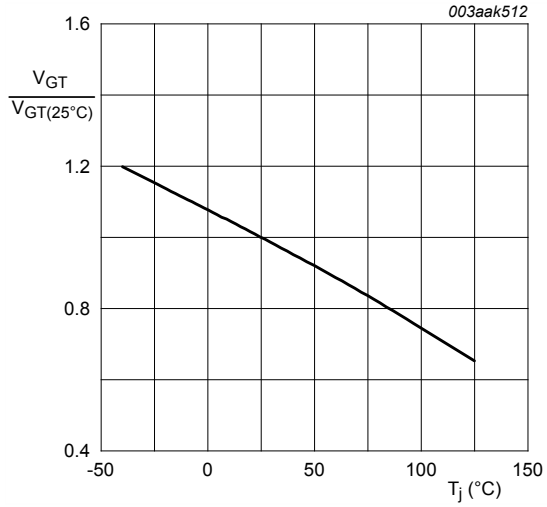



**Fig. 11. Normalized gate trigger voltage as a function of junction temperature**

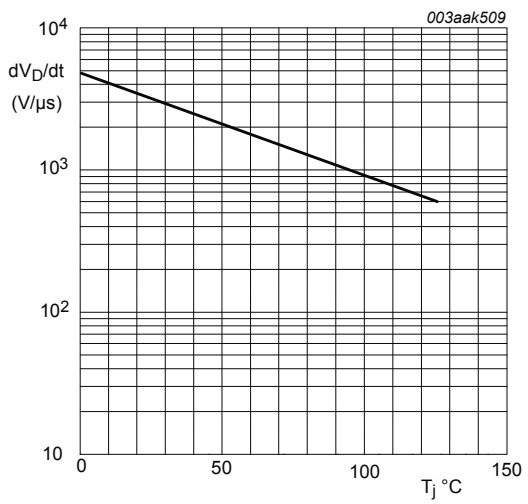
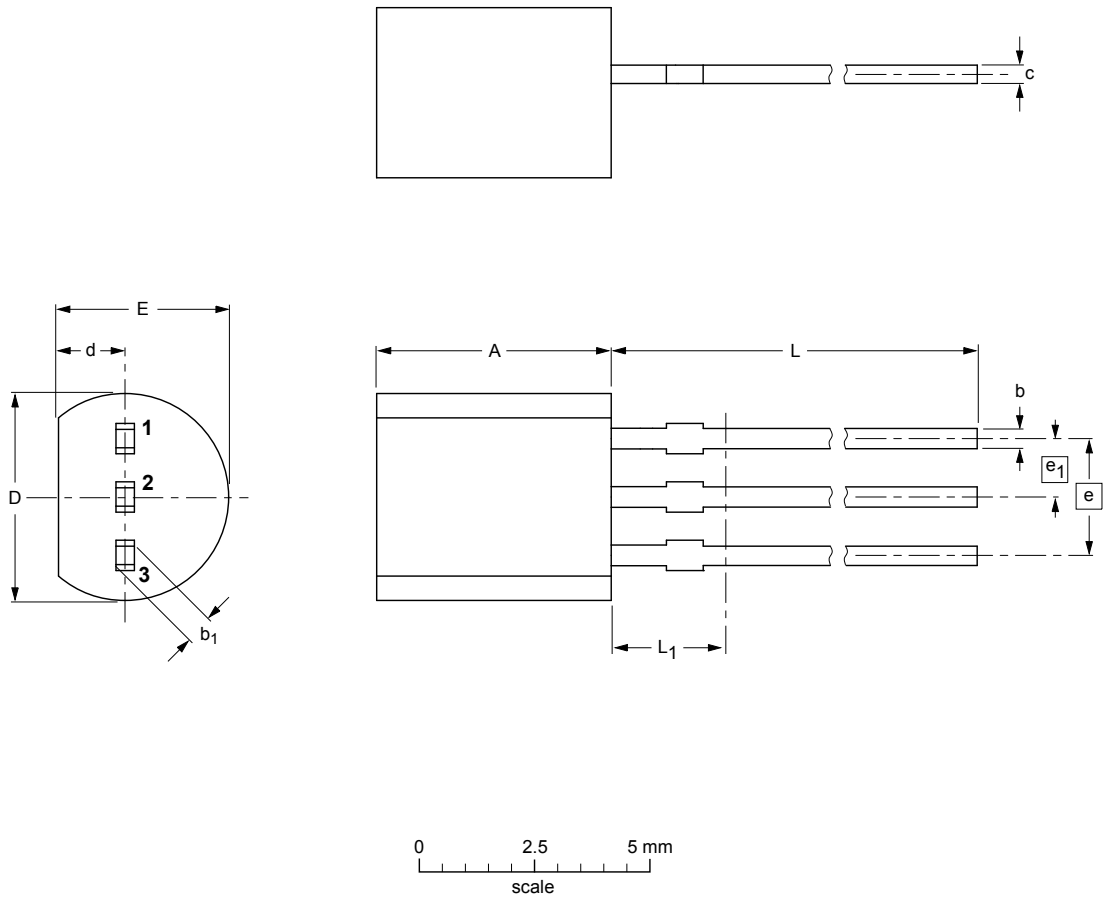



**Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; minimum values**

## 10. Package outline

**Plastic single-ended leaded (through hole) package; 3 leads** **SOT54**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | b | $b_1$ | c | D | d | E | e | $e_1$ | L | $L_1$ (1) max. |
|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 5.2<br>5.0 | 0.48<br>0.40 | 0.66<br>0.55 | 0.45<br>0.38 | 4.8<br>4.4 | 1.7<br>1.4 | 4.2<br>3.6 | 2.54 | 1.27 | 14.5<br>12.7 | 2.5 |

**Note**

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT54 | | TO-92 | SC-43A | | | ~~04-06-28~~<br>04-11-16 |

**Fig. 13. Package outline TO-92 (SOT54)**

# 11. Legal information

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| Document status [1][2] | Product status [3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
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**Date of release: 11 June 2014**