



# BT137S-600E

4Q Triac

12 June 2014

Product data sheet

## 1. General description

Planar passivated sensitive gate four quadrant triac in a SOT428 (DPAK) surface-mountable plastic package intended for use in general purpose bidirectional switching and phase control applications. This sensitive gate "series E" triac is intended to be interfaced directly to microcontrollers, logic integrated circuits and other low power gate trigger circuits.

## 2. Features and benefits

- Direct triggering from low power drivers and logic ICs
- High blocking voltage capability
- Low holding current for low current loads and lowest EMI at commutation
- Planar passivated for voltage ruggedness and reliability
- Sensitive gate
- Surface-mountable package
- Triggering in all four quadrants

## 3. Applications

- General purpose motor control
- General purpose switching

## 4. Quick reference data

Table 1. Quick reference data

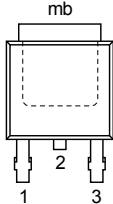

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	-	600	V
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	-	65	A
$I_{T(\text{RMS})}$	RMS on-state current	full sine wave; $T_{mb} \leq 102\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	-	8	A
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>	-	2.5	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>	-	4	10	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	5	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	11	25	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	2.5	20	mA

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	T1	main terminal 1	 <p style="text-align: center;"><b>DPAK (SOT428)</b></p>	
2	T2	main terminal 2		
3	G	gate		
mb	T2	mounting base; main terminal 2		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		Version
	Name	Description	
BT137S-600E	DPAK	plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped)	SOT428

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{mb} \leq 102\text{ °C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a> ; <a href="#">Fig. 3</a>	-	8	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 4</a> ; <a href="#">Fig. 5</a>	-	65	A
		full sine wave; $T_{j(init)} = 25\text{ °C}$ ; $t_p = 16.7\text{ ms}$	-	71	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	21	A <sup>2</sup> s
$di_T/dt$	rate of rise of on-state current	$I_T = 12\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$ ; T2+ G+	-	50	A/ $\mu\text{s}$
		$I_T = 12\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$ ; T2+ G-	-	50	A/ $\mu\text{s}$
		$I_T = 12\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$ ; T2- G-	-	50	A/ $\mu\text{s}$
		$I_T = 12\text{ A}$ ; $I_G = 0.2\text{ A}$ ; $dI_G/dt = 0.2\text{ A}/\mu\text{s}$ ; T2- G+	-	10	A/ $\mu\text{s}$
$I_{GM}$	peak gate current		-	2	A
$P_{GM}$	peak gate power		-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.5	W
$T_{stg}$	storage temperature		-40	150	°C
$T_j$	junction temperature		-	125	°C

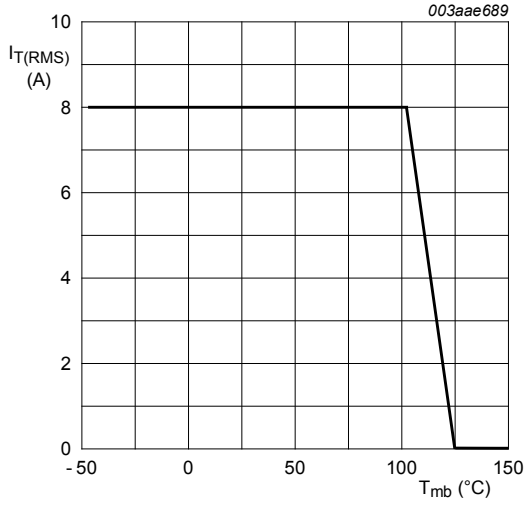
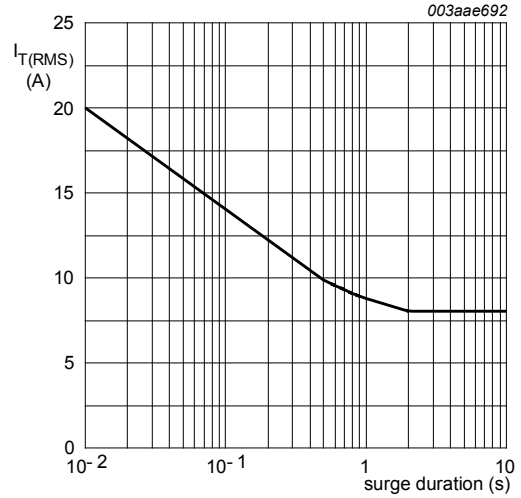
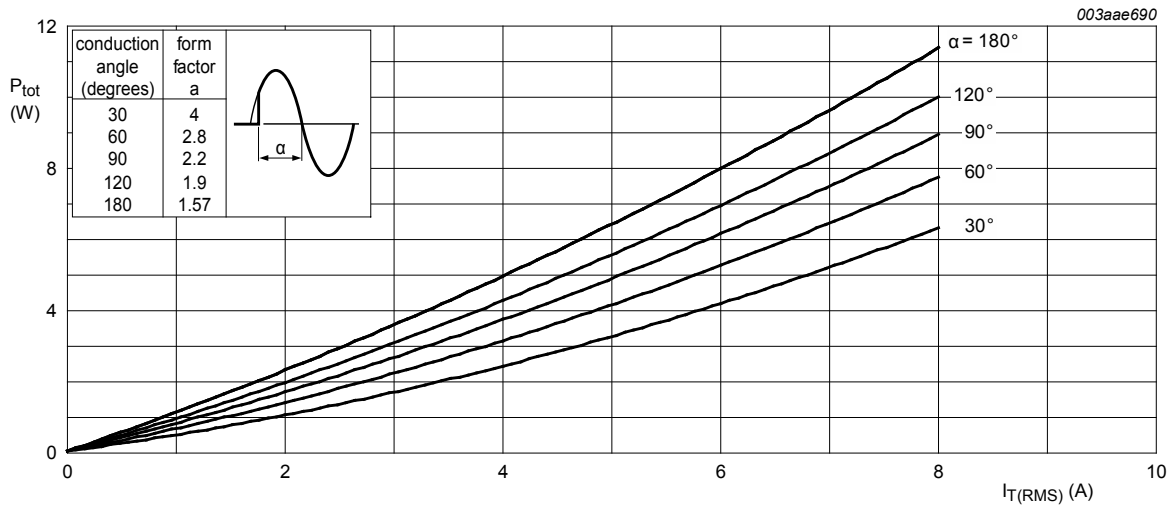


Fig. 1. RMS on-state current as a function of mounting base temperature; maximum values



f = 50 Hz  
 $T_{mb} \leq 102\text{ }^{\circ}\text{C}$

Fig. 2. RMS on-state current as a function of surge duration; maximum values



$\alpha$  = conduction angle  
 a = form factor =  $I_{T(RMS)}/I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values

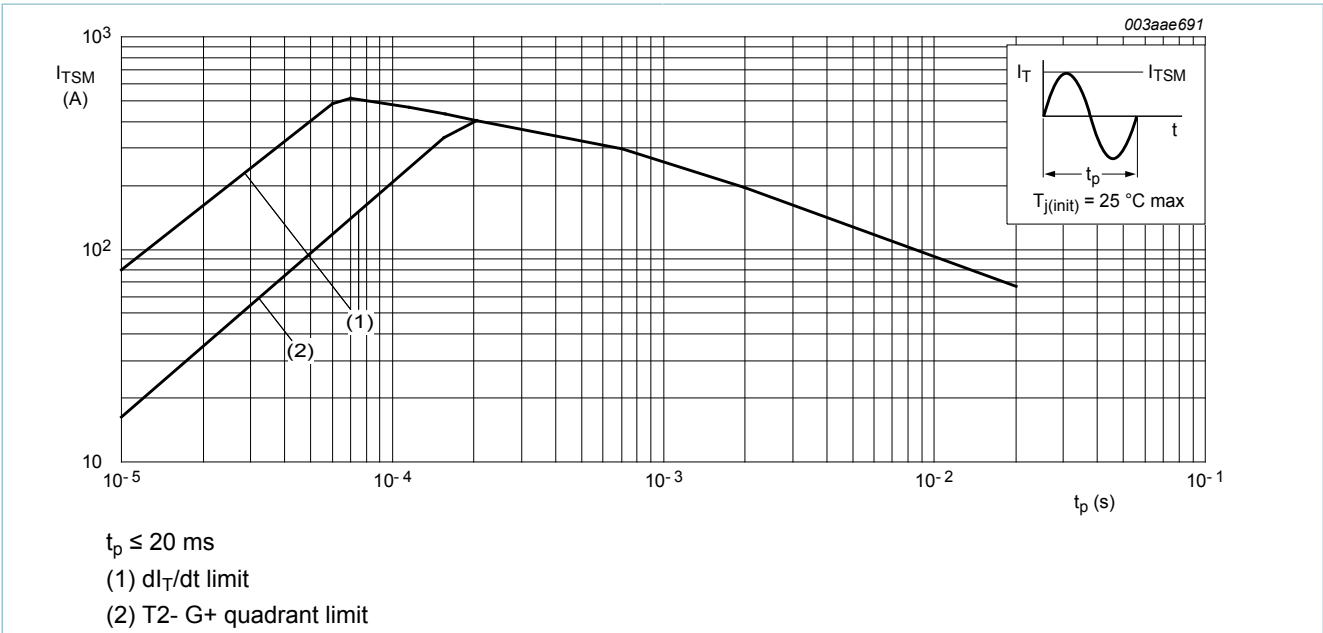


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

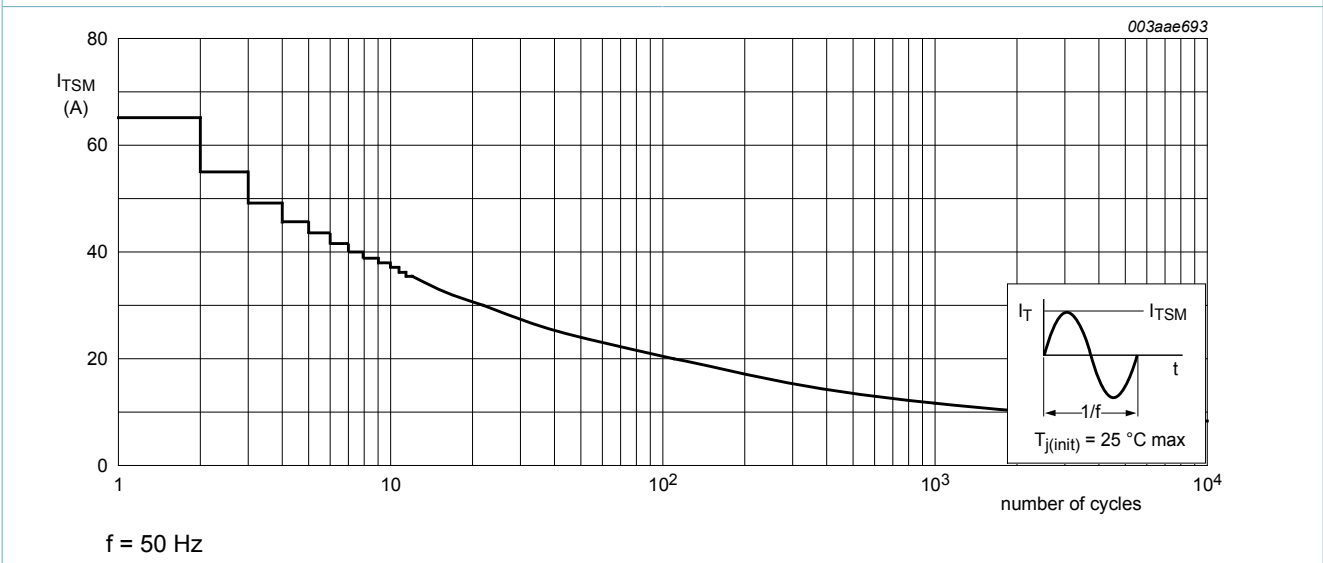


Fig. 5. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	half cycle; <a href="#">Fig. 6</a>	-	-	2.4	K/W
		full cycle; <a href="#">Fig. 6</a>	-	-	2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	PCB (FR4) mounted; minimum pad sizes	-	75	-	K/W

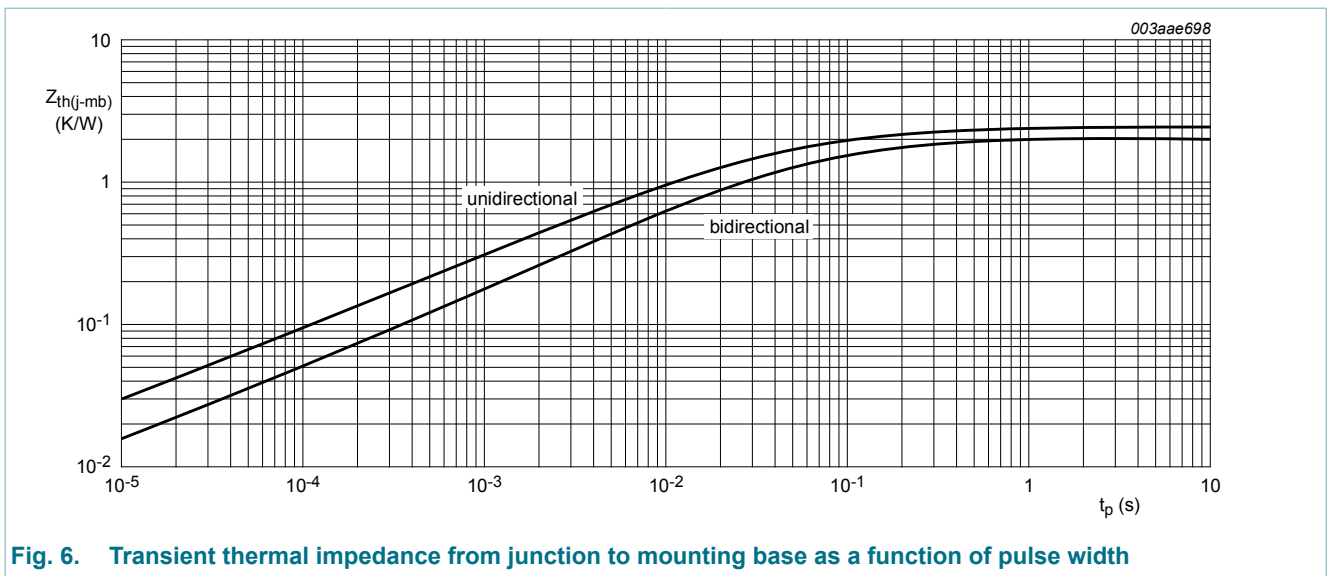
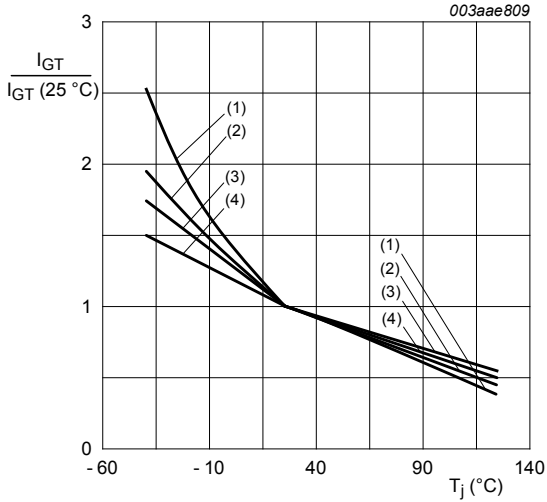


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

## 9. Characteristics

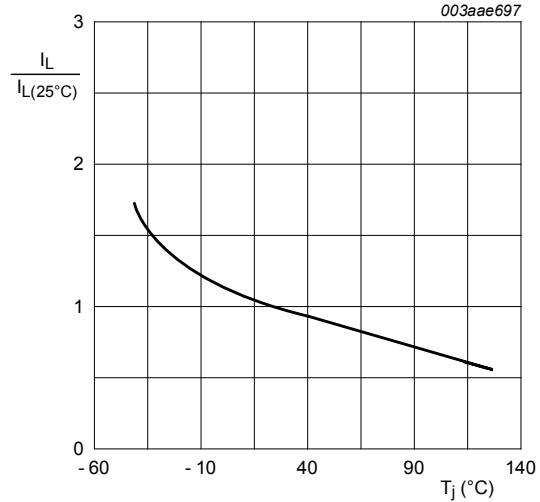
Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$I_{GT}$	gate trigger current	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	2.5	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	4	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	5	10	mA
		$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	-	11	25	mA
$I_L$	latching current	$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	3	25	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2+ G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	14	35	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	3	25	mA
		$V_D = 12\text{ V}$ ; $I_G = 0.1\text{ A}$ ; T2- G+; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 8</a>	-	4	35	mA
$I_H$	holding current	$V_D = 12\text{ V}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 9</a>	-	2.5	20	mA
$V_T$	on-state voltage	$I_T = 10\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 10</a>	-	1.3	1.65	V
$V_{GT}$	gate trigger voltage	$V_D = 12\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	-	0.7	1	V
		$V_D = 400\text{ V}$ ; $I_T = 0.1\text{ A}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; <a href="#">Fig. 11</a>	0.25	0.4	-	V
$I_D$	off-state current	$V_D = 600\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$	-	0.1	0.5	mA
<b>Dynamic characteristics</b>						
$dV_D/dt$	rate of rise of off-state voltage	$V_{DM} = 402\text{ V}$ ; $T_j = 125\text{ }^\circ\text{C}$ ; ( $V_{DM} = 67\%$ of $V_{DRM}$ ); exponential waveform; gate open circuit	-	50	-	V/ $\mu\text{s}$
$t_{gt}$	gate-controlled turn-on time	$I_{TM} = 12\text{ A}$ ; $V_D = 600\text{ V}$ ; $I_G = 0.1\text{ A}$ ; $dI_G/dt = 5\text{ A}/\mu\text{s}$	-	2	-	$\mu\text{s}$

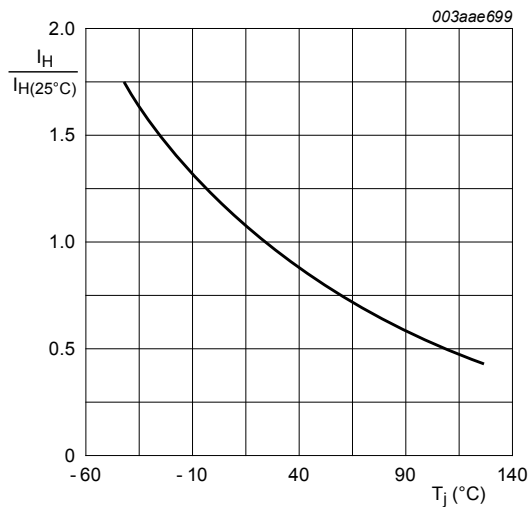


- (1) T2- G+
- (2) T2- G-
- (3) T2+ G-
- (4) T2+ G+

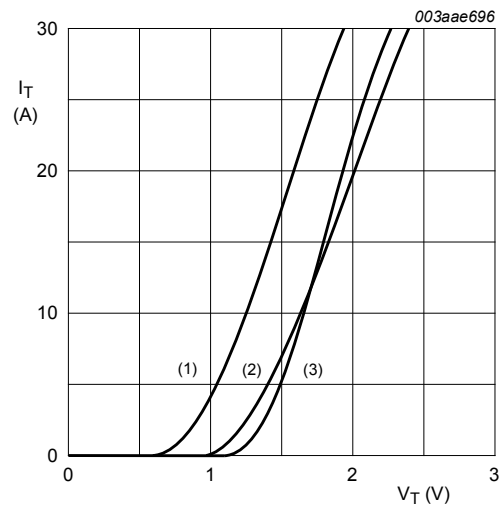
**Fig. 7. Normalized gate trigger current as a function of junction temperature**



**Fig. 8. Normalized latching current as a function of junction temperature**



**Fig. 9. Normalized holding current as a function of junction temperature**



$V_o = 1.264 \text{ V}$

$R_s = 0.038 \ \Omega$

(1)  $T_j = 125^\circ\text{C}$ ; typical values

(2)  $T_j = 125^\circ\text{C}$ ; maximum values

(3)  $T_j = 25^\circ\text{C}$ ; maximum values

**Fig. 10. On-state current as a function of on-state voltage**



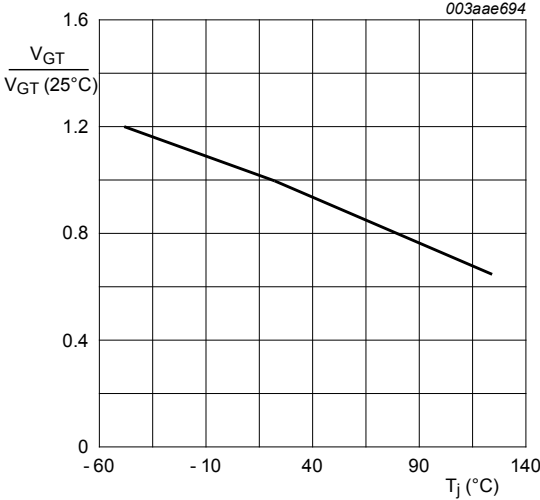
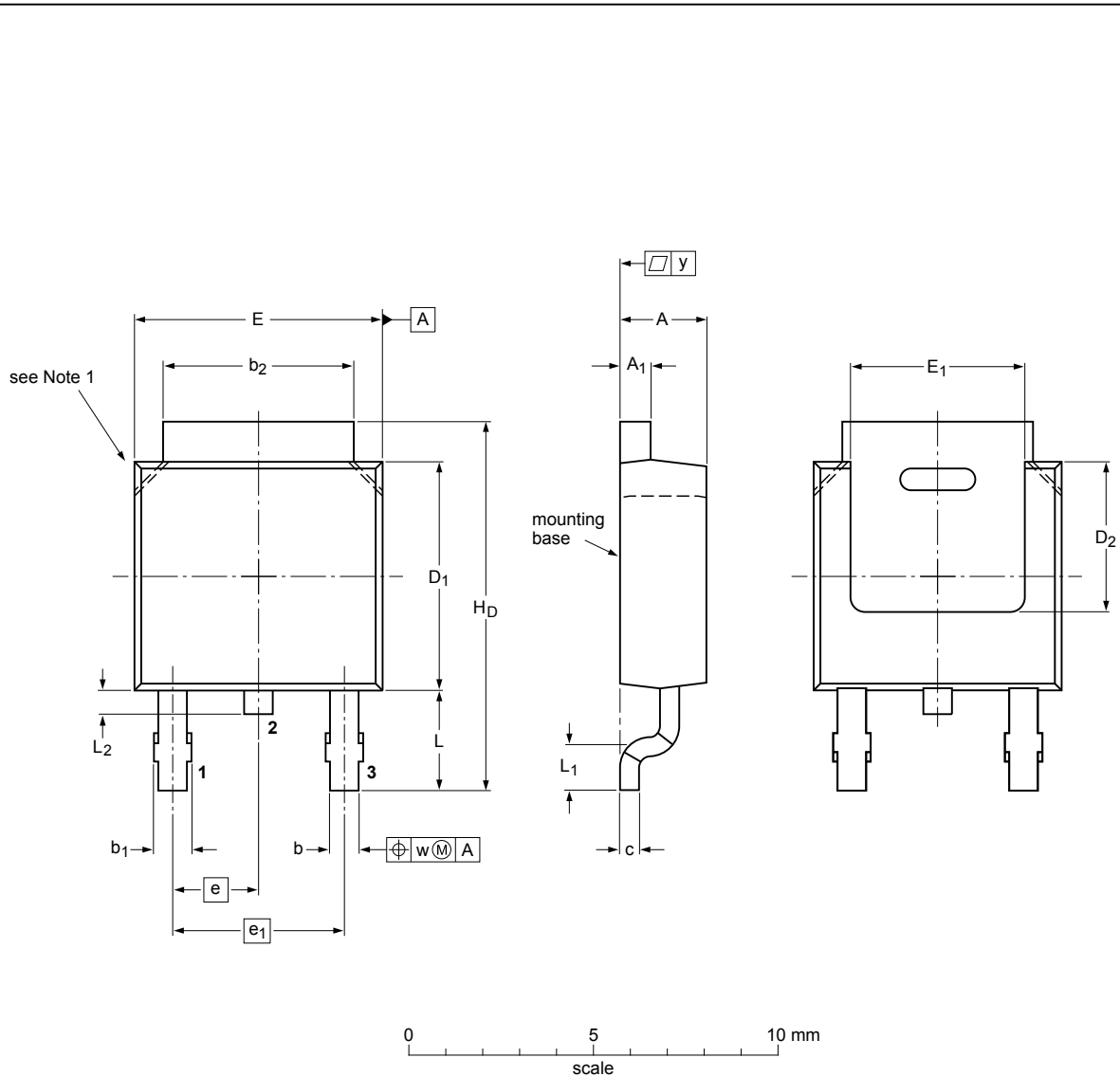


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

### 10. Package outline

Plastic single-ended surface-mounted package (DPAK); 3 leads (one lead cropped) SOT428



Dimensions (mm are the original dimensions)

Unit	A	A <sub>1</sub>	b	b <sub>1</sub>	b <sub>2</sub>	c	D <sub>1</sub>	D <sub>2</sub>	E	E <sub>1</sub>	e	e <sub>1</sub>	H <sub>D</sub>	L	L <sub>1</sub>	L <sub>2</sub>	w	y
max	2.38	0.93	0.89	1.1	5.46	0.56	6.22		6.73				10.4	2.95		0.9		0.2
nom											2.285	4.57					0.2	
min	2.22	0.46	0.71	0.9	5.00	0.20	5.98	4.0	6.47	4.45			9.6	2.55	0.5	0.5		

Note

1. Plastic body may have 45° chamfer.

sot428\_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT428		TO-252	SC-63		06-03-16 14-06-10

Fig. 12. Package outline DPAK (SOT428)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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