ACT108W-800E

AC Thyristor power switch

20 August 2014 **Product data sheet**

1. General description

AC Thyristor power switch in a SOT223 surface-mountable plastic package with self-protective capabilities against low and high energy transients.

2. Features and benefits

- Common terminal on mounting base allows multiple ACTs on shared cooling pad
- Exclusive negative gate triggering
- Full cycle AC conduction
- High voltage capability
- Remote gate separates the gate driver from the effects of the load current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients
- Surface-mountable package
- Very high noise immunity

3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads
- Contactors, circuit breakers, valves, dispensers and door locks

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	800	V
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	-	13	A
T_j	junction temperature			-	-	125	°C
$I_{T(RMS)}$	RMS on-state current	full sine wave; Fig. 1; Fig. 2; Fig. 3		-	-	0.8	A
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; ten pulses on each voltage polarity; 20s or more between successive pulses; Fig. 6		-	-	2.5	kV

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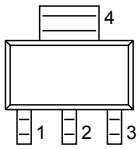
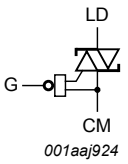
Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 10		1	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 10		1	-	10	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 15		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 0.8 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 16; Fig. 17		0.5	-	-	A/ms

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	LD	load	 **SC-73 (SOT223)**	 *001aaj924*
2	CM	common		
3	G	gate		
4	CM	common		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
ACT108W-800E	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	800	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; Fig. 1; Fig. 2; Fig. 3		-	0.8	A
I_{TSM}	non-repetitive peak on-state current	full sine wave; $T_{j(init)}$ = 25 °C; t_p = 20 ms; Fig. 4; Fig. 5		-	13	A
		full sine wave; $T_{j(init)}$ = 25 °C; t_p = 16.7 ms		-	14.3	A
I^2t	I^2t for fusing	t_p = 10 ms; sine-wave pulse		-	0.84	A^2s
dI_T/dt	rate of rise of on-state current	I_T = 1 A; I_G = 20 mA; dI_G/dt = 0.2 A/µs		-	100	A/µs
I_{GM}	peak gate current	t = 20 µs		-	1	A
V_{GM}	peak gate voltage	positive applied gate voltage		-	15	V
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.1	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	125	°C
V_{PP}	peak pulse voltage	T_j = 25 °C; non-repetitive, off-state; ten pulses on each voltage polarity; 20s or more between successive pulses; Fig. 6		-	2.5	kV

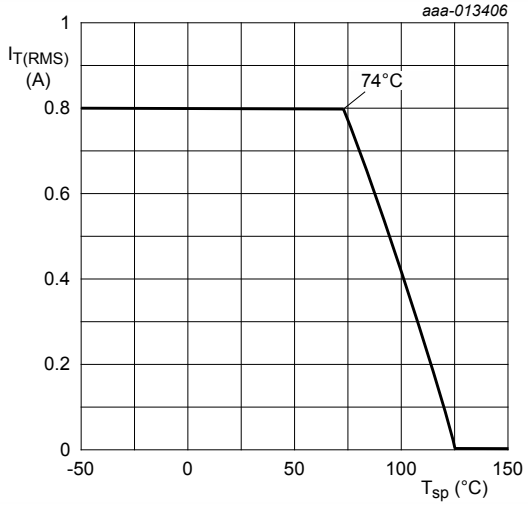
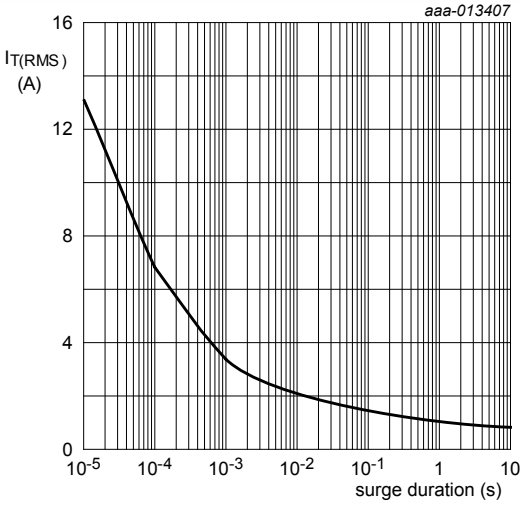


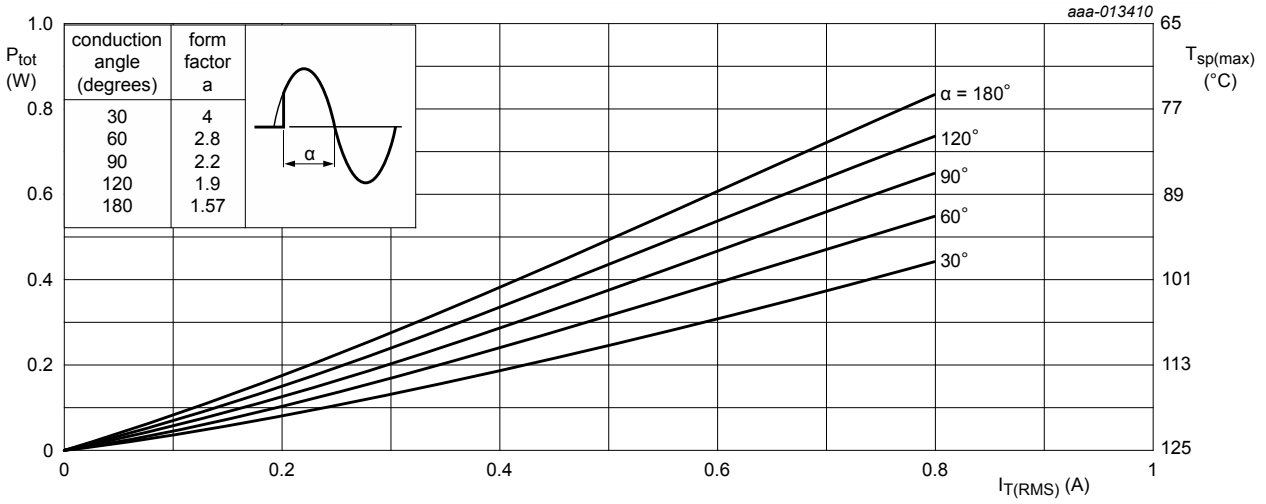
Fig. 1. RMS on-state current as a function of solder point temperature; maximum values



f = 50 Hz

T_{sp} = 74 °C

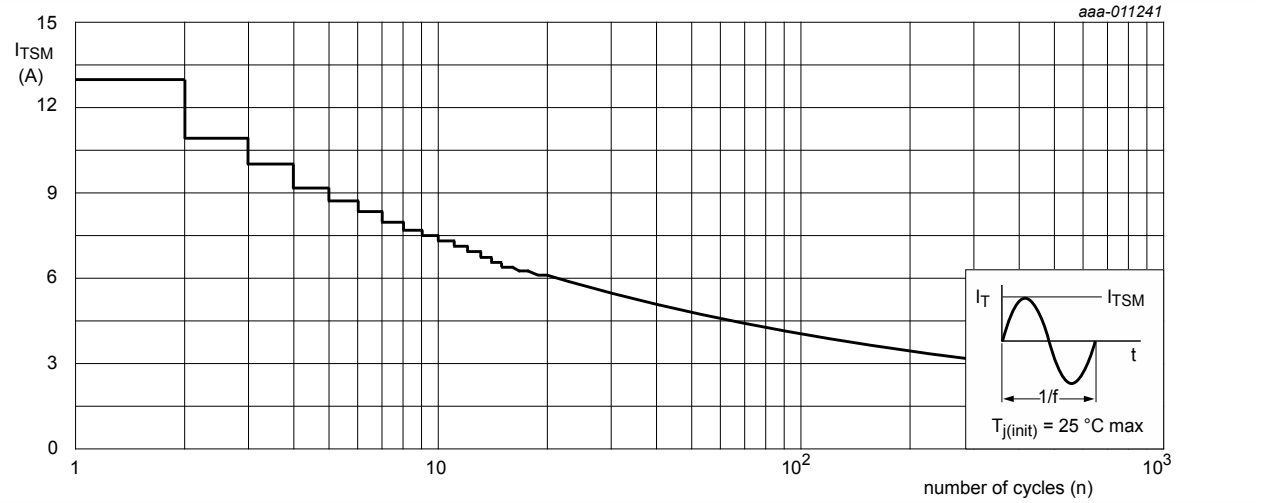
Fig. 2. RMS on-state current as a function of surge duration; maximum values



α = conduction angle

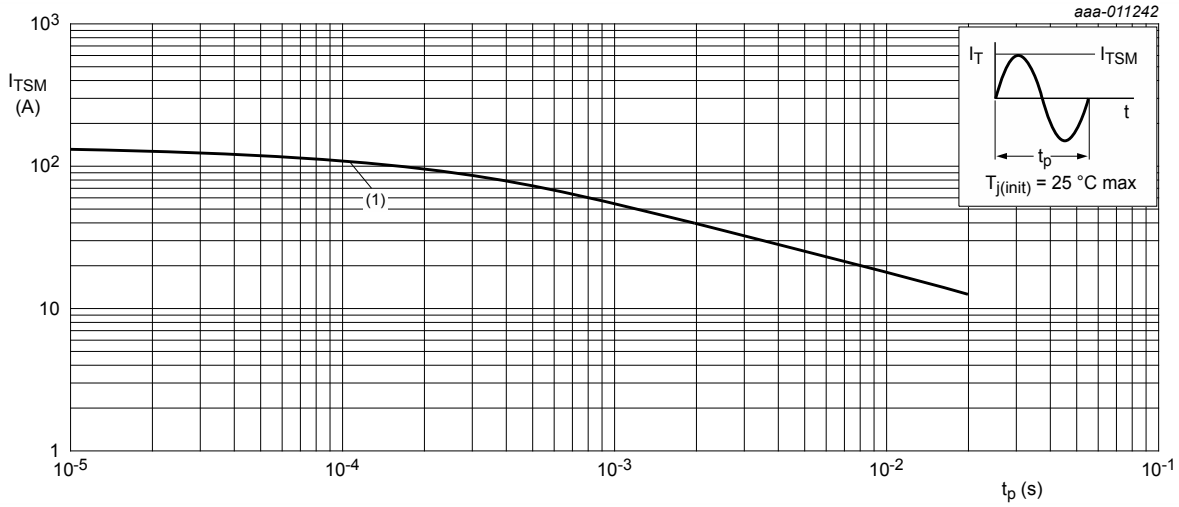
a = form factor = $I_{T(RMS)}/I_{T(AV)}$

Fig. 3. Total power dissipation as a function of RMS on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 20$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width; maximum values

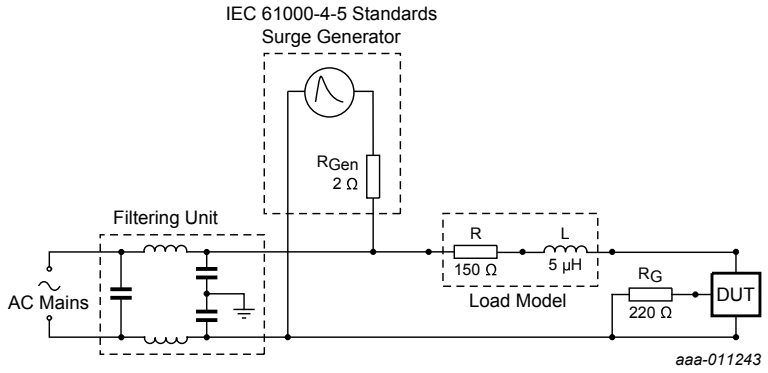


Fig. 6. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	full cycle with heatsink compound;; Fig. 7		-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; printed-circuit board mounted for pad area; Fig. 8		-	70	-	K/W
		full cycle; printed-circuit board mounted for minimum footprint; Fig. 9		-	156	-	K/W

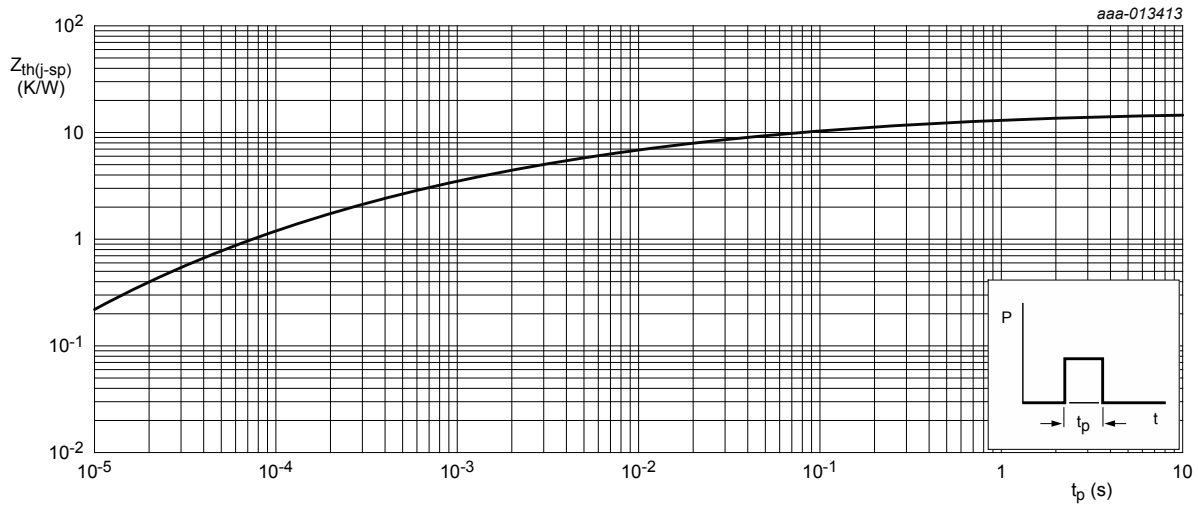
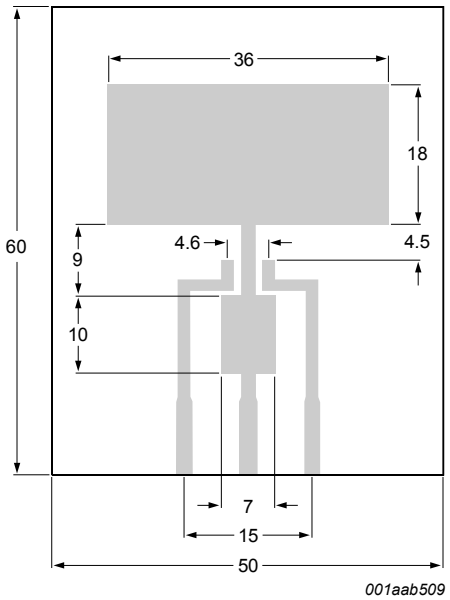


Fig. 7. Transient thermal impedance from junction to solder point as a function of pulse width

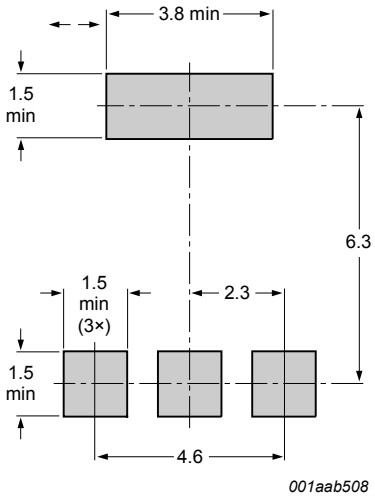


All dimensions are in mm

Printed circuit board:

FR4 epoxy glass (1.6 mm thick), copper laminate (35 um thick)

Fig. 8. Printed circuit board pad area: SOT223



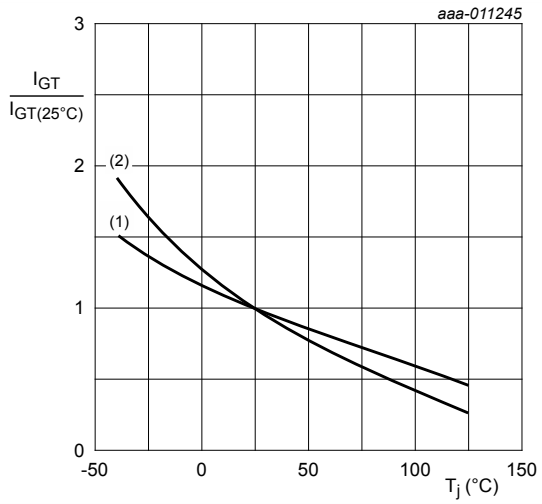
All dimensions are in mm

Fig. 9. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 100 mA; LD+ G-; T_j = 25 °C; Fig. 10		1	-	10	mA
		V_D = 12 V; I_T = 100 mA; LD- G-; T_j = 25 °C; Fig. 10		1	-	10	mA
I_L	latching current	V_D = 12 V; I_G = 100 mA; LD+ G-; T_j = 25 °C; Fig. 11		-	-	25	mA
		V_D = 12 V; I_G = 100 mA; LD- G-; T_j = 25 °C; Fig. 11		-	-	20	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 12		-	-	20	mA
V_T	on-state voltage	I_T = 1.1 A; T_j = 25 °C; Fig. 13		-	-	1.3	V
V_{GT}	gate trigger voltage	V_D = 400 V; I_T = 100 mA; T_j = 125 °C; Fig. 14		0.15	-	-	V
		V_D = 12 V; I_T = 100 mA; T_j = 25 °C; Fig. 14		-	-	1	V
I_D	off-state current	V_D = 800 V; T_j = 25 °C		-	-	2	µA
		V_D = 800 V; T_j = 125 °C		-	-	0.2	mA
V_{CL}	clamping voltage	I_{CL} = 0.1 mA; t_p = 1 ms; T_j = 25 °C		850	-	-	V
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 536 V; T_j = 125 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 15		500	-	-	V/µs
dI_{com}/dt	rate of change of commutating current	V_D = 400 V; T_j = 125 °C; $I_{T(RMS)}$ = 0.8 A; dV_{com}/dt = 20 V/µs; (snubberless condition); gate open circuit; Fig. 16; Fig. 17		0.5	-	-	A/ms



(1) LD+ G-
(2) LD- G-

Fig. 10. Normalized gate trigger current as a function of junction temperature

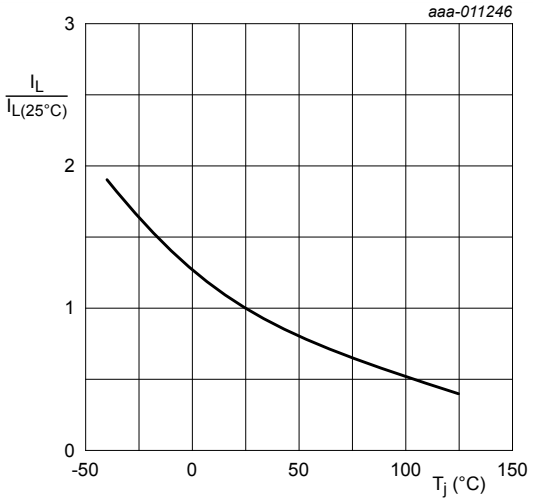


Fig. 11. Normalized latching current as a function of junction temperature

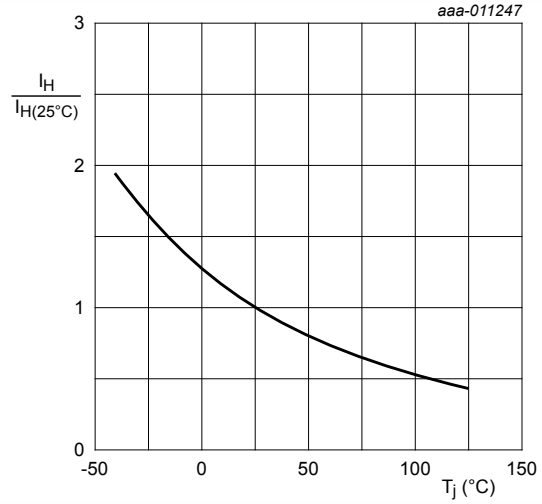
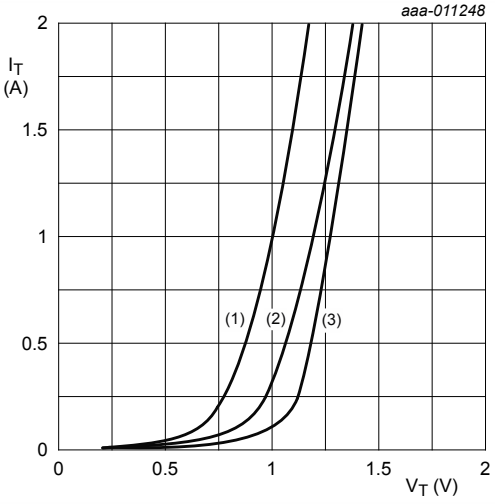


Fig. 12. Normalized holding current as a function of junction temperature



V_o = 0.967 V; R_s = 0.225 Ω
(1) T_j = 125 °C; typical values
(2) T_j = 125 °C; maximum values
(3) T_j = 25 °C; maximum values

Fig. 13. On-state current as a function of on-state voltage

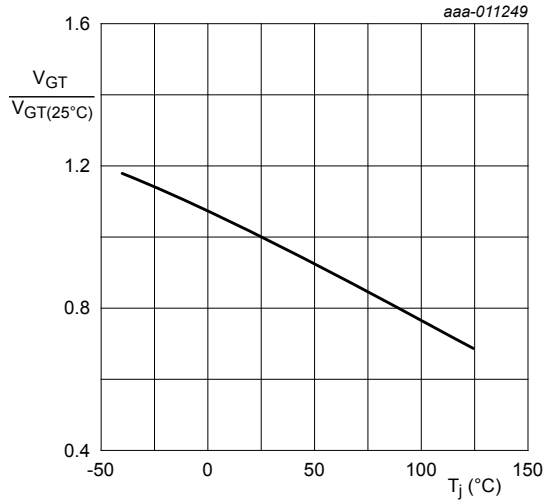
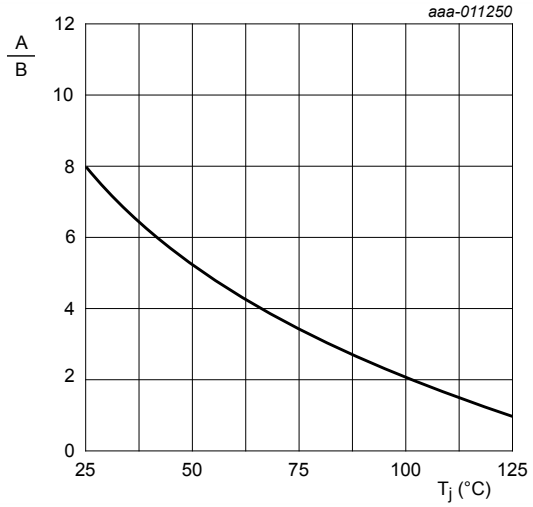


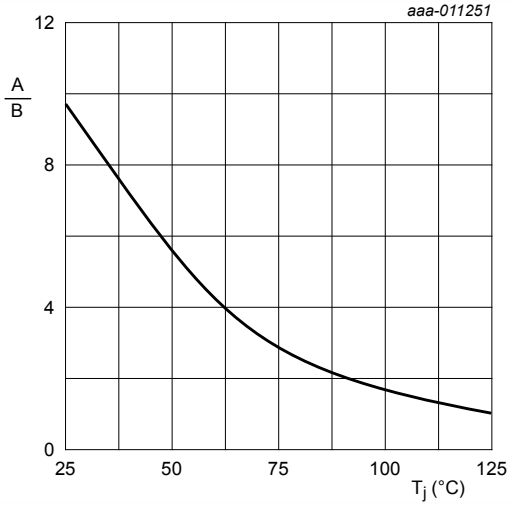
Fig. 14. Normalized gate trigger voltage as a function of junction temperature



A = dV_D/dt at condition T_j °C

B = dV_D/dt at condition T_j [125] °C

Fig. 15. Normalized rate of rise of off-state voltage as a function of junction temperature

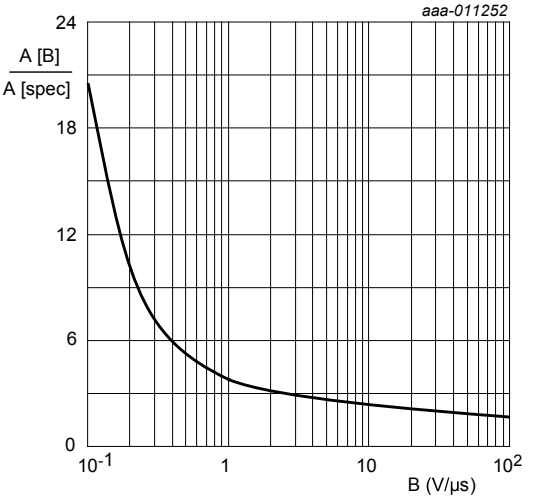


A = dI_{com}/dt at condition T_j °C

B = dI_{com}/dt at condition T_j [125] °C

V_D = 400 V

Fig. 16. Normalized critical rate of rise of commutating current as a function of junction temperature



A [B] = dI_{com}/dt at condition B, dV_{com}/dt

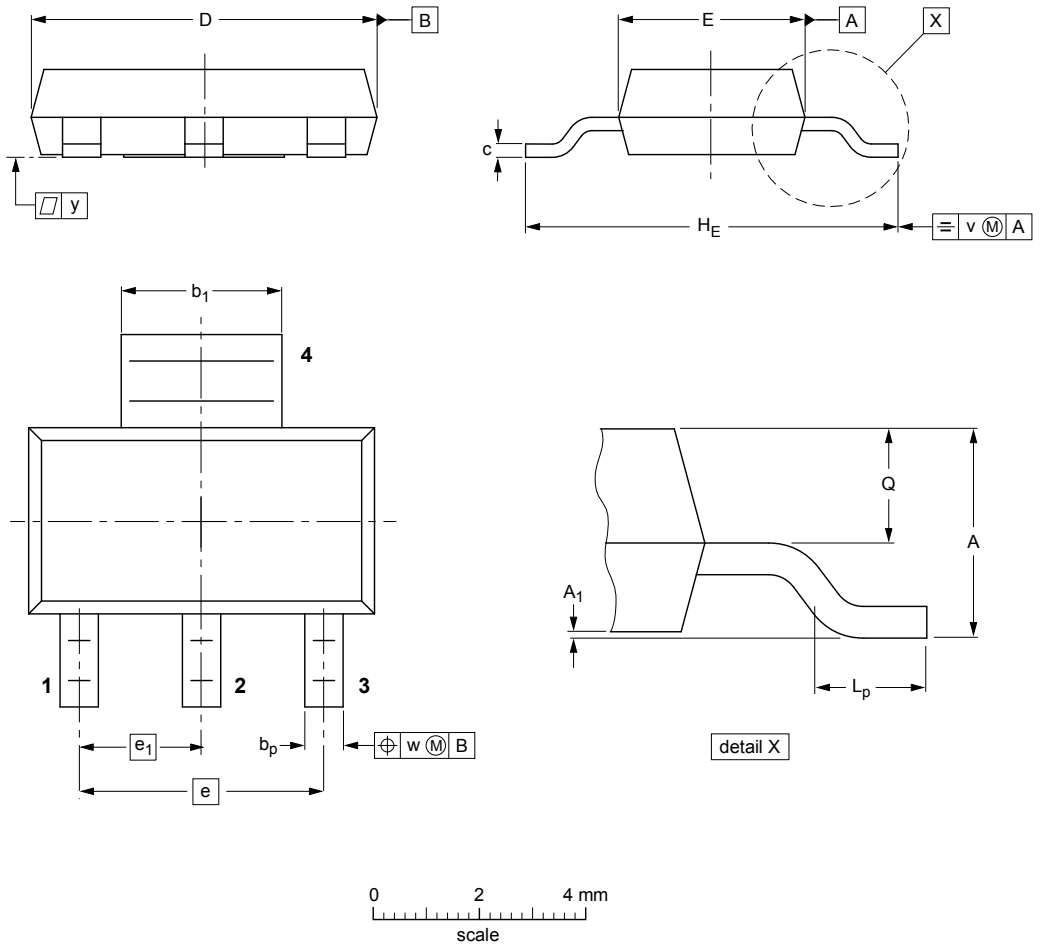
A [spec] is the data sheet value for dI_{com}/dt

turn-off time is less than 20 ms

Fig. 17. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values

10. Package outline

Plastic surface-mounted package with increased heatsink; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT223			SC-73			~~04-11-10~~ 06-03-16

Fig. 18. Package outline SC-73 (SOT223)

11. Soldering

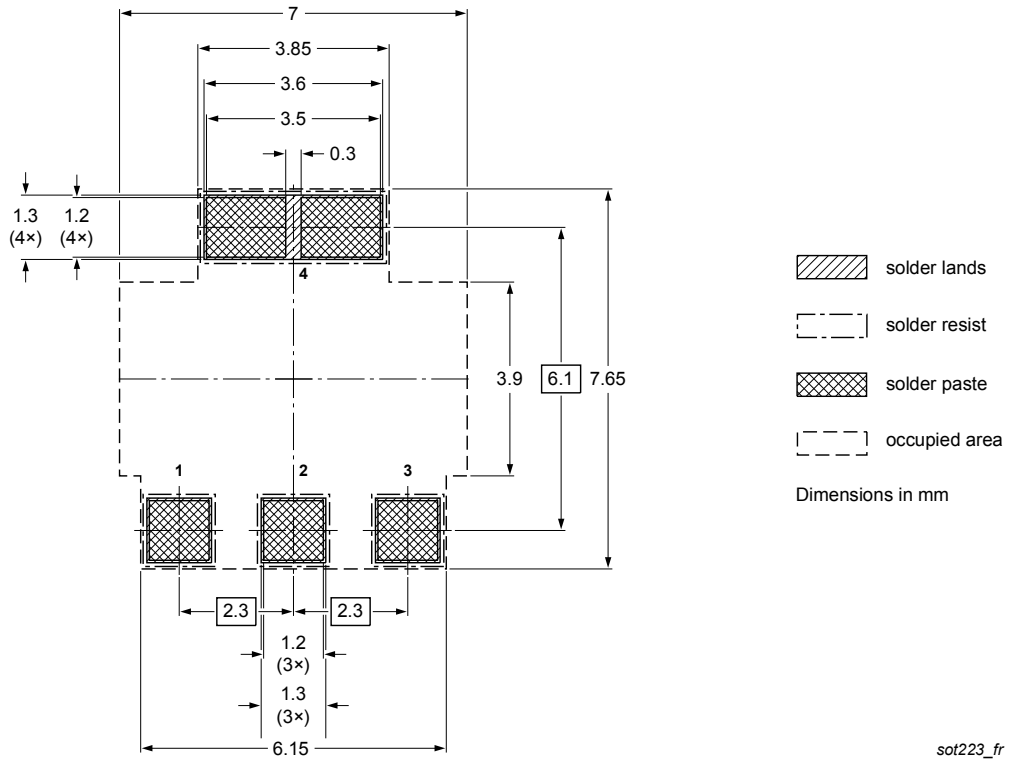


Fig. 19. Reflow soldering footprint for SC-73 (SOT223)

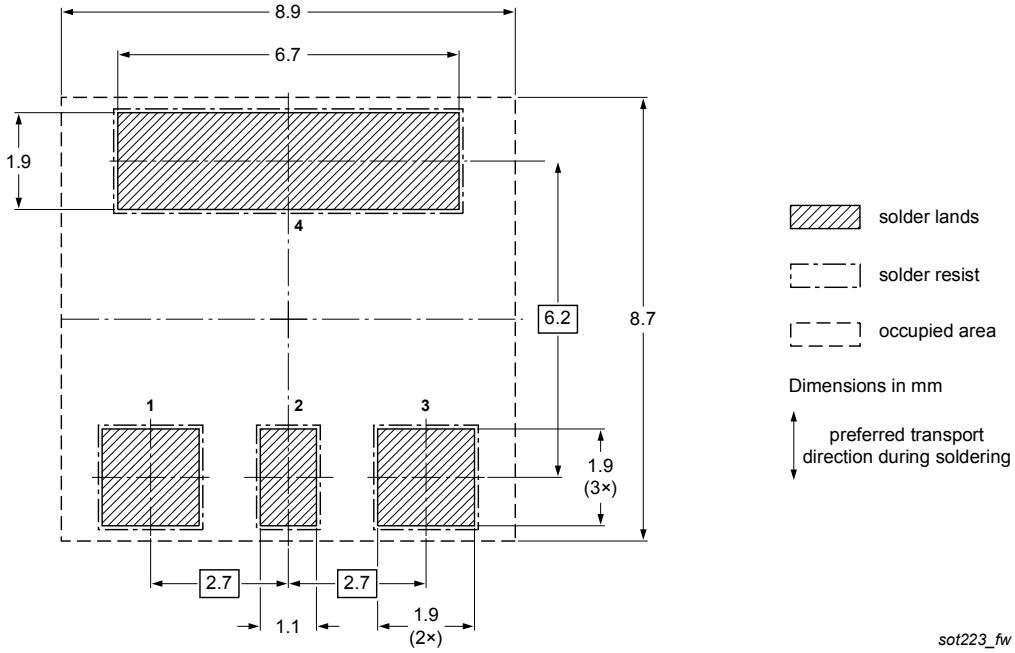


Fig. 20. Wave soldering footprint for SC-73 (SOT223)

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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