



# ACT102H-600D

AC Thyristor power switch

20 August 2014

Product data sheet

## 1. General description

An AC Thyristor power switch with very high noise immunity and over-voltage protection configured for negative gate triggering in a SOT96-1 (SO8) small surface-mountable plastic package

## 2. Features and benefits

- Exclusive negative gate triggering
- Full cycle AC conduction
- High noise immunity
- Remote gate separates the gate driver from the effects of the load current
- Surface-mountable package
- Very sensitive gate for lowest gate trigger current
- Safe clamping of low energy over-voltage transients
- Self-protective turn-on during high energy voltage transients

## 3. Applications

- Fan motor circuits
- Pump motor circuits
- Lower-power highly inductive, resistive and safety loads

## 4. Quick reference data

Table 1. Quick reference data

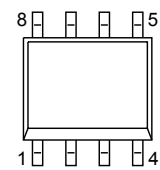
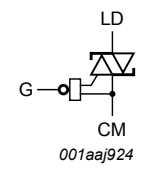
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{\text{DRM}}$	repetitive peak off-state voltage		-	-	600	V
$I_{\text{TSM}}$	non-repetitive peak on-state current	full sine wave; $T_{\text{J}(\text{init})} = 25\text{ }^{\circ}\text{C}$ ; $t_{\text{p}} = 20\text{ ms}$ ; <a href="#">Fig. 3</a> ; <a href="#">Fig. 4</a>	-	-	8	A
$I_{\text{T(RMS)}}$	RMS on-state current	full sine wave; $T_{\text{amb}} \leq 100\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a>	-	-	0.2	A
$V_{\text{PP}}$	peak pulse voltage	$T_{\text{J}} \leq 25\text{ }^{\circ}\text{C}$ ; non-repetitive, off-state; <a href="#">Fig. 5</a>	-	-	2	kV
<b>Static characteristics</b>						
$I_{\text{GT}}$	gate trigger current	$V_{\text{D}} = 12\text{ V}$ ; $I_{\text{T}} = 100\text{ mA}$ ; LD+ G-; $T_{\text{J}} = 25\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 7</a>	0.5	-	5	mA



Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		$V_D = 12\text{ V}$ ; $I_T = 100\text{ mA}$ ; LD- G-; $T_j = 25\text{ }^\circ\text{C}$ ; <a href="#">Fig. 7</a>	0.5	-	5	mA
$V_{CL}$	clamping voltage	$I_{CL} = 0.1\text{ mA}$ ; $t_p = 1\text{ ms}$ ; $T_j \leq 125\text{ }^\circ\text{C}$	650	-	-	V

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	n.c.	not connected	 <p><b>SO8 (SOT96-1)</b></p>	 <p>001aaJ924</p>
2	LD	Load		
3	n.c.	not connected		
4	n.c.	not connected		
5	G	Gate		
6	CM	Common		
7	CM	Common		
8	n.c.	not connected		

## 6. Ordering information

Table 3. Ordering information

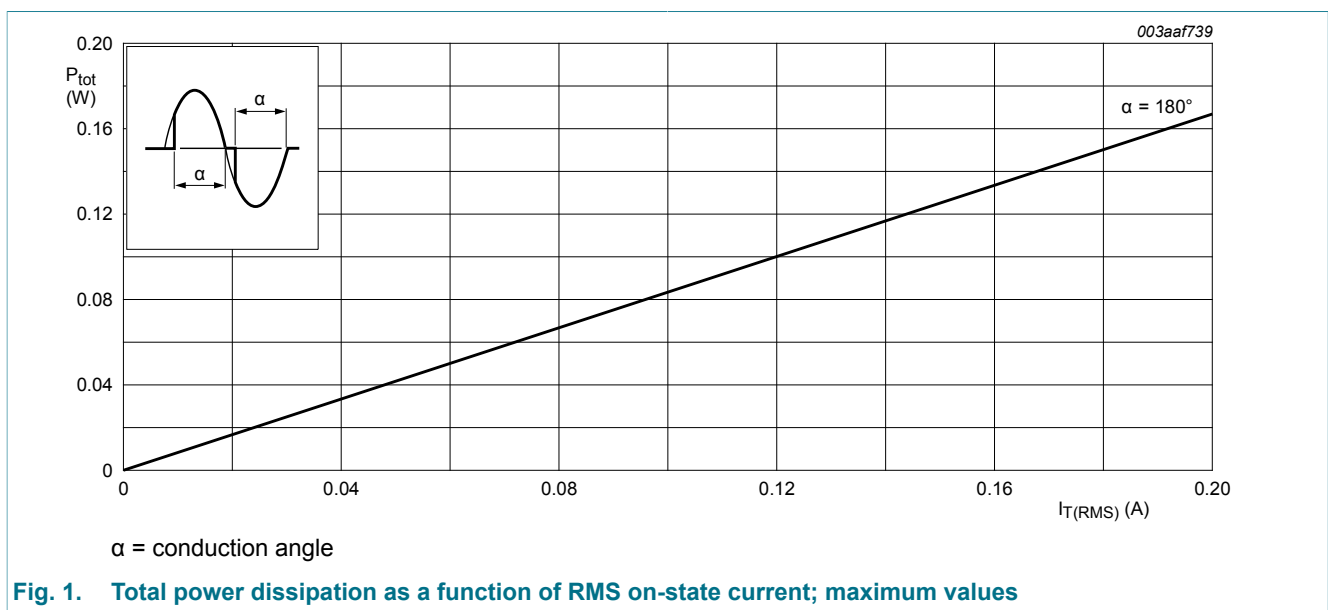
Type number	Package		
	Name	Description	Version
ACT102H-600D	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

## 7. Limiting values

**Table 4. Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DRM}$	repetitive peak off-state voltage		-	600	V
$I_{T(RMS)}$	RMS on-state current	full sine wave; $T_{amb} \leq 100\text{ }^{\circ}\text{C}$ ; <a href="#">Fig. 1</a> ; <a href="#">Fig. 2</a>	-	0.2	A
$I_{TSM}$	non-repetitive peak on-state current	full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 16.7\text{ ms}$	-	8.8	A
		full sine wave; $T_{j(init)} = 25\text{ }^{\circ}\text{C}$ ; $t_p = 20\text{ ms}$ ; <a href="#">Fig. 3</a> ; <a href="#">Fig. 4</a>	-	8	A
$I^2t$	$I^2t$ for fusing	$t_p = 10\text{ ms}$ ; SIN	-	0.31	$\text{A}^2\text{s}$
$di_T/dt$	rate of rise of on-state current	$I_T = 1\text{ A}$ ; $I_G = 20\text{ mA}$ ; $di_G/dt = 0.2\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
$I_{GM}$	peak gate current	$t = 20\text{ }\mu\text{s}$	-	1	A
$P_{GM}$	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
$T_{stg}$	storage temperature		-40	150	$^{\circ}\text{C}$
$T_j$	junction temperature		-	125	$^{\circ}\text{C}$
$V_{PP}$	peak pulse voltage	$T_j \leq 25\text{ }^{\circ}\text{C}$ ; non-repetitive, off-state; <a href="#">Fig. 5</a>	-	2	kV



**Fig. 1. Total power dissipation as a function of RMS on-state current; maximum values**

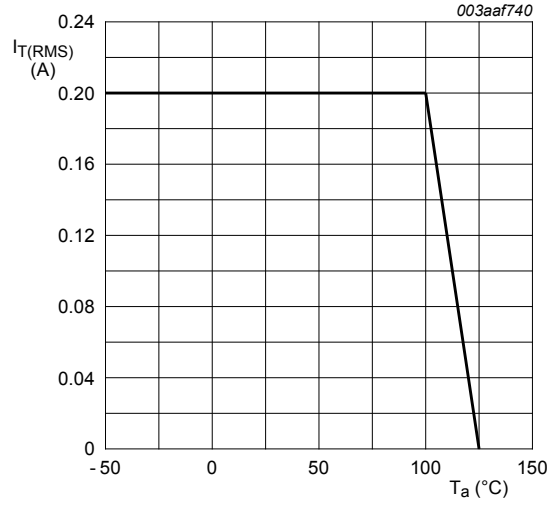


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

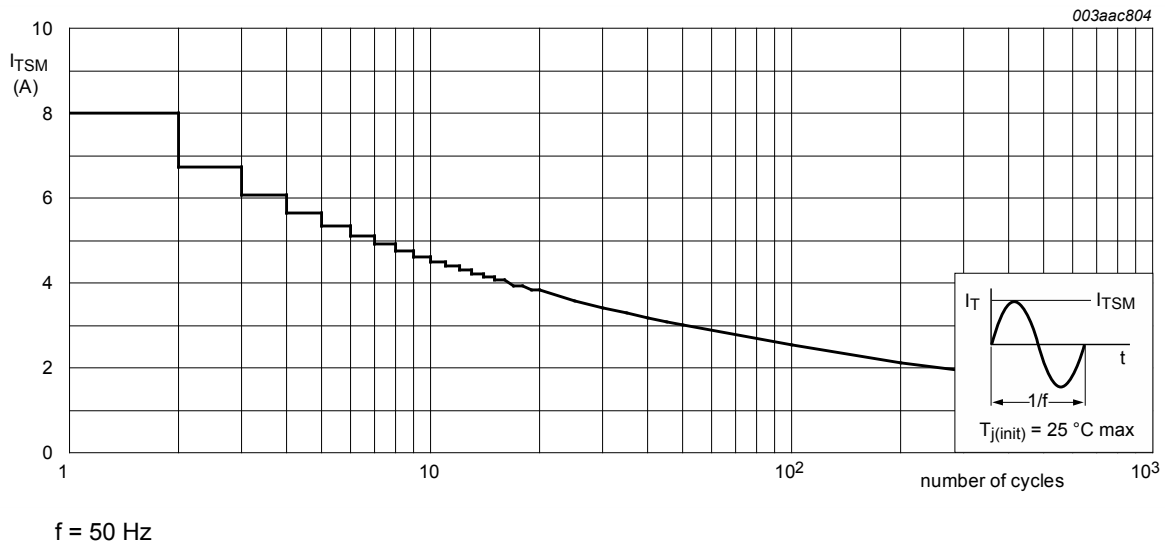


Fig. 3. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values

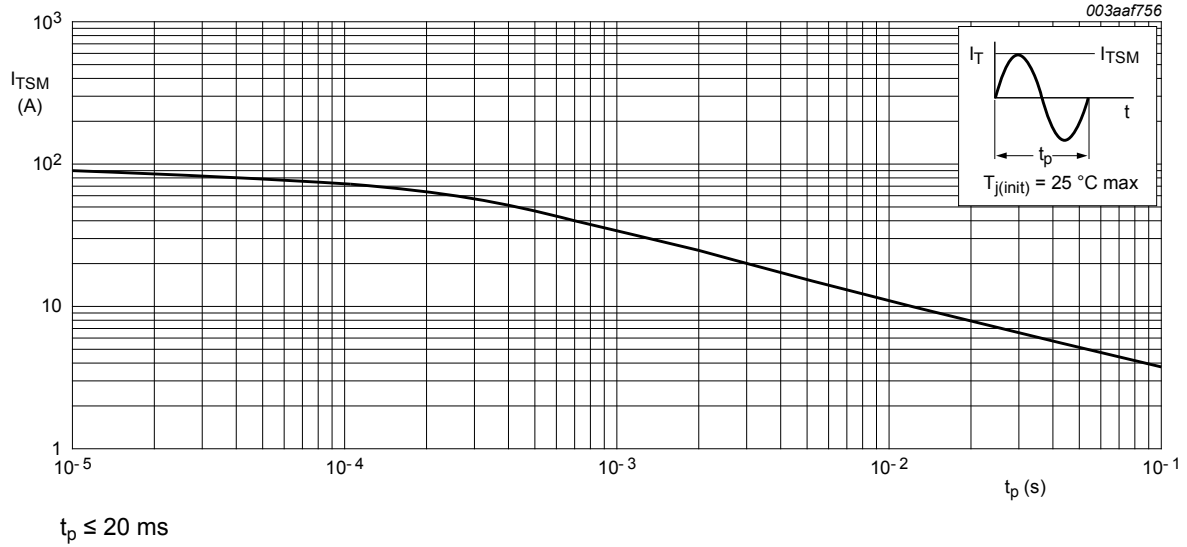


Fig. 4. Non-repetitive peak on-state current as a function of pulse width; maximum values

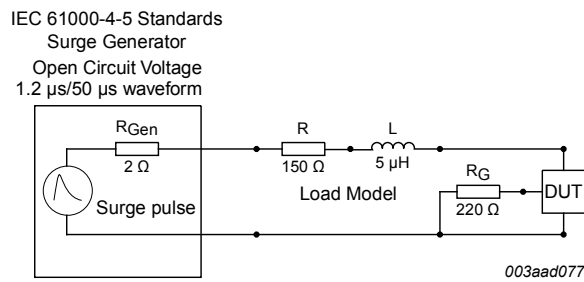


Fig. 5. Test circuit for inductive and resistive loads with conditions equivalent to IEC 61000-4-5

## 8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	full cycle; <a href="#">Fig. 6</a>	-	150	-	K/W

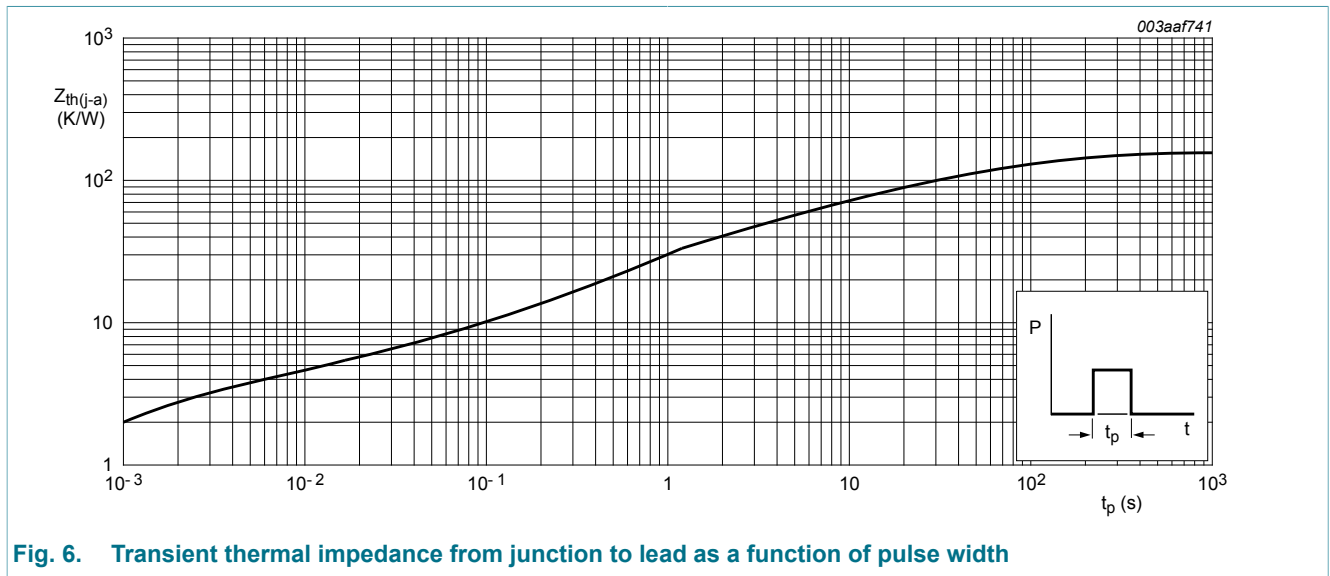


Fig. 6. Transient thermal impedance from junction to lead as a function of pulse width

## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
I <sub>GT</sub>	gate trigger current	V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	0.5	-	5	mA
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 7</a>	0.5	-	5	mA
I <sub>L</sub>	latching current	V <sub>D</sub> = 12 V; I <sub>G</sub> = 100 mA; LD+ G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	25	mA
		V <sub>D</sub> = 12 V; I <sub>G</sub> = 100 mA; LD- G-; T <sub>j</sub> = 25 °C; <a href="#">Fig. 8</a>	-	-	25	mA
I <sub>H</sub>	holding current	V <sub>D</sub> = 12 V; T <sub>j</sub> = 25 °C; <a href="#">Fig. 9</a>	-	-	20	mA
V <sub>T</sub>	on-state voltage	I <sub>T</sub> = 0.3 A; T <sub>j</sub> = 25 °C; <a href="#">Fig. 10</a>	-	-	1.2	V
V <sub>GT</sub>	gate trigger voltage	V <sub>D</sub> = 400 V; I <sub>T</sub> = 100 mA; T <sub>j</sub> = 125 °C	0.15	-	-	V
		V <sub>D</sub> = 12 V; I <sub>T</sub> = 100 mA; T <sub>j</sub> = 25 °C	-	-	0.9	V
I <sub>D</sub>	off-state current	V <sub>D</sub> = 600 V; T <sub>j</sub> = 25 °C	-	-	2	μA
		V <sub>D</sub> = 600 V; T <sub>j</sub> = 125 °C	-	-	0.2	mA
V <sub>CL</sub>	clamping voltage	I <sub>CL</sub> = 0.1 mA; t <sub>p</sub> = 1 ms; T <sub>j</sub> ≤ 125 °C	650	-	-	V
<b>Dynamic characteristics</b>						
dV <sub>D</sub> /dt	rate of rise of off-state voltage	V <sub>DM</sub> = 402 V; T <sub>j</sub> = 125 °C; (V <sub>DM</sub> = 67% of V <sub>DRM</sub> ); exponential waveform; gate open circuit; <a href="#">Fig. 11</a>	300	-	-	V/μs
di <sub>com</sub> /dt	rate of change of commutating current	V <sub>D</sub> = 400 V; T <sub>j</sub> = 125 °C; I <sub>T(RMS)</sub> 1 A; dV <sub>com</sub> /dt = 15 V/μs; gate open circuit; <a href="#">Fig. 12</a> ; <a href="#">Fig. 13</a>	0.15	-	-	A/ms

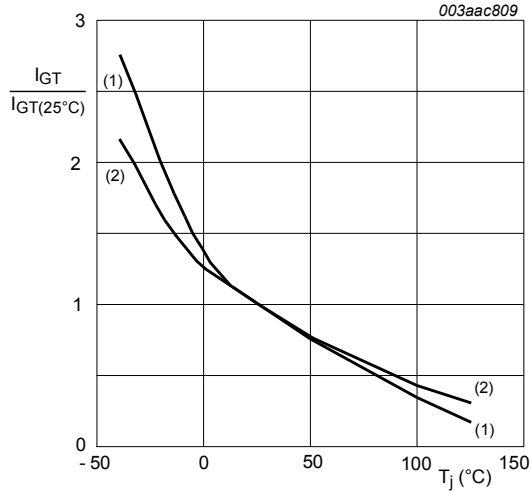


Fig. 7. Normalized gate trigger current as a function of junction temperature

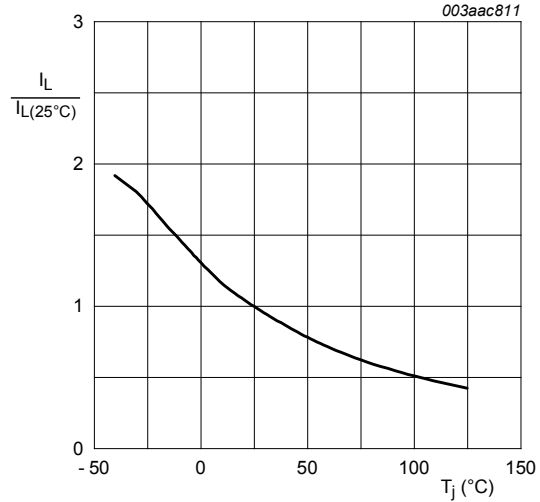


Fig. 8. Normalized latching current as a function of junction temperature

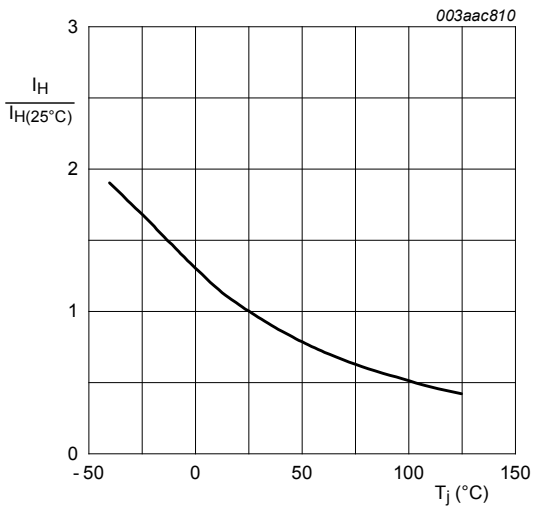
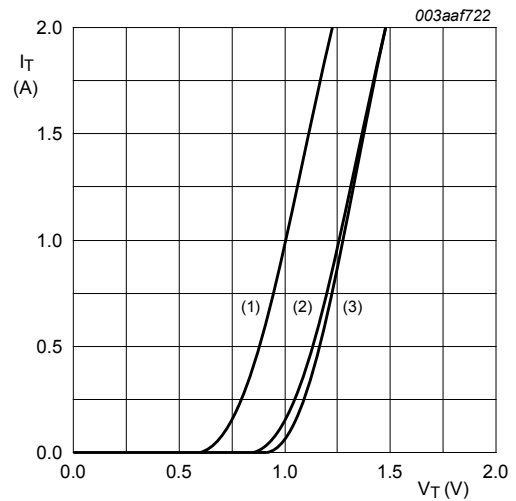


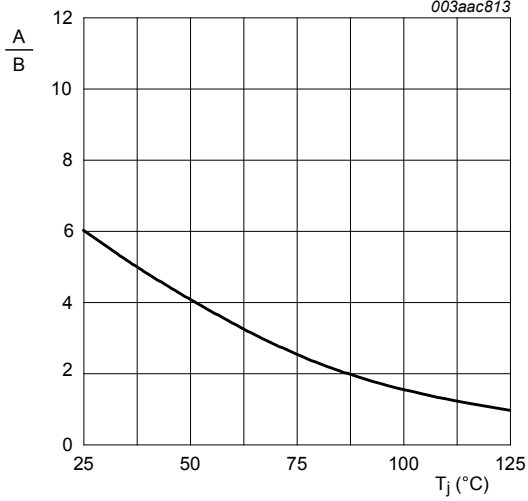
Fig. 9. Normalized holding current as a function of junction temperature



$V_o = 0.758 \text{ V}$ ;  $R_s = 0.263 \Omega$   
 (1)  $T_j = 125^{\circ}\text{C}$ ; typical values  
 (2)  $T_j = 125^{\circ}\text{C}$ ; maximum values  
 (3)  $T_j = 25^{\circ}\text{C}$ ; maximum values

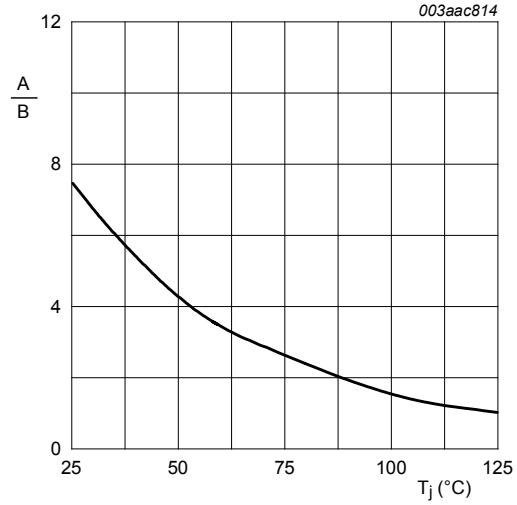
Fig. 10. On-state current as a function of on-state voltage





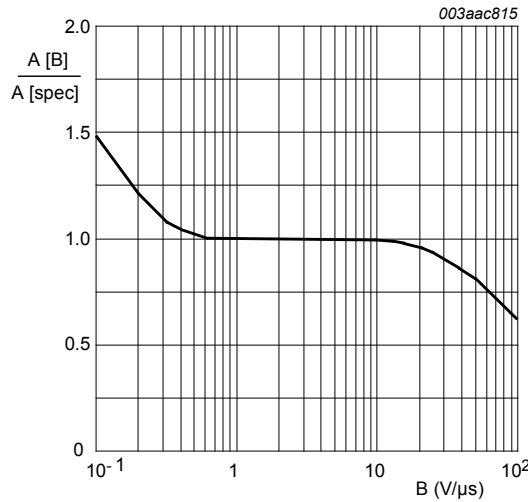
A =  $dV_D/dt$  at condition  $T_j$  °C  
 B =  $dV_D/dt$  at condition  $T_j$  [125] °C

**Fig. 11. Normalized rate of rise of off-state voltage as a function of junction temperature**



A =  $di_{com}/dt$  at condition  $T_j$  °C  
 B =  $di_{com}/dt$  at condition  $T_j$  [125] °C  
 $V_D = 400$  V

**Fig. 12. Normalized critical rate of rise of commutating current as a function of junction temperature**



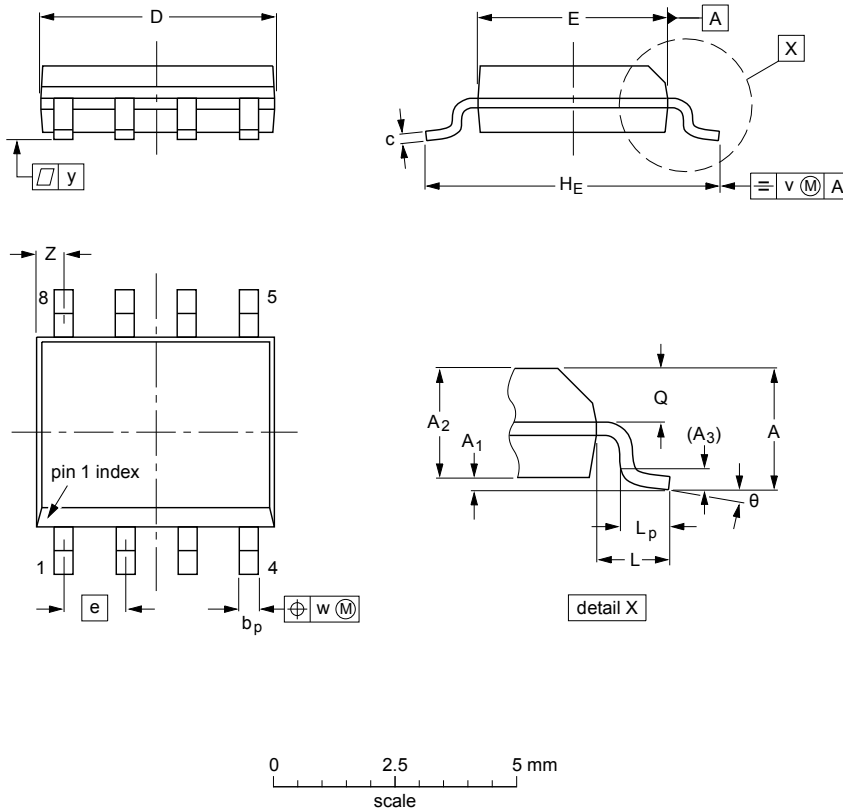
A [B] =  $di_{com}/dt$  at condition B,  $dV_{com}/dt$   
 A [spec] is the data sheet value for  $di_{com}/dt$   
 turn-off time is less than 20 ms

**Fig. 13. Normalized critical rate of change of commutating current as a function of critical rate of change of commutating voltage; minimum values**

10. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT96-1	076E03	MS-012				99-12-27- 03-02-18

Fig. 14. Package outline SO8 (SOT96-1)

### 11. Soldering

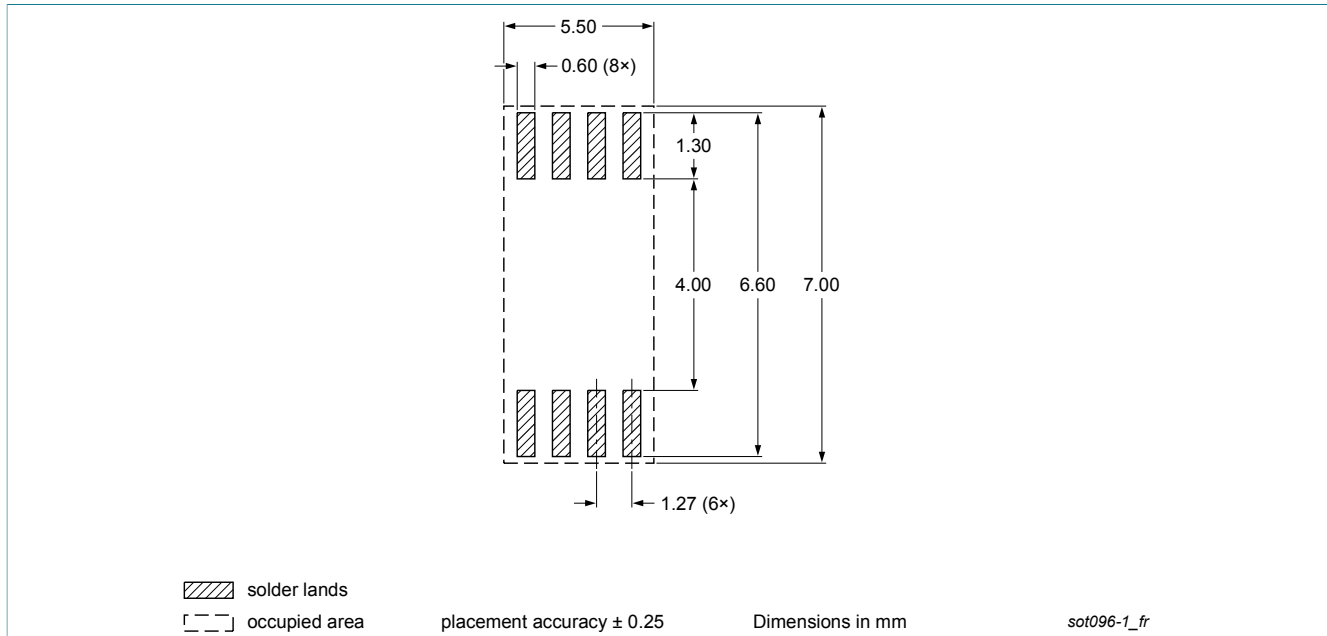


Fig. 15. Reflow soldering footprint for SO8 (SOT96-1)

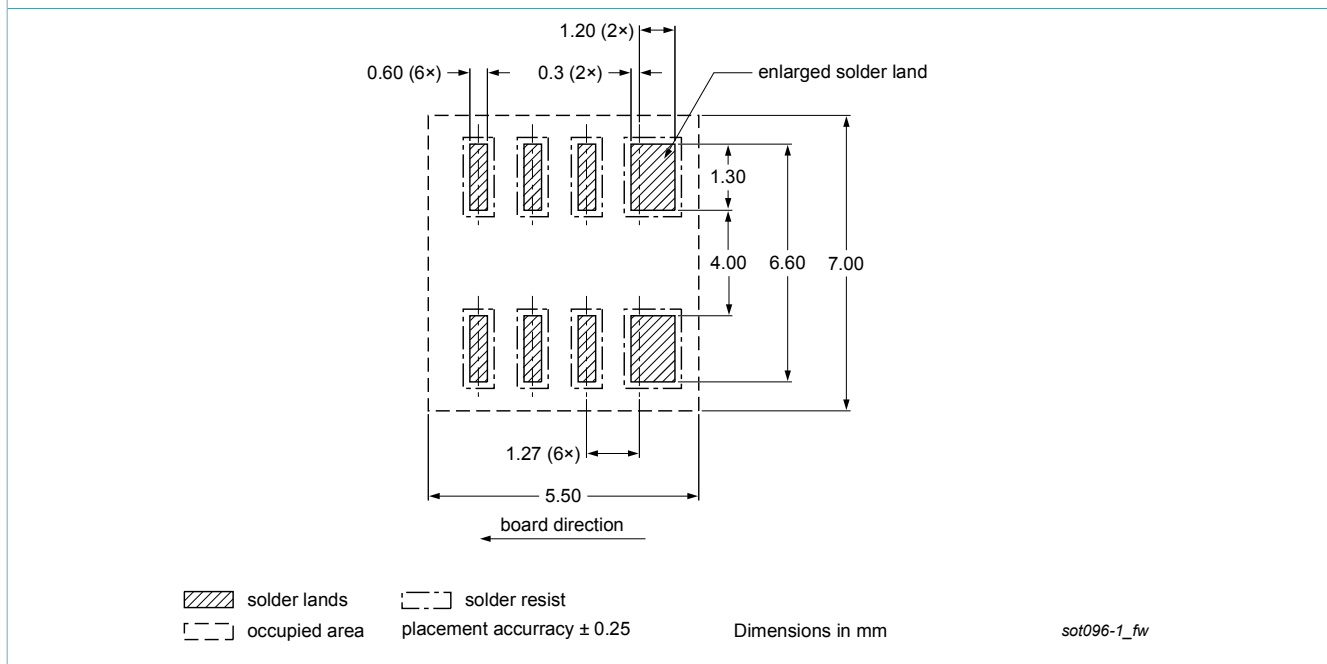


Fig. 16. Wave soldering footprint for SO8 (SOT96-1)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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**Date of release: 20 August 2014**