BT151-1000RT

SCR

13 March 2014 Product data sheet

1. General description

Planar passivated Silicon Controlled Rectifier (SCR) in a SOT78 (TO-220AB) plastic package intended for use in applications requiring very high bidirectional blocking voltage capability, high junction temperature capability and high thermal cycling performance.

2. Features and benefits

- High junction operating temperature capability
- High thermal cycling performance
- Planar passivated for voltage ruggedness and reliability
- Very high bidirectional blocking voltage capability

3. Applications

- Capacitive Discharge Ignition (CDI)
- Crowbar protection
- Inrush protection
- Motor control
- Voltage regulation

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	-	1000	V
V_{RRM}	repetitive peak reverse voltage			-	-	1000	V
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)}$ = 25 °C; t_p = 10 ms; Fig. 4; Fig. 5		-	-	120	A
T_j	junction temperature			-	-	150	°C
$I_{T(RMS)}$	RMS on-state current	half sine wave; T_{mb} ≤ 134 °C; Fig. 1; Fig. 2; Fig. 3		-	-	12	A
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA

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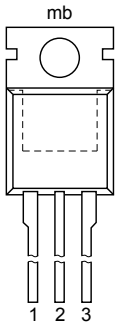
5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 TO-220AB (SOT78)	
2	A	anode		
3	G	gate		
mb	A	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BT151-1000RT	TO-220AB	plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB	SOT78

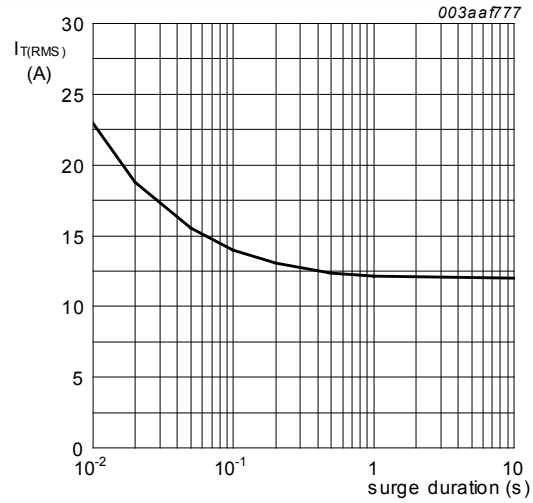
7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage			-	1000	V
V_{RRM}	repetitive peak reverse voltage			-	1000	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{mb} \leq 134$ °C		-	7.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{mb} \leq 134$ °C; Fig. 1; Fig. 2; Fig. 3		-	12	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25$ °C; $t_p = 10$ ms; Fig. 4; Fig. 5		-	120	A
		half sine wave; $T_{j(init)} = 25$ °C; $t_p = 8.3$ ms		-	132	A
I^2t	I^2t for fusing	$t_p = 10$ ms; SIN		-	72	A^2s
dI_T/dt	rate of rise of on-state current	$I_T = 20$ A; $I_G = 50$ mA; $dI_G/dt = 50$ mA/µs		-	50	A/µs
I_{GM}	peak gate current			-	2	A

Symbol	Parameter	Conditions		Min	Max	Unit
V_{RGM}	peak reverse gate voltage			-	5	V
P_{GM}	peak gate power			-	5	W
$P_{G(AV)}$	average gate power	over any 20 ms period		-	0.5	W
T_{stg}	storage temperature			-40	150	°C
T_j	junction temperature			-	150	°C



f = 50 Hz; T_{mb} = 134 °C

Fig. 1. RMS on-state current as a function of surge duration; maximum values

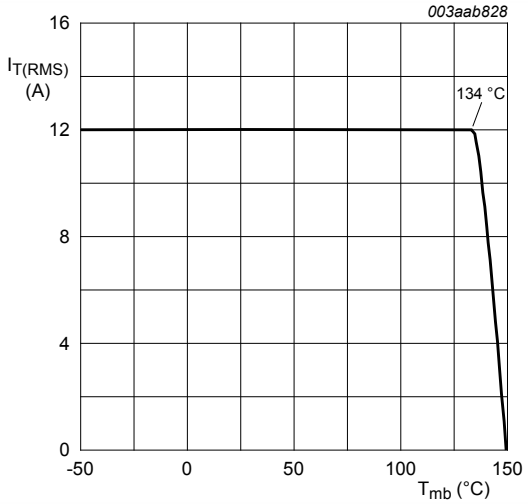
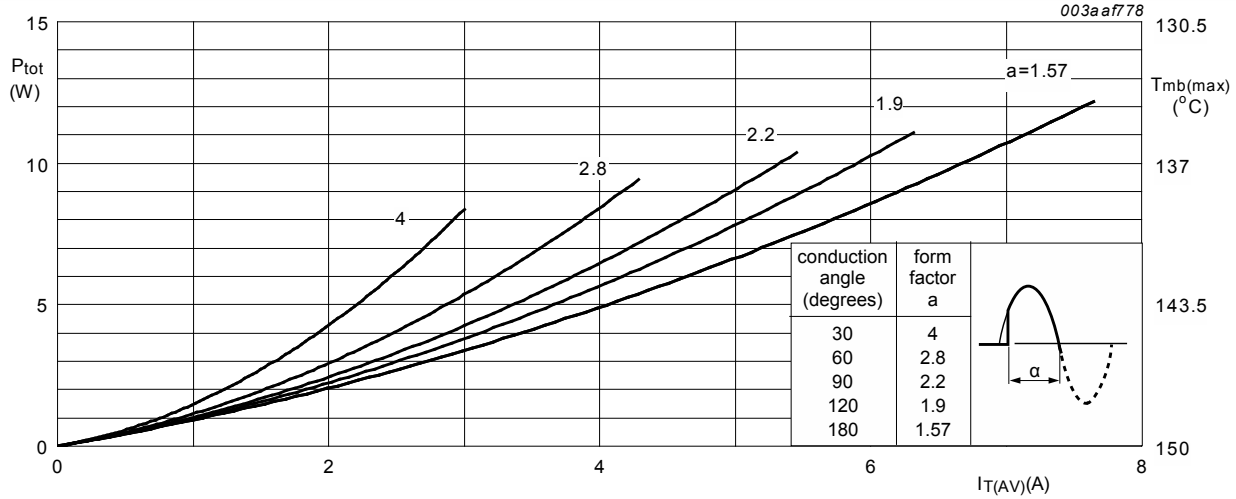


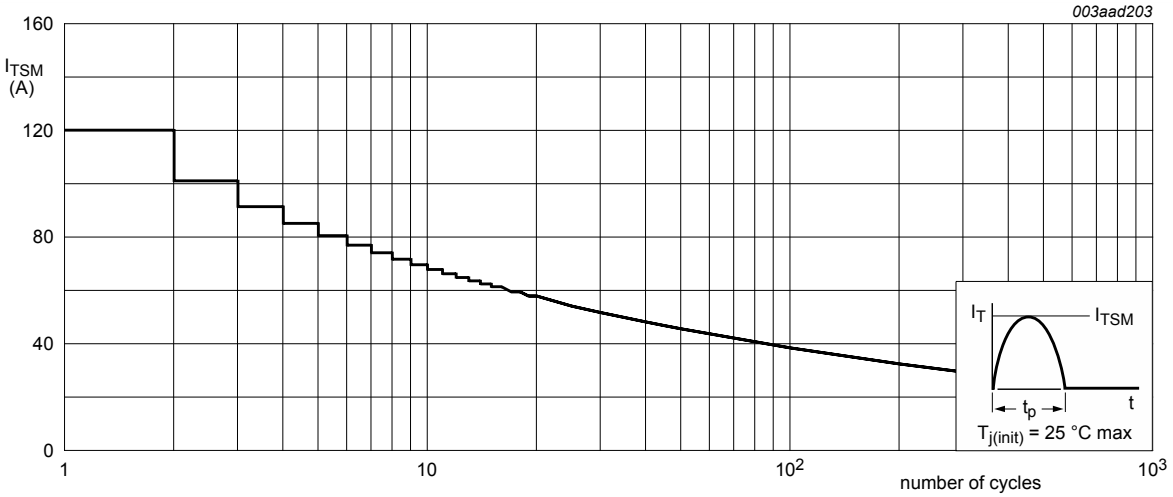
Fig. 2. RMS on-state current as a function of mounting base temperature; maximum values



α = conduction angle

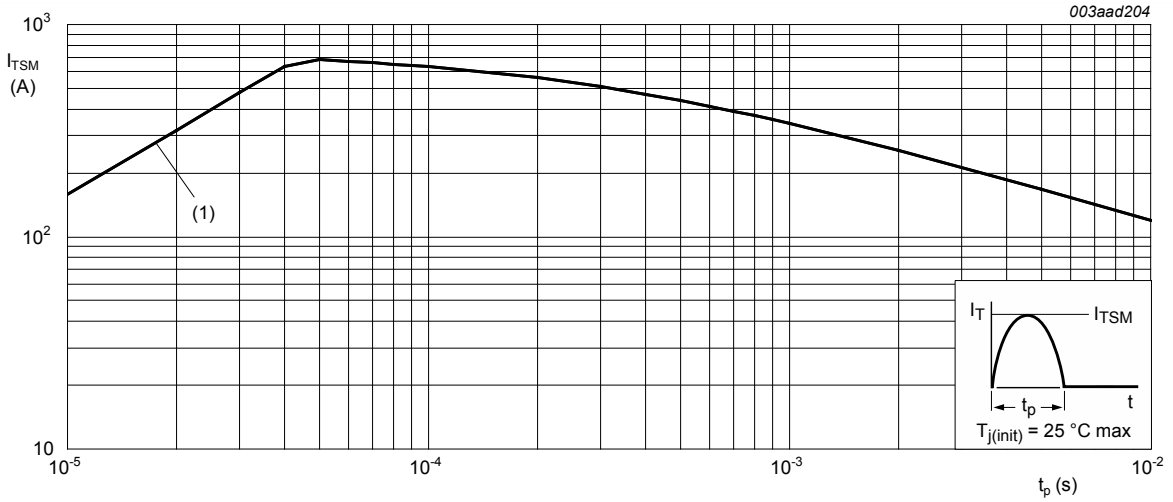
a = form factor = $I_{T(RMS)}$ / $I_{T(AV)}$

Fig. 3. Total power dissipation as a function of average on-state current; maximum values



f = 50 Hz

Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



$t_p \leq 10$ ms

(1) dI_T/dt limit

Fig. 5. Non-repetitive peak on-state current as a function of pulse width for sinusoidal currents; maximum values

8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Fig. 6		-	-	1.3	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air		-	60	-	K/W

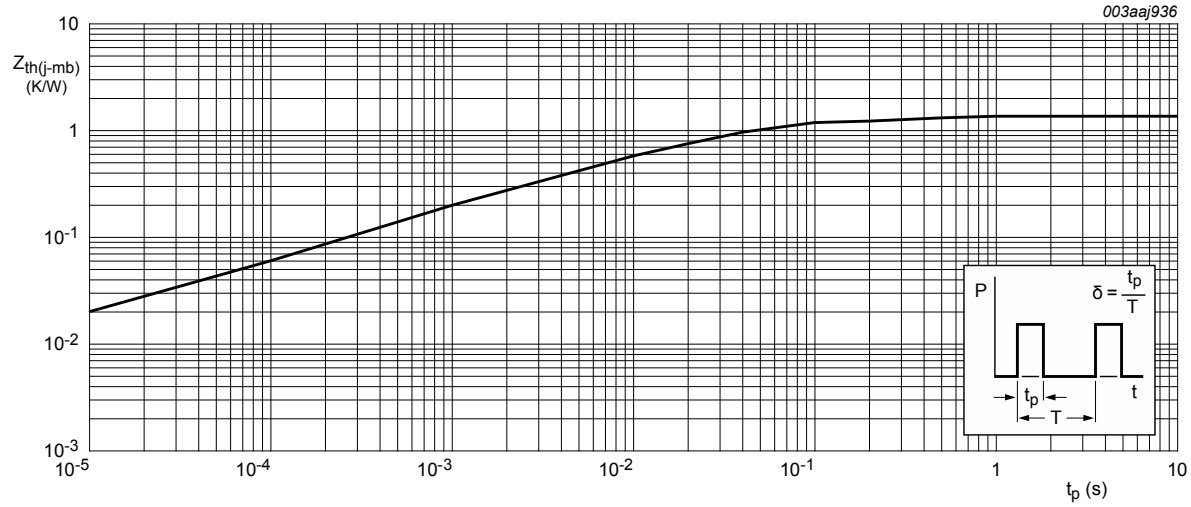


Fig. 6. Transient thermal impedance from junction to mounting base as a function of pulse width

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Static characteristics							
I_{GT}	gate trigger current	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 7		-	2	15	mA
I_L	latching current	V_D = 12 V; I_G = 0.1 A; T_j = 25 °C; Fig. 8		-	10	40	mA
I_H	holding current	V_D = 12 V; T_j = 25 °C; Fig. 9		-	7	20	mA
V_T	on-state voltage	I_T = 23 A; T_j = 25 °C; Fig. 10		-	1.4	1.75	V
V_{GT}	gate trigger voltage	V_D = 12 V; I_T = 0.1 A; T_j = 25 °C; Fig. 11		-	0.6	1	V
		V_D = 1000 V; I_T = 0.1 A; T_j = 150 °C; Fig. 11		0.25	0.4	-	V
I_D	off-state current	V_D = 1000 V; T_j = 150 °C		-	0.5	2.5	mA
I_R	reverse current	V_R = 1000 V; T_j = 150 °C		-	0.5	2.5	mA
Dynamic characteristics							
dV_D/dt	rate of rise of off-state voltage	V_{DM} = 670 V; T_j = 150 °C; (V_{DM} = 67% of V_{DRM}); exponential waveform; gate open circuit; Fig. 12		-	300	-	V/µs
t_{gt}	gate-controlled turn-on time	I_{TM} = 40 A; V_D = 1000 V; I_G = 0.1 A; dI_G/dt = 5 A/µs; T_j = 25 °C		-	2	-	µs
t_q	commutated turn-off time	V_{DM} = 670 V; T_j = 150 °C; I_{TM} = 20 A; V_R = 25 V; $(dI_T/dt)_M$ = 30 A/µs; dV_D/dt = 50 V/µs; R_{GK} = 100 Ω; (V_{DM} = 67% of V_{DRM})		-	70	-	µs

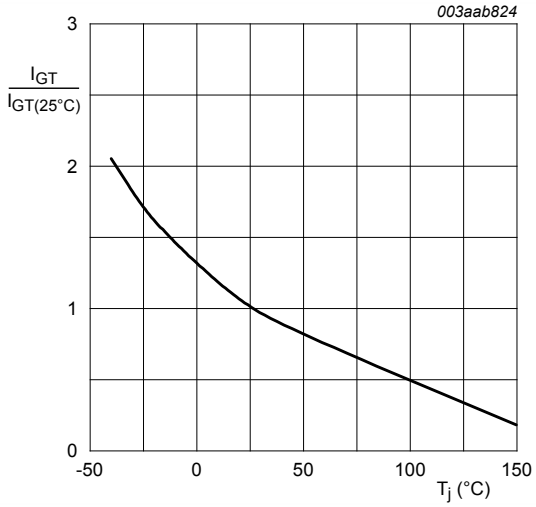


Fig. 7. Normalized gate trigger current as a function of junction temperature

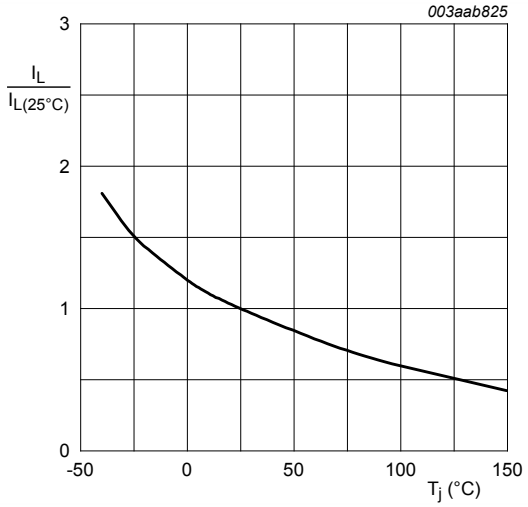


Fig. 8. Normalized latching current as a function of junction temperature

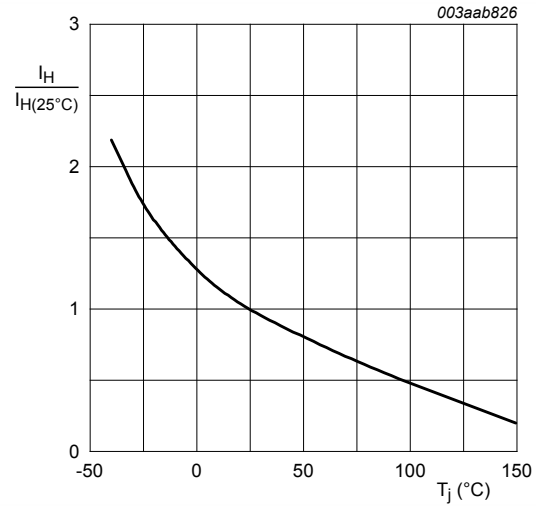
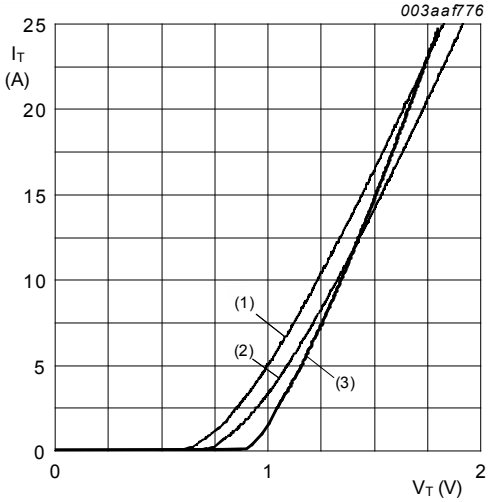


Fig. 9. Normalized holding current as a function of junction temperature



Vo = 0.825 V; Rs = 0.41 Ω
(1) Tj = 150°C; typical values
(2) Tj = 150°C; maximum values
(3) Tj = 25°C; maximum values

Fig. 10. On-state current as a function of on-state voltage

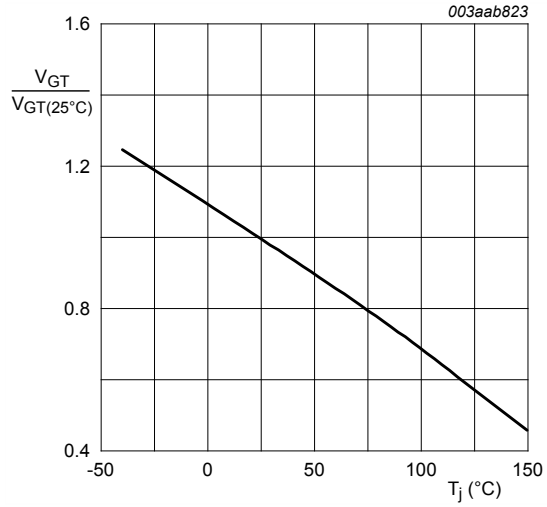
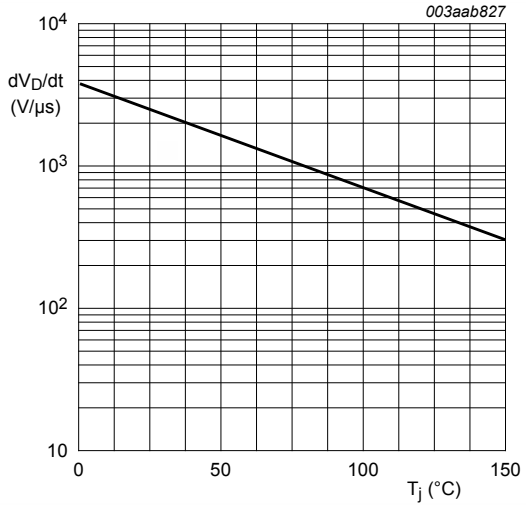


Fig. 11. Normalized gate trigger voltage as a function of junction temperature

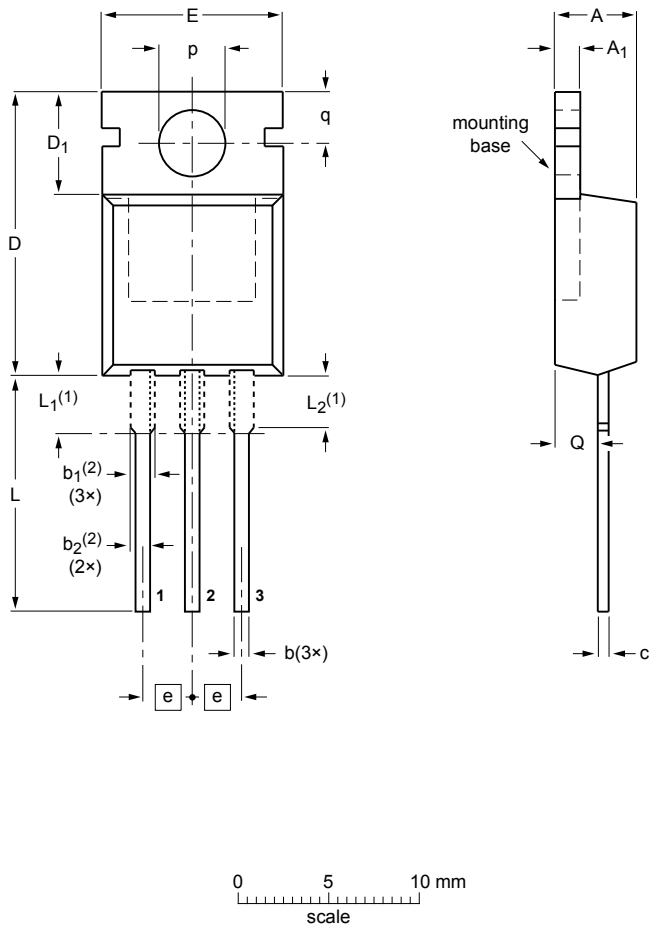


gate open circuit

Fig. 12. Critical rate of rise of off-state voltage as a function of junction temperature; typical values

10. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1(2)	b_2(2)	c	D	D_1	E	e	L	L_1(1)	L_2(1) max.	p	q	Q
mm	4.7 4.1	1.40 1.25	0.9 0.6	1.6 1.0	1.3 1.0	0.7 0.4	16.0 15.2	6.6 5.9	10.3 9.7	2.54	15.0 12.8	3.30 2.79	3.0	3.8 3.5	3.0 2.7	2.6 2.2

Notes

1. Lead shoulder designs may vary.
2. Dimension includes excess dambar.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT78		3-lead TO-220AB	SC-46			~~08-04-23~~ 08-06-13

Fig. 13. Package outline TO-220AB (SOT78)

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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