Unit: mm

TOSHIBA Diode Silicon Epitaxial Planar Type

# **1SS201**

## Ultra High Speed Switching Application

Low forward voltage : VF (3) = 0.9V (typ.)
Fast reverse recovery time: t<sub>rr</sub> = 1.6ns (typ.)
Small total capacitance : CT = 0.9pF (typ.)

### **Absolute Maximum Ratings (Ta = 25°C)**

Characteristic	Symbol	Rating	Unit
Maximum (peak) reverse voltage	$V_{RM}$	85	V
Reverse voltage	V <sub>R</sub>	80	$(\nearrow)$
Maximum (peak) forward current	I <sub>FM</sub>	300 (*)	mA
Average forward current	Io	100 (*)	mΑ
Surge current (10ms)	I <sub>FSM</sub>	2 (*)	A
Power dissipation	Р	200	mW
Junction temperature	Tj	125	°C
Storage temperature range	T <sub>stg</sub>	-55~125	/°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in

temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

(\*) Unit rating. Total rating = Unit rating ×1.5.

#### Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Circuit	Test Condition	Min	Тур.	Max	Unit
	V <sub>F</sub> (t)	_	I <sub>F</sub> = 1mA		0.60	_	
Forward voltage	VF (2)	_	I <sub>F</sub> = 10mA	1	0.72	_	V
	VF(3)	_	I <sub>F</sub> = 100mA		0.90	1.20	
Reverse-current	IR (1)	_	V <sub>R</sub> = 30V		1	0.1	μA
Nevelse-current	I <sub>R</sub> (2)	_	V <sub>R</sub> = 80V	1	l	0.5	μ
Total capacitance	√ C <sub>T</sub>	_	V <sub>R</sub> = 0, f = 1MHz		0.9	3.0	pF
Reverse recovery time	t <sub>rr</sub>	_	I <sub>F</sub> = 10mA (Fig.1)	_	1.6	4.0	ns

4.2MAX. 4.2MAX. 80 0.55MAX. 1.27.127 0.60 1 2. CATHODE 1, 2 3. ANODE 2

1-4E2A

Weight: 0.13g (typ.)

JEITA TOSHIBA

2007-11-01

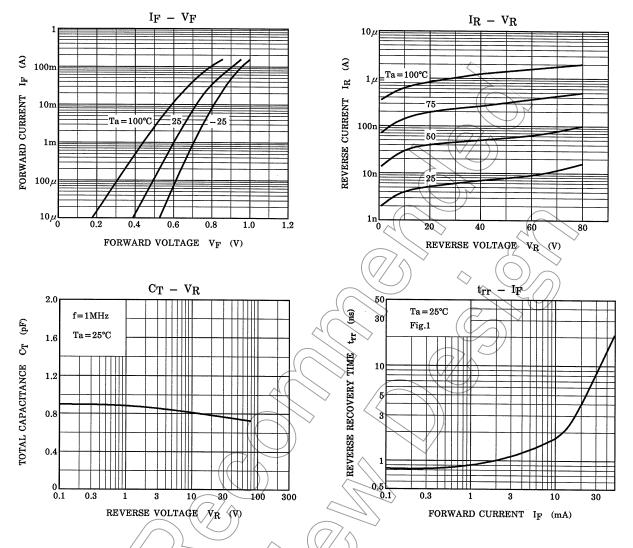
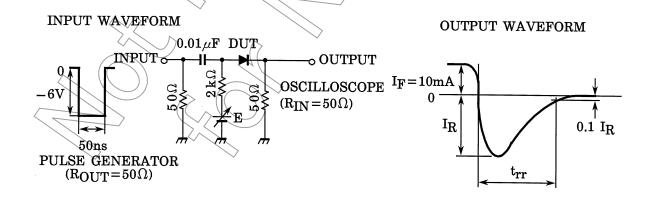


Fig.1 Reverse recovery time (trr) test circuit



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