MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

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Designer's Data Sheet

TMOS E-FET
High Energy Power FET
N-Channel Enhancement-Mode Silicon Gate

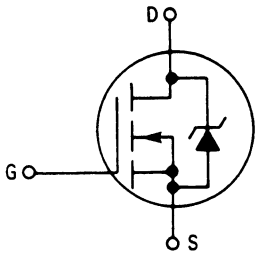
MTM24N45E

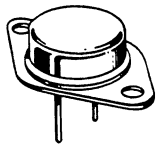
TMOS POWER FET
24 AMPERES
$r_{DS(on)}$ = 0.2 OHMS
450 VOLTS

This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads. The avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltge transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode

TMOS™





CASE 197A-02
TO-204AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	450	Vdc
Drain-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	450	Vdc
Gate-Source Voltage — Continuous — Non-repetitive	V_{GS} V_{GSM}	±20 ±40	Vdc Vpk
Drain Current — Continuous — Pulsed	I_D I_{DM}	24 85	Adc
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	300 2.4	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T_J = 25°C — T_J = 100°C Repetitive Pulse Drain-to-Source Avalanche Energy	$W_{DSS(1)}$ $W_{DSR(2)}$	1200 160 30	mJ

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	0.416 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

(1) V_{DD} = 50 V, I_D = 24 A.
(2) Pulse Width and frequency is limited by T_J(max) and thermal response.

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Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)		$V_{(BR)DSS}$	450	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 450 V, V_{GS} = 0) (V_{DS} = 360 V, V_{GS} = 0, T_J = 125°C)		I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)		I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)		I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) (T_J = 125°C)		$V_{GS(th)}$	2.0 1.5	— —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 12 A)		$r_{DS(on)}$	—	—	0.2	Ohms
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 24 A) (I_D = 12 A, T_J = 125°C)		$V_{DS(on)}$	 — —	 — —	 8.0 8.0	Vdc
Forward Transconductance (V_{DS} = 15 Vdc, I_D = 12 A)		g_{FS}	13	—	—	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	4000	—	pF
Output Capacitance		C_{oss}	—	520	—	
Transfer Capacitance		C_{rss}	—	115	—	
SWITCHING CHARACTERISTICS*						
Turn-On Delay Time	(V_{DD} = 225 V, $I_D \approx$ 24 A, R_G = 4.3 Ω, $V_{GS(on)}$ = 10 V)	$t_{d(on)}$	—	32	—	ns
Rise Time		t_r	—	95	—	
Turn-Off Delay Time		$t_{d(off)}$	—	75	—	
Fall Time		t_f	—	80	—	
Total Gate Charge	(V_{DS} = 360 V, I_D = 24 A, V_{GS} = 10 V)	Q_g	—	115	140	nC
Gate-Source Charge		Q_{gs}	—	21	—	
Gate-Drain Charge		Q_{gd}	—	60	—	
SOURCE-DRAIN DIODE CHARACTERISTICS						
Forward On-Voltage	(I_S = 24 A, di/dt = 100 A/μs)	V_{SD}	—	—	1.6	Vdc
Forward Turn-On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	500	1000	
INTERNAL PACKAGE INDUCTANCE						
Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and center of the die)		L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source pin 0.25" from package to source bond pad)		L_S	—	12.5	—	

*Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2.0%.
**Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

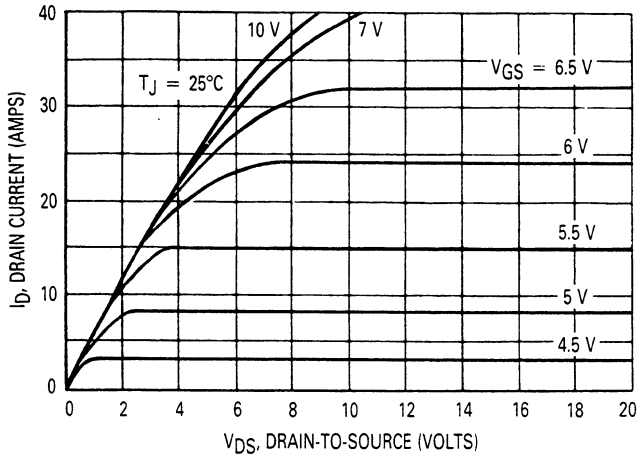


Figure 2. Gate-Threshold Voltage Variation With Temperature

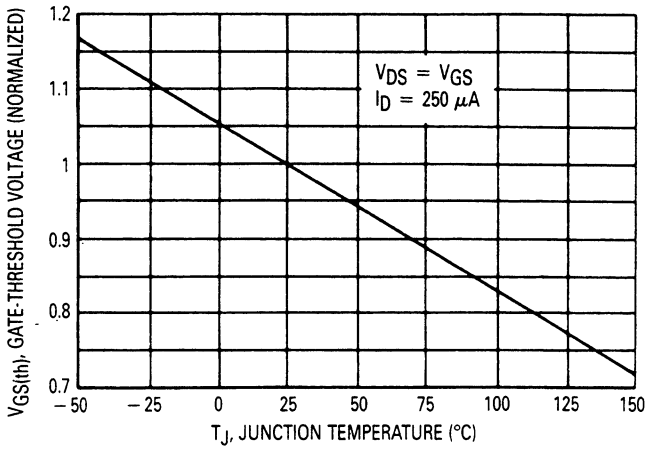


Figure 3. Transfer Characteristics

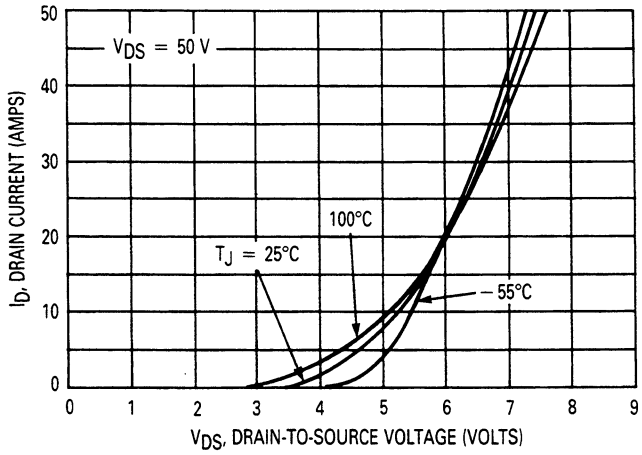


Figure 4. Breakdown Voltage Variation With Temperature

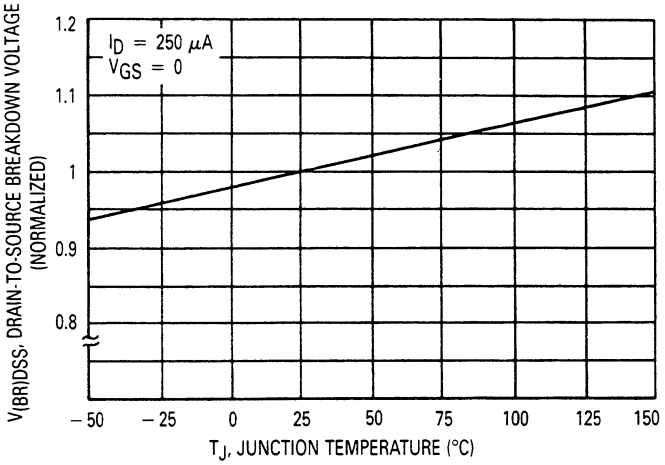


Figure 5. On-Resistance versus Drain Current

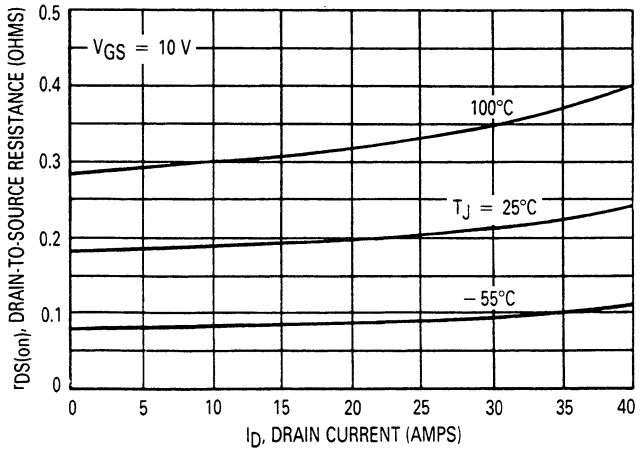
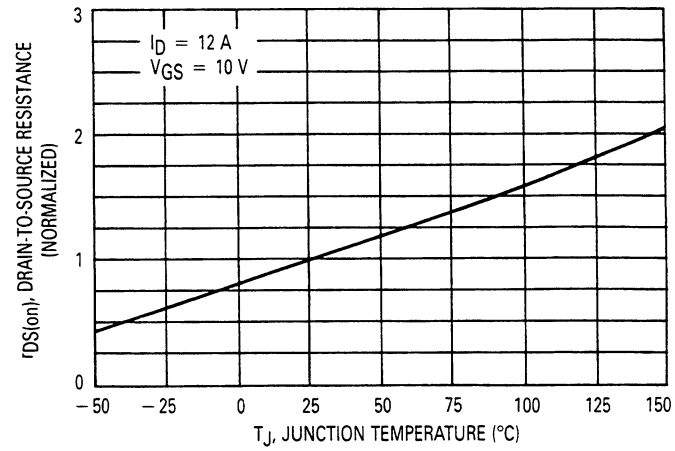


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

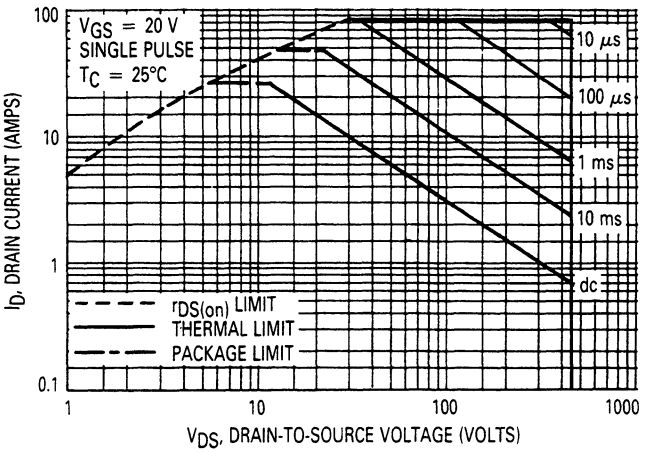
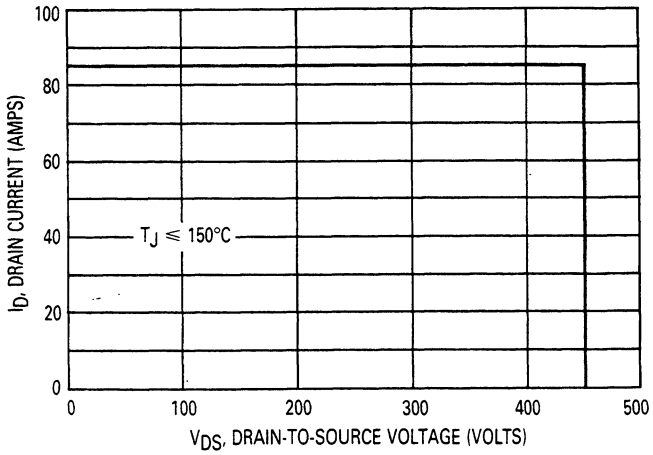


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

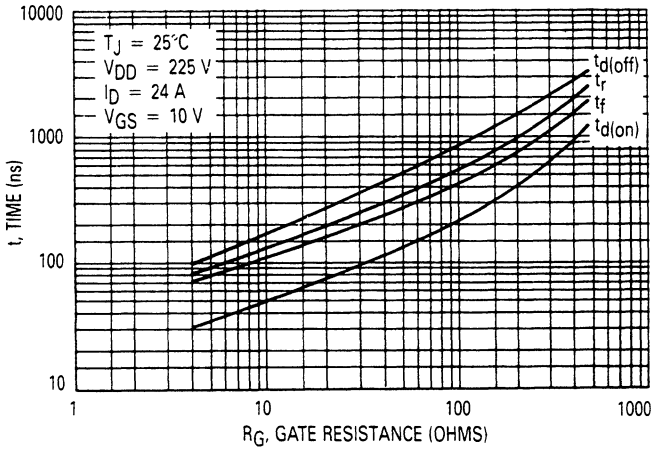
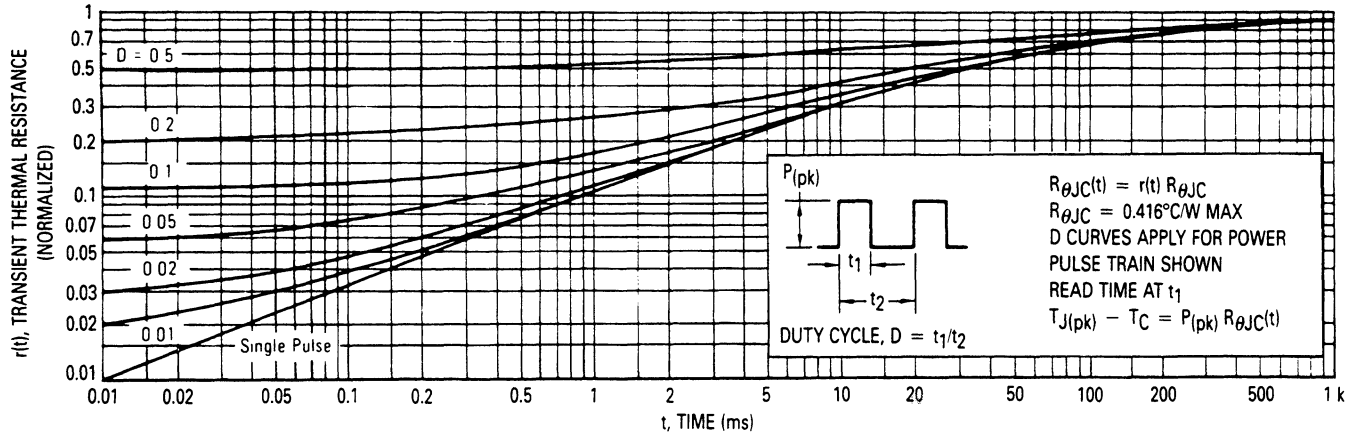


Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

Figure 12. Commutating Safe Operating Area (CSOA)

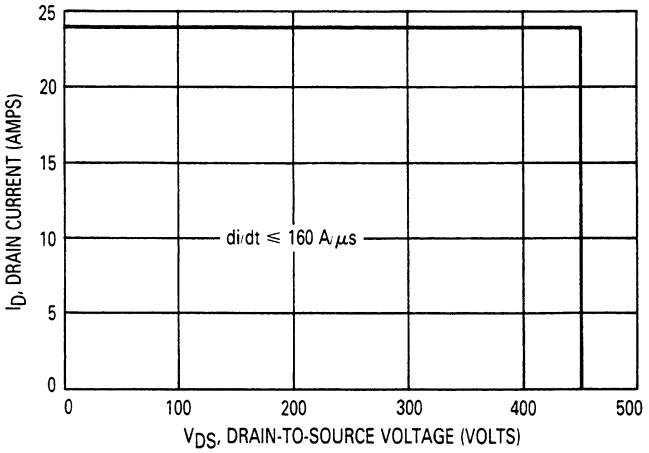


Figure 14. Unclamped Inductive Switching Test Circuit

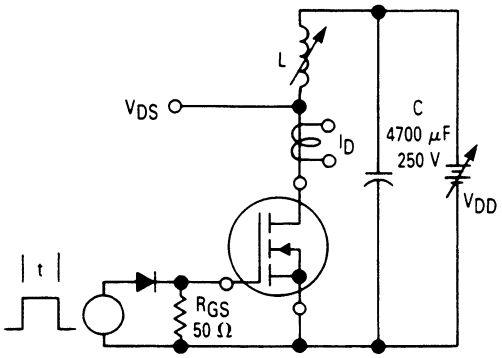


Figure 11. Commutating Waveforms

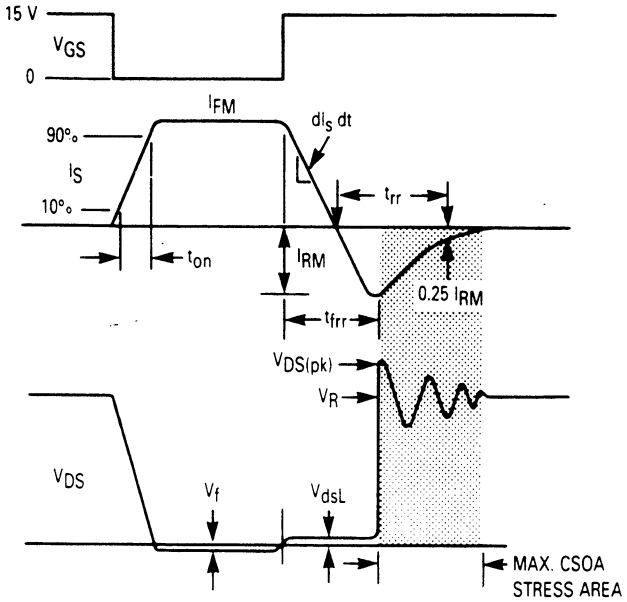


Figure 13. Commutating Safe Operating Area Test Circuit

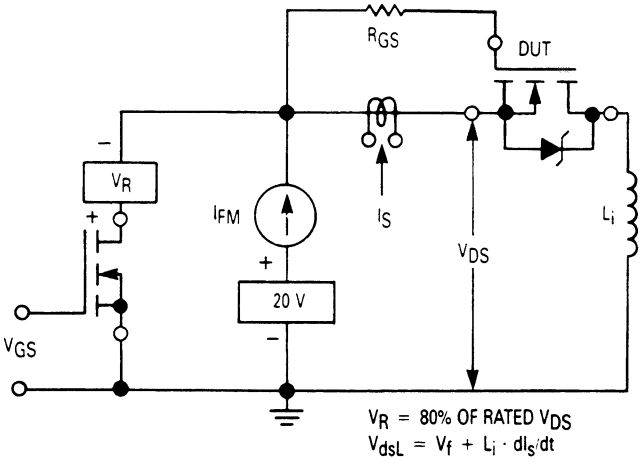
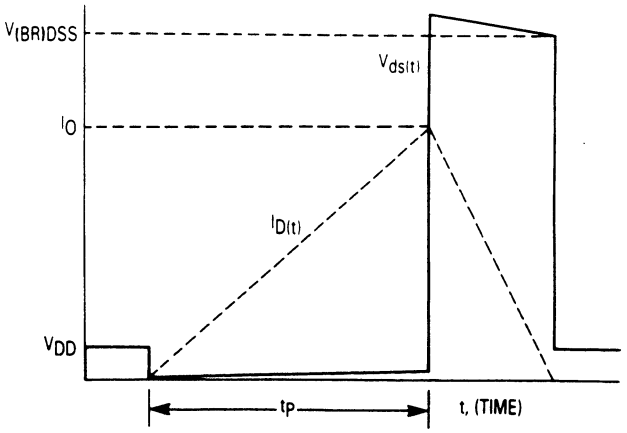


Figure 15. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 16. Capacitance Variation

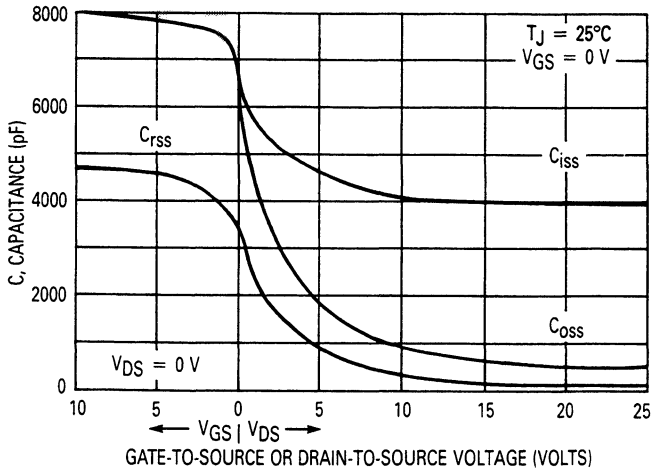


Figure 17. Gate Charge versus Gate-to-Source Voltage

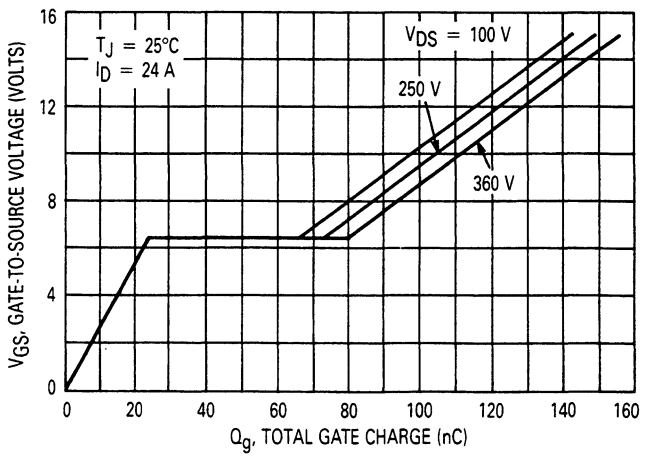
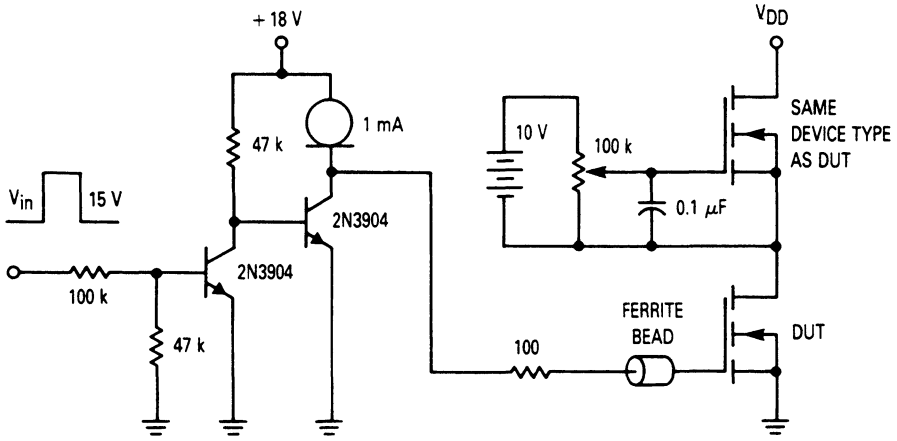
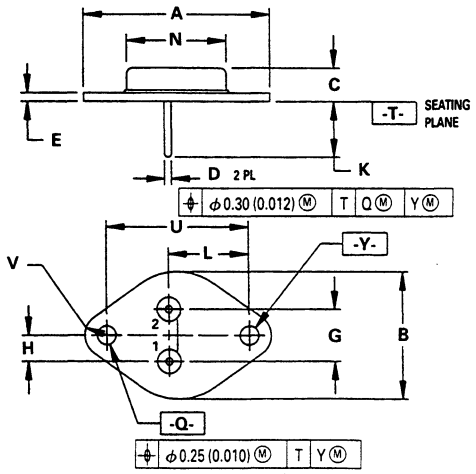


Figure 18. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

OUTLINE DIMENSIONS



CASE 197A-02
TO-204AE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	38.86 REF		1.530 REF	
B	25.15	26.67	0.990	1.050
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
K	11.18	12.19	0.440	0.480
L	16.89 BSC		0.665 BSC	
N	19.31	21.08	0.760	0.830
Q	3.84	4.19	0.151	0.165
U	30.15 BSC		1.187 BSC	
V	3.33	4.77	0.131	0.188

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