

MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Designer's Data Sheet

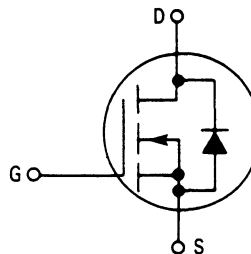
TMOS E-FET

High Energy Power FET

N-Channel Enhancement-Mode Silicon Gate

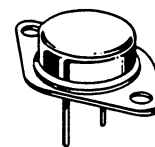
This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode



MTM10N100E

TMOS POWER FET
10 AMPERES
r_{DS(on)} = 1.2 OHMS
1000 VOLTS



CASE 197A-02
TO-204AE

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V _{DSS}	1000	Volts
Drain-to-Gate Voltage, R _{GS} = 1.0 MΩ	V _{DGR}	1000	Vdc
Gate-to-Source Voltage — Continuous — Non-Repetitive	V _{GS} V _{GSM}	± 20 ± 40	Vdc
Drain Current — Continuous — Pulsed	I _D I _{DM}	10 40	Adc
Total Power Dissipation @ T _C = 25°C Derate above 25°C	P _D	300 2.4	Watts W/°C
Operating and Storage Temperature Range	T _J , T _{stg}	-55 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T _J = 25°C — T _J = 100°C	W _{DSS} (1)	1000 160	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	W _{DSS} (2)	30	

THERMAL CHARACTERISTICS

Thermal Resistance — Junction to Case — Junction-to-Ambient	R _{θJC} R _{θJA}	0.416 30	°C/W
Maximum Lead Temperature for Soldering Purposes 1/8" from Case for 5 seconds	T _L	275	°C

(1) V_{DD} = 50 V, I_D = 10 A

(2) Pulse Width and frequency is limited by T_{J(max)} and thermal response

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

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MOTOROLA

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage ($V_{GS} = 0, I_D = 0.25 \text{ mA}$)	$V_{(BR)DSS}$	1000	—	—	Vdc
Zero Gate Voltage Drain Current ($V_{DS} = 1000 \text{ V}, V_{GS} = 0$) ($V_{DS} = 1000 \text{ V}, V_{GS} = 0, T_J = 125^\circ\text{C}$)	I_{DSS}	—	—	0.25 1.0	mAdc
Gate-Body Leakage Current — Forward ($V_{GSF} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse ($V_{GSR} = 20 \text{ Vdc}, V_{DS} = 0$)	I_{GSSR}	—	—	100	nAdc

ON CHARACTERISTICS*

Gate Threshold Voltage ($V_{DS} = V_{GS}, I_D = 0.25 \text{ mAdc}$) ($T_J = 125^\circ\text{C}$)	$V_{GS(th)}$	2.0 1.5	3.0 —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance ($V_{GS} = 10 \text{ Vdc}, I_D = 5.0 \text{ Adc}$)	$r_{DS(on)}$	—	—	1.2	Ohms
Drain-to-Source On-Voltage ($V_{GS} = 10 \text{ Vdc}$) ($I_D = 10 \text{ A}$) ($I_D = 5.0 \text{ A}, T_J = 125^\circ\text{C}$)	$V_{DS(on)}$	—	—	14 14	Vdc
Forward Transconductance ($V_{DS} = 15 \text{ Vdc}, I_D = 5.0 \text{ Adc}$)	g_{FS}	5.0	—	—	mhos

DYNAMIC CHARACTERISTICS

Input Capacitance	$(V_{DS} = 25 \text{ V}, V_{GS} = 0, f = 1.0 \text{ MHz})$	C_{iss}	—	3900	—	pF
Output Capacitance		C_{oss}	—	300	—	
Transfer Capacitance		C_{rss}	—	65	—	

SWITCHING CHARACTERISTICS*

Turn-On Delay Time	$(V_{DD} = 250 \text{ V}, I_D = 5.0 \text{ A}, R_{gen} = 4.3 \text{ ohms})$	$t_{d(on)}$	—	40	—	ns
Rise Time		t_r	—	100	—	
Turn-Off Delay Time		$t_{d(off)}$	—	100	—	
Fall Time		t_f	—	100	—	
Total Gate Charge	$(V_{DS} = 400 \text{ V}, I_D = 10 \text{ A}, V_{GS} = 10 \text{ V})$	Q_g	—	100	140	nC
Gate-Source Charge		Q_{gs}	—	20	—	
Gate-Drain Charge		Q_{gd}	—	40	—	

SOURCE-DRAIN DIODE CHARACTERISTICS


Forward On-Voltage	$(I_S = 10 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s})$	V_{SD}	—	—	1.5	Vdc
Forward Turn-On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	600	1000	

INTERNAL PACKAGE INDUCTANCE

Internal Drain Inductance (Measured from the contact screw on the header closer to the source pin and center of the die)	L_D	—	5.0	—	nH
Internal Source Inductance (Measured from the source pin 0.25" from package to source bond pad.)	L_S	—	12.5	—	

*Indicates Pulse Test: Pulse Width = 300 μs max, Duty Cycle = 2.0%.

**Limited by circuit inductance.

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TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

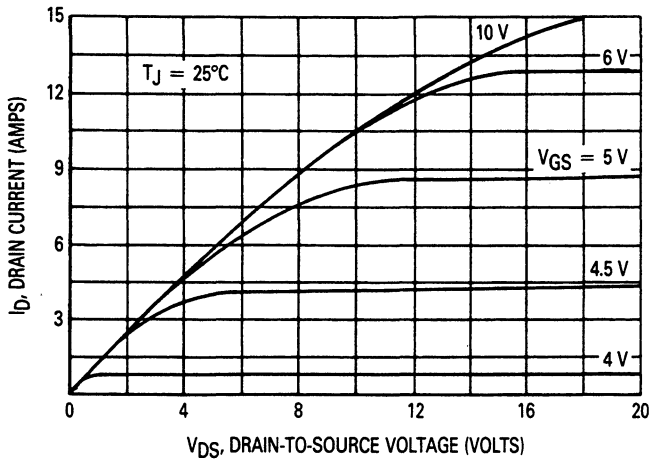


Figure 2. Gate Threshold Variation With Temperature

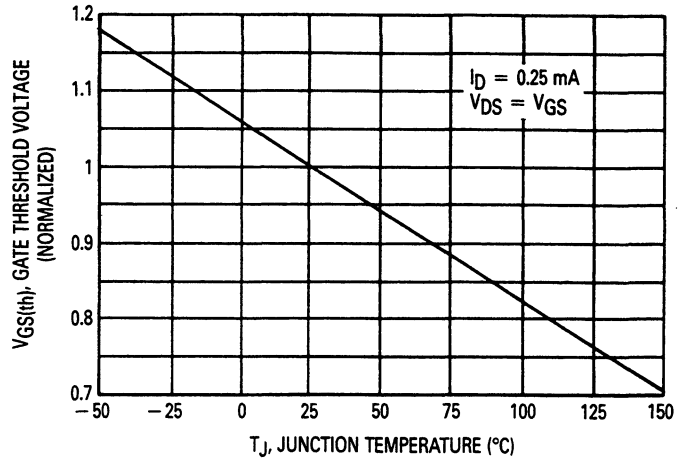


Figure 3. Transfer Characteristics

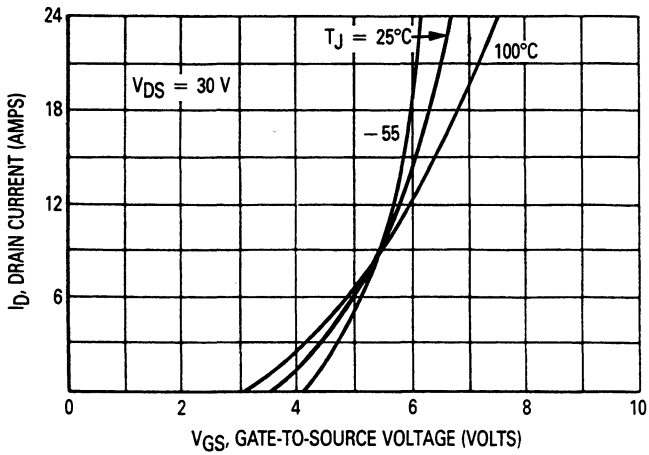


Figure 4. Breakdown Voltage Variation With Temperature

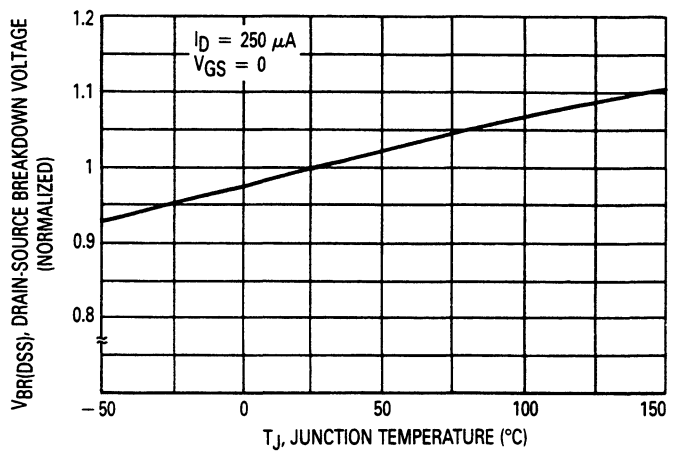


Figure 5. On-Resistance versus Drain Current

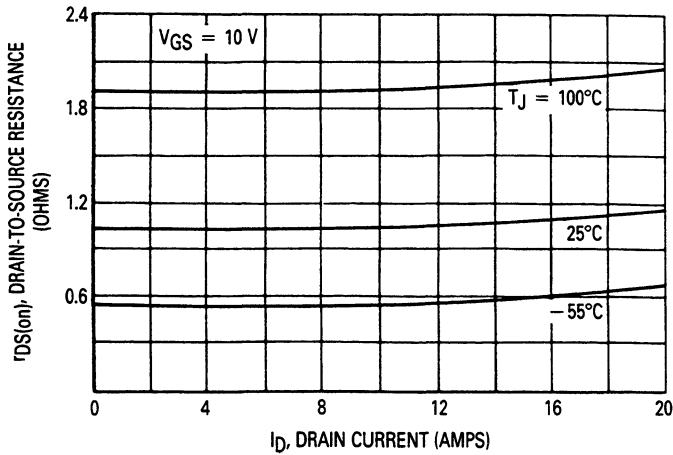
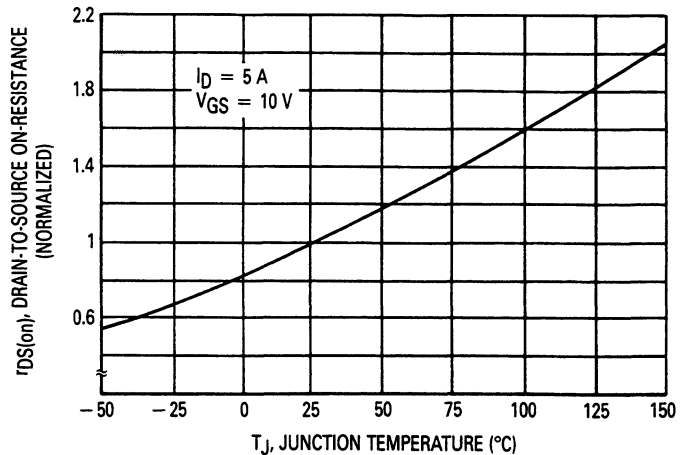
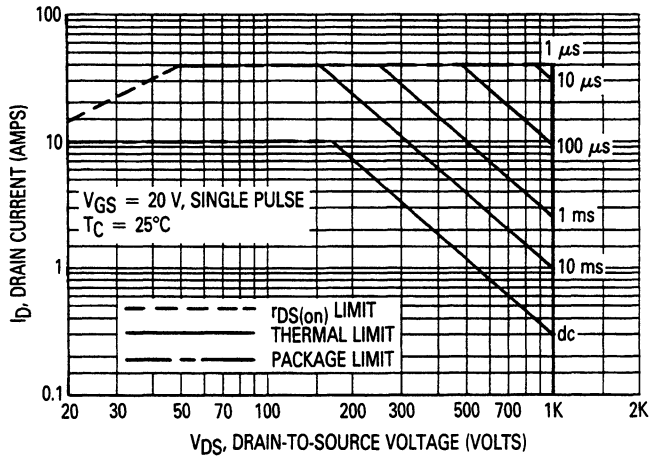


Figure 6. On-Resistance versus Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

Figure 8. Thermal Response

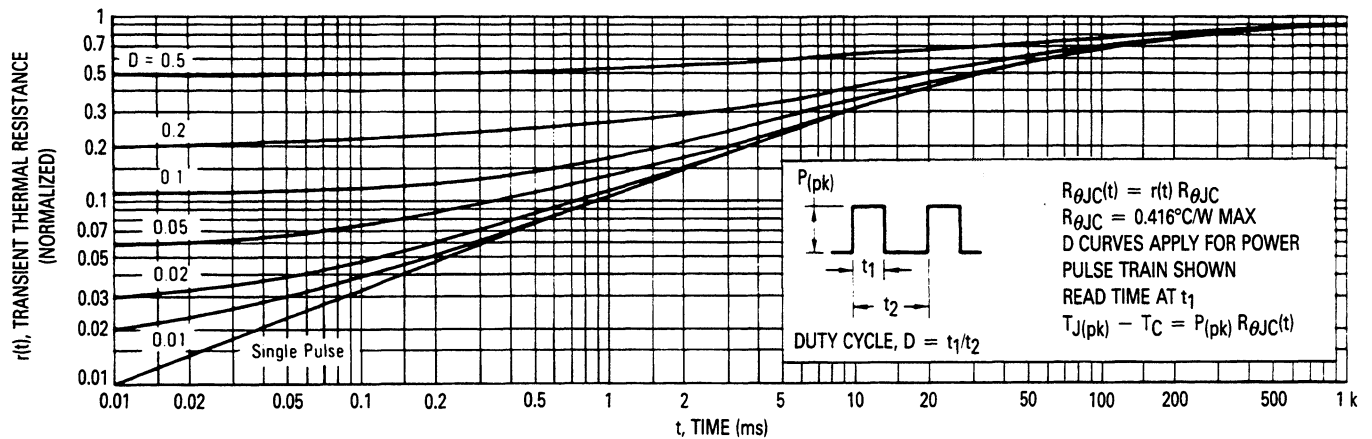


Figure 9. Capacitance Variation

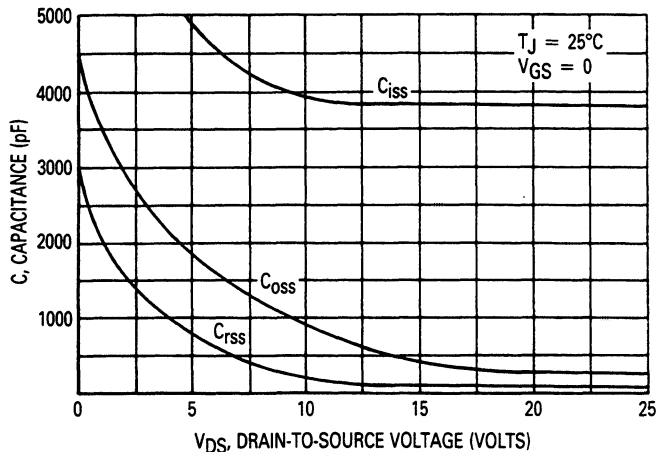
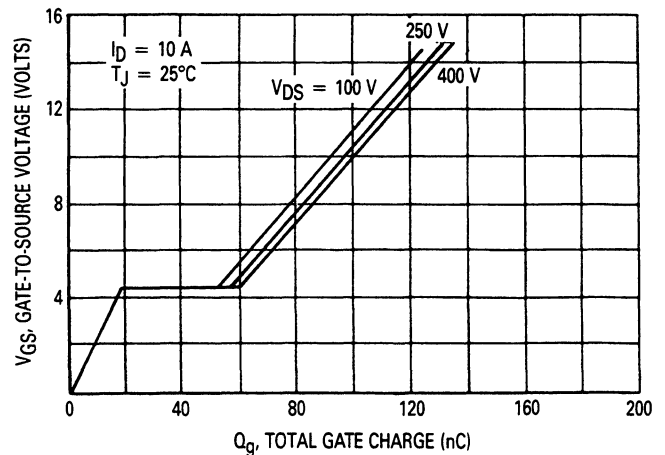


Figure 10. Gate Charge versus Gate-To-Source Voltage



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_{DS} for a given rate of change of source current. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

Device stresses increases with increasing rate of change of source current so di_s/dt is specified with a maximum value. Higher values of di_s/dt require an appropriate derating of I_{FM} , peak V_{DS} or both. Ultimately di_s/dt is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances in Motorola's test circuit are assumed to be practical minimums. dV_{DS}/dt in excess of 10 V/ns was attained with di_s/dt of 400 A/ μ s.

Figure 12. Commutating Safe Operating Area (CSOA)

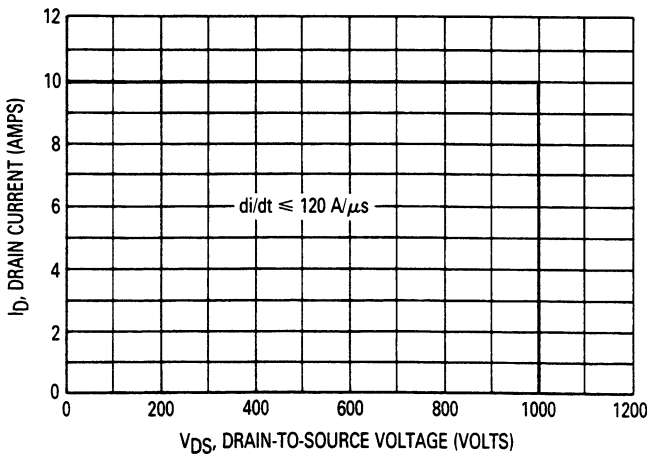


Figure 14. Unclamped Inductive Switching Test Circuit

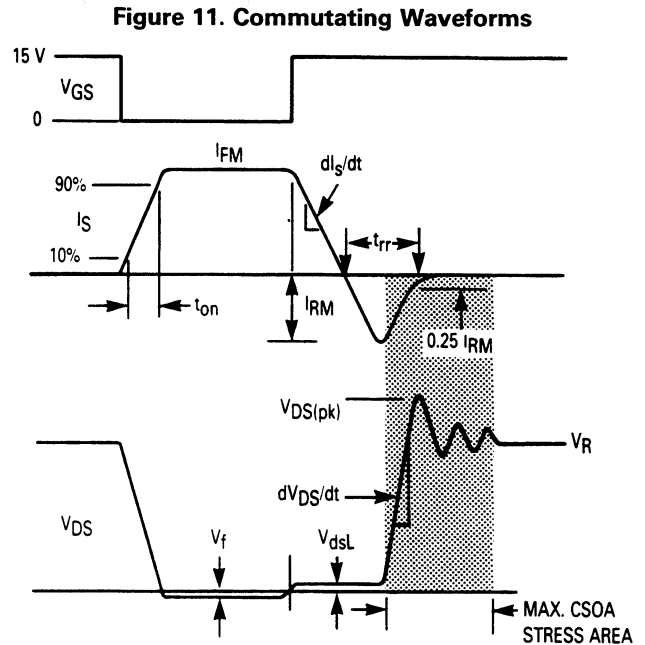
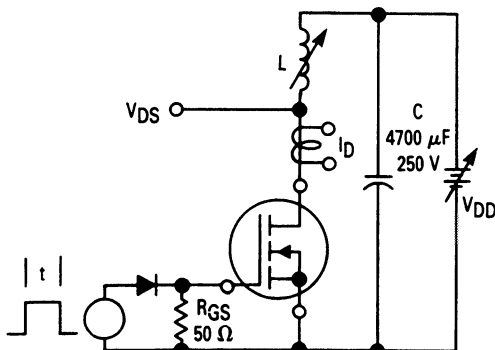


Figure 13. Commutating Safe Operating Area Test Circuit

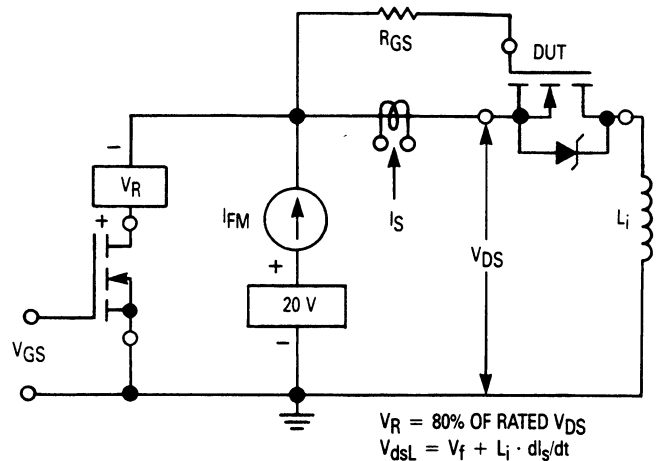
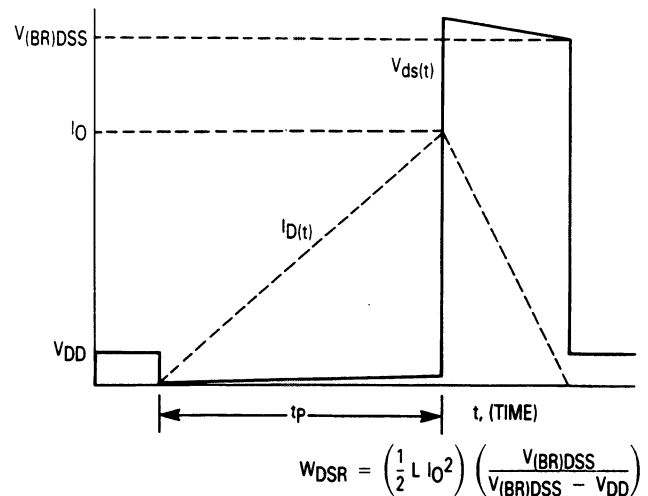
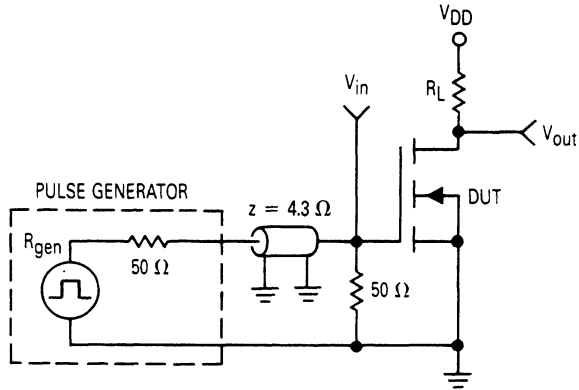


Figure 15. Unclamped Inductive Switching Waveforms



RESISTIVE SWITCHING

Figure 16. Switching Test Circuit



*Note: The Mirror is shorted to the Kelvin terminal for this test.

Figure 17. Switching Waveforms

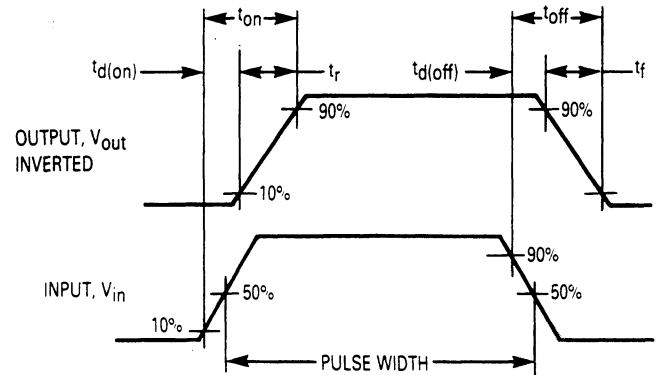
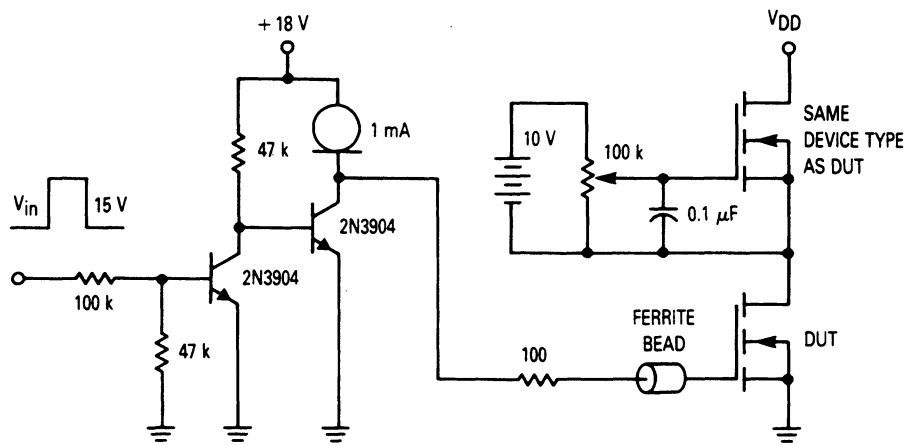


Figure 18. Gate Charge Test Circuit



$V_{in} = 15 V_{pk}$; PULSE WIDTH $\leq 100 \mu s$, DUTY CYCLE $\leq 10\%$

OUTLINE DIMENSIONS

STYLE 3:
PIN 1. GATE
2. SOURCE
CASE. DRAIN


**CASE 197A-02
TO-204AE**

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	38.86 REF		1.530 REF	
B	25.15	26.67	0.990	1.050
C	6.35	8.25	0.250	0.325
D	1.45	1.60	0.057	0.063
E	1.53	1.77	0.060	0.070
G	10.92 BSC		0.430 BSC	
H	5.46 BSC		0.215 BSC	
K	11.18	12.19	0.440	0.480
L	16.89 BSC		0.665 BSC	
N	19.31	21.08	0.760	0.830
Q	3.84	4.19	0.151	0.165
U	30.15 BSC		1.187 BSC	
V	3.33	4.77	0.131	0.188

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