MOTOROLA
SEMICONDUCTOR
TECHNICAL DATA

Order this data sheet
by MTG9N50E/D

Designer's Data Sheet

Full Pak Isolated TMOS E-FET High Energy Power MOSFET

N-Channel Enhancement-Mode Silicon Gate

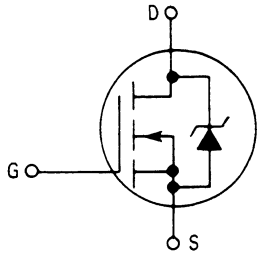
MTG9N50E

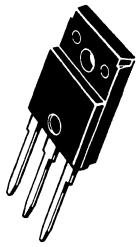
TMOS POWER FET
9.0 AMPERES
$r_{DS(on)}$ = 0.4 OHM MAX
500 VOLTS

This advanced high voltage TMOS E-FET is designed to withstand high energy in the avalanche mode and switch efficiently. This new high energy device also offers a drain-to-source diode with fast recovery time. Designed for high voltage, high speed switching applications such as power supplies, PWM motor controls and other inductive loads, the avalanche energy capability is specified to eliminate the guesswork in designs where inductive loads are switched and offer additional safety margin against unexpected voltage transients. The device is housed in an isolated TO-218 Full Pak which has an isolation voltage rating up to 4500 Volts.

- Avalanche Energy Capability Specified at Elevated Temperature
- Low Stored Gate Charge for Efficient Switching
- Internal Source-to-Drain Diode Designed to Replace External Zener Transient Suppressor — Absorbs High Energy in the Avalanche Mode
- Source-to-Drain Diode Recovery Time Comparable to Discrete Fast Recovery Diode
- Isolated Version of the MTH13N50E

TMOS™





CASE 340B-03

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	500	Volts
Drain-to-Gate Voltage (R_{GS} = 1.0 MΩ)	V_{DGR}	500	Volts
Gate-to-Source Voltage — Continuous — Non-repetitive	V_{GS} V_{GSM}	±20 ±40	Volts
Drain Current — Continuous — Pulsed	I_D I_{DM}	9.0 36	Amps
RMS Isolation Voltage (t = 1 second, R.H. ≤ 30%, T_A = 25°C) Per Figure 19 Per Figure 20	V_{ISO1}	4500 3500	Volts
Total Power Dissipation @ T_C = 25°C Derate above 25°C	P_D	70 0.56	Watts W/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

UNCLAMPED DRAIN-TO-SOURCE AVALANCHE CHARACTERISTICS (T_J < 150°C)

Single Pulse Drain-to-Source Avalanche Energy — T_J = 25°C — T_J = 100°C	$W_{DSS(1)}$	860 110	mJ
Repetitive Pulse Drain-to-Source Avalanche Energy	$W_{DSS(2)}$	7.0	

(1) V_{DD} = 50 V, I_D = 9.0 A
(2) Pulse Width and frequency is limited by T_J(max) and thermal response

Full Pak, TMOS, E-FET and Designer's are trademarks of Motorola Inc.

Designer's Data for "Worst Case" Conditions — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Resistance — Junction to Case — Junction to Ambient	$R_{\theta JC}$ $R_{\theta JA}$	1.79 30	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	T_L	275	°C

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Characteristics	Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS					
Drain-to-Source Breakdown Voltage (V_{GS} = 0, I_D = 0.25 mA)	$V_{(BR)DSS}$	500	—	—	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 500 V, V_{GS} = 0) (V_{DS} = 400 V, V_{GS} = 0, T_J = 125°C)	I_{DSS}	— —	— —	0.25 1.0	mAdc
Gate-Body Leakage Current — Forward (V_{GSF} = 20 Vdc, V_{DS} = 0)	I_{GSSF}	—	—	100	nAdc
Gate-Body Leakage Current — Reverse (V_{GSR} = 20 Vdc, V_{DS} = 0)	I_{GSSR}	—	—	100	nAdc
ON CHARACTERISTICS*					
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 0.25 mAdc) (T_J = 125°C)	$V_{GS(th)}$	2.0 1.5	3.0 —	4.0 3.5	Vdc
Static Drain-to-Source On-Resistance (V_{GS} = 10 Vdc, I_D = 7.0 Adc)	$r_{DS(on)}$	—	—	0.4	Ohm
Drain-to-Source On-Voltage (V_{GS} = 10 Vdc) (I_D = 13 Adc) (I_D = 7.0 Adc, T_J = 125°C)	$V_{DS(on)}$	— —	— —	5.2 5.0	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 7.0 Adc)	g_{FS}	5.0	—	—	mhos
DYNAMIC CHARACTERISTICS					
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	—	2900	—	pF
Output Capacitance		C_{oss}	—	350	—	
Transfer Capacitance		C_{rss}	—	75	—	
SWITCHING CHARACTERISTICS*					
Turn-On Delay Time	(V_{DD} = 250 V, I_D = 13 A, V_{GS} = 10 V, R_{gen} = 6.1 Ohms)	$t_{d(on)}$	—	28	—	ns
Rise Time		t_r	—	80	—	
Turn-Off Delay Time		$t_{d(off)}$	—	80	—	
Fall Time		t_f	—	60	—	
Total Gate Charge	(V_{DS} = 400 V, I_D = 13 A, V_{GS} = 10 V)	Q_g	—	88	130	nC
Gate-Source Charge		Q_{gs}	—	14	—	
Gate-Drain Charge		Q_{gd}	—	45	—	
SOURCE-DRAIN DIODE CHARACTERISTICS					
Forward On-Voltage	(I_S = 13 A, di/dt = 100 A/μs)	V_{SD}	—	1.1	1.6	Vdc
Forward Turn-On Time		t_{on}	—	**	—	ns
Reverse Recovery Time		t_{rr}	—	600	—	
INTERNAL PACKAGE INDUCTANCE					
Internal Drain Inductance (Measured from screw on tab to center of die) (Measured from the drain lead 0.25" from package to center of die)	L_D	— —	4.0 5.0	— —	nH
Internal Source Inductance (Measured from the source lead 0.25" from package to source bond pad)	L_S	—	10	—	
ISOLATION CAPACITANCE					
Drain to Heatsink Capacitance	C_{iso}	—	17	—	pF

*Indicates Pulse Test: Pulse Width = 300 μs, Duty Cycle = 2.0%.
**Limited by circuit inductance.

TYPICAL ELECTRICAL CHARACTERISTICS

Figure 1. On-Region Characteristics

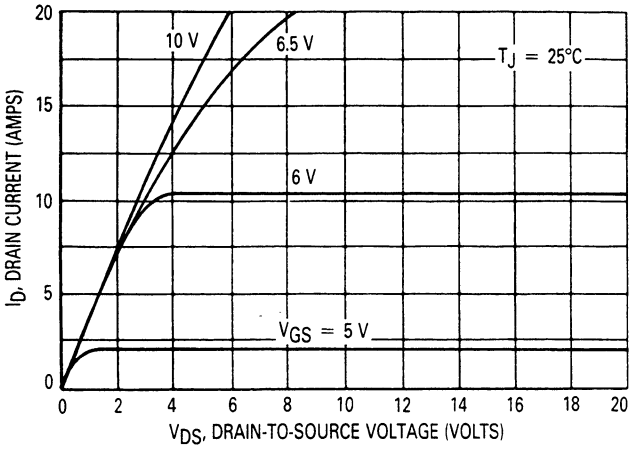


Figure 2. Gate-Threshold Voltage Variation With Temperature

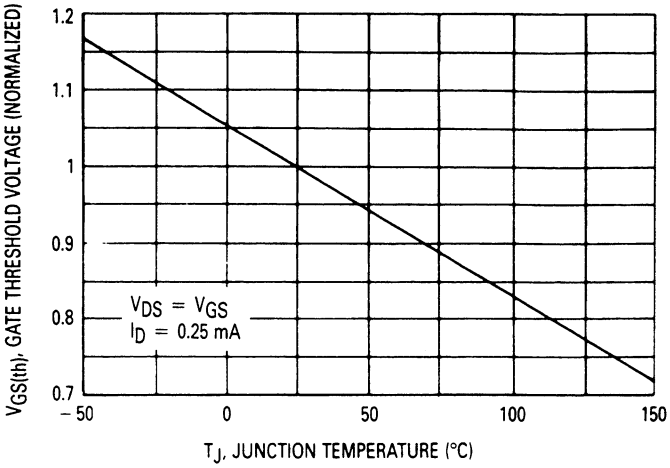


Figure 3. Transfer Characteristics

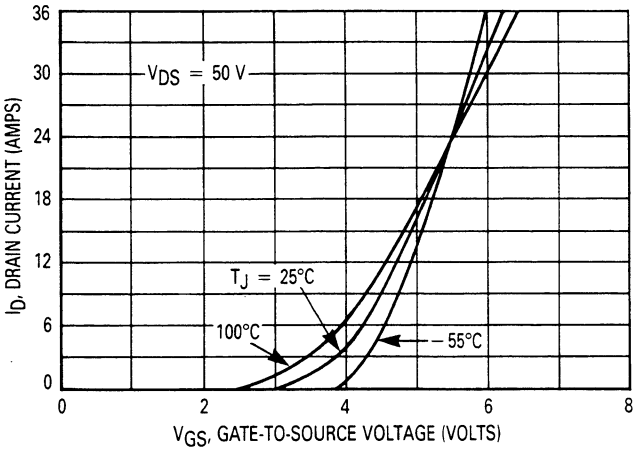


Figure 4. Breakdown Voltage Variation With Temperature

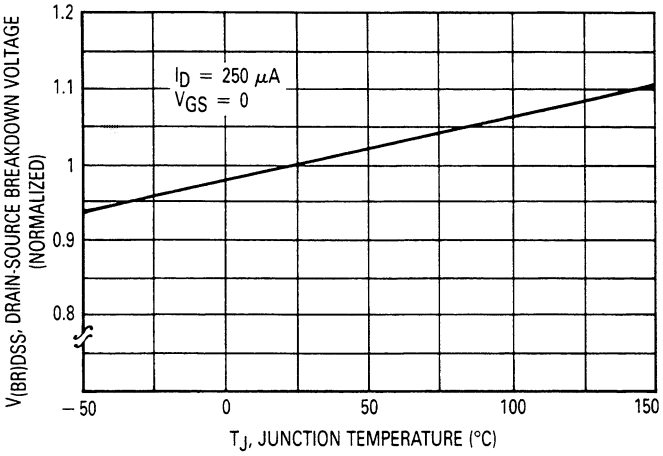


Figure 5. On-Resistance versus Drain Current

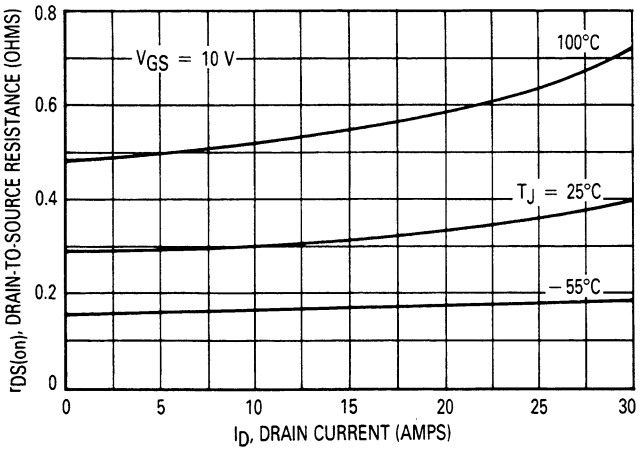
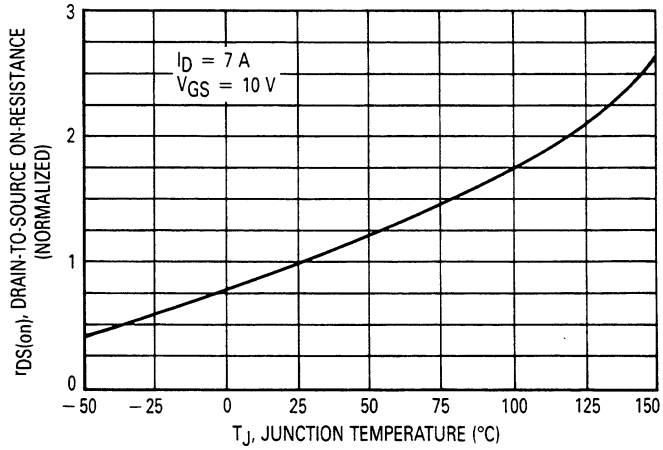


Figure 6. On-Resistance Variation With Temperature



SAFE OPERATING AREA INFORMATION

Figure 7. Maximum Rated Forward Biased Safe Operating Area

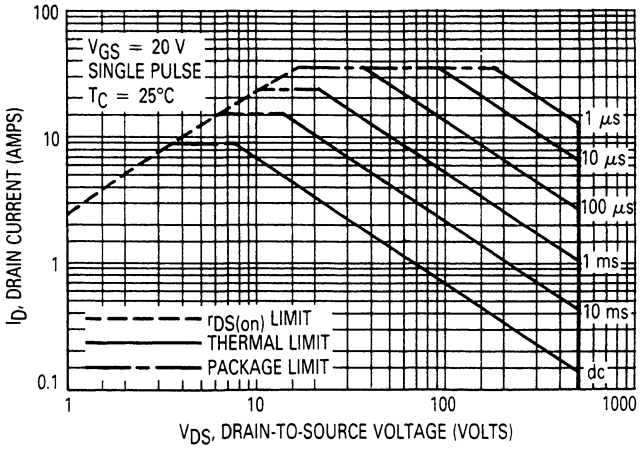
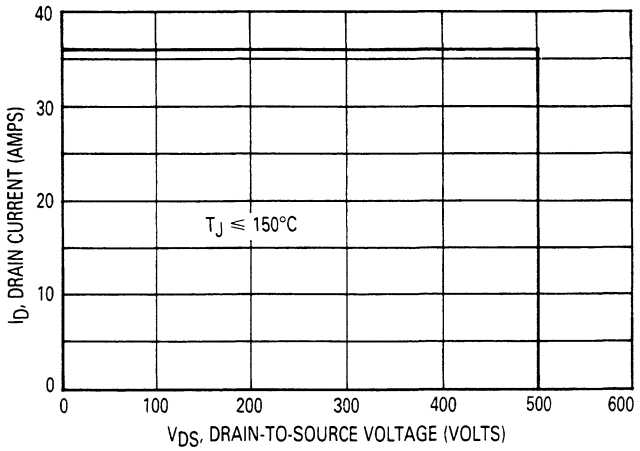


Figure 8. Maximum Rated Switching Safe Operating Area



FORWARD BIASED SAFE OPERATING AREA

The FBSOA curves define the maximum drain-to-source voltage and drain current that a device can safely handle when it is forward biased, or when it is on, or being turned on. Because these curves include the limitations of simultaneous high voltage and high current, up to the rating of the device, they are especially useful to designers of linear systems. The curves are based on a case temperature of 25°C and a maximum junction temperature of 150°C. Limitations for repetitive pulses at various case temperatures can be determined by using the thermal response curves. Motorola Application Note, AN569, "Transient Thermal Resistance-General Data and Its Use" provides detailed instructions.

SWITCHING SAFE OPERATING AREA

The switching safe operating area (SOA) of Figure 8 is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, I_{DM} and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 8 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

Figure 9. Resistive Switching Time Variation versus Gate Resistance

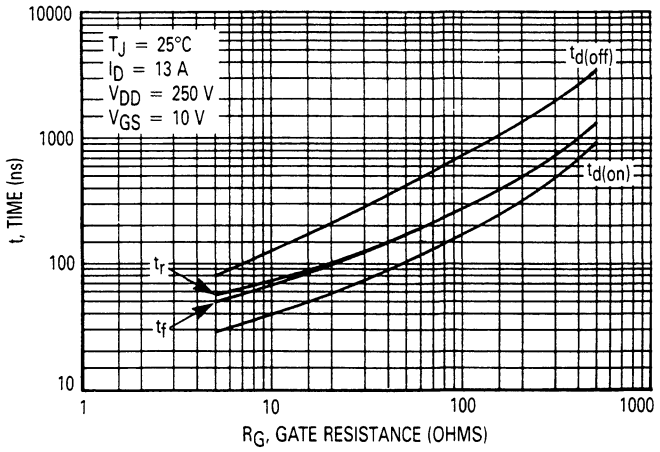
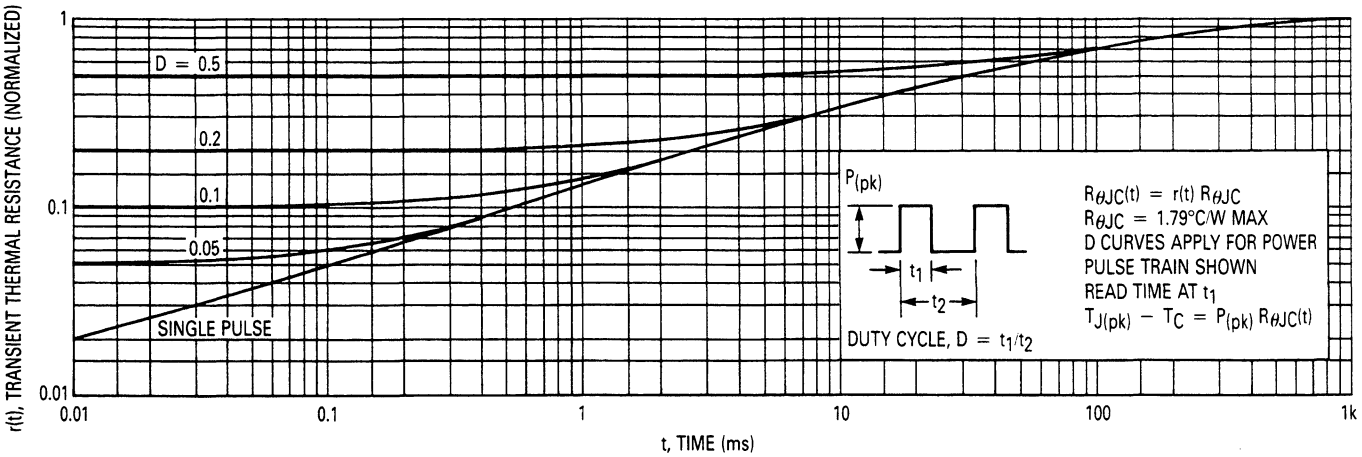


Figure 10. Thermal Response



COMMUTATING SAFE OPERATING AREA (CSOA)

The Commutating Safe Operating Area (CSOA) of Figure 12 defines the limits of safe operation for commutated source-drain current versus re-applied drain voltage when the source-drain diode has undergone forward bias. The curve shows the limitations of I_{FM} and peak V_R for a given commutation speed. It is applicable when waveforms similar to those of Figure 11 are present. Full or half-bridge PWM DC motor controllers are common applications requiring CSOA data.

The time interval t_{frr} is the speed of the commutation cycle. Device stresses increase with commutation speed, so t_{frr} is specified with a minimum value. Faster commutation speeds require an appropriate derating of I_{FM}, peak V_R or both. Ultimately, t_{frr} is limited primarily by device, package, and circuit impedances. Maximum device stress occurs during t_{rr} as the diode goes from conduction to reverse blocking.

$V_{DS(pk)}$ is the peak drain-to-source voltage that the device must sustain during commutation; I_{FM} is the maximum forward source-drain diode current just prior to the onset of commutation.

V_R is specified at 80% of $V_{(BR)DSS}$ to ensure that the CSOA stress is maximized as I_S decays from I_{RM} to zero.

R_{GS} should be minimized during commutation. T_J has only a second order effect on CSOA.

Stray inductances, L_i in Motorola's test circuit are assumed to be practical minimums.

Figure 11. Commutating Waveforms

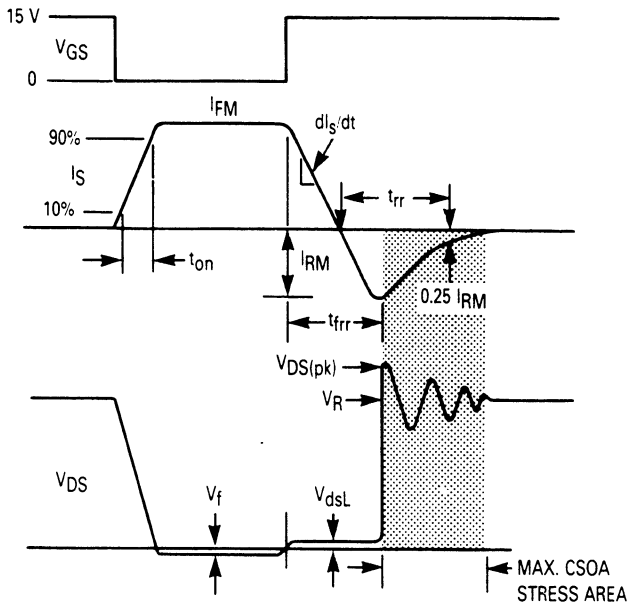


Figure 12. Commutating Safe Operating Area (CSOA)

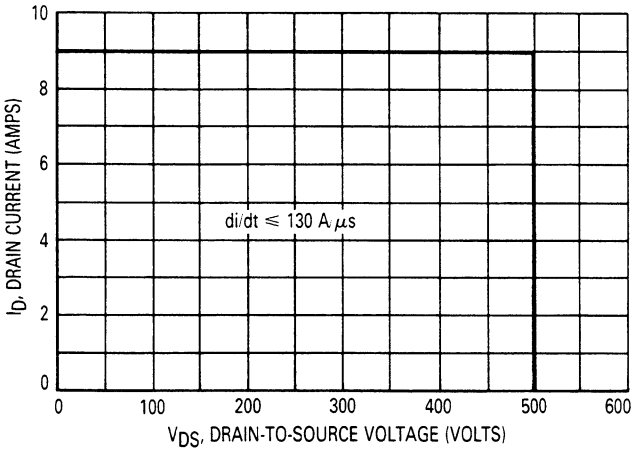


Figure 13. Commutating Safe Operating Area Test Circuit

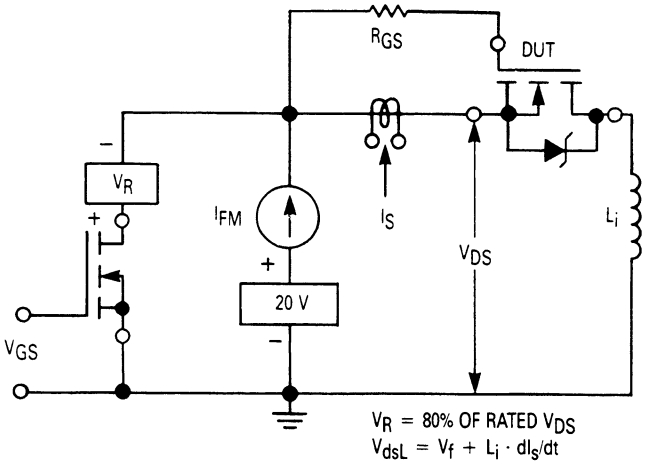


Figure 14. Unclamped Inductive Switching Test Circuit

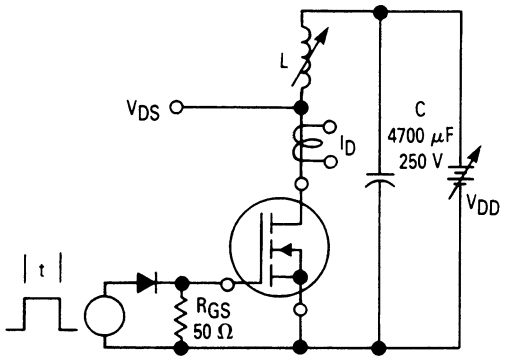
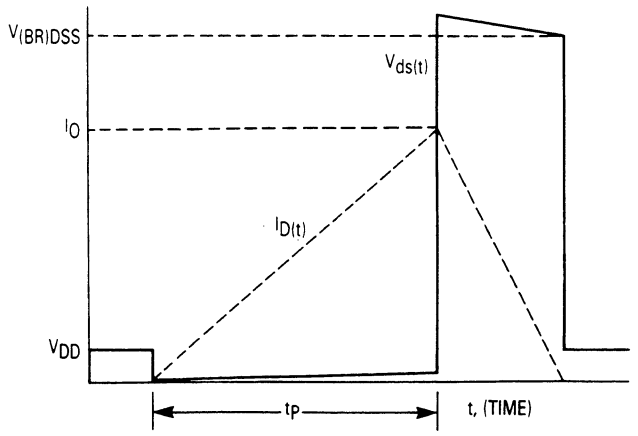


Figure 15. Unclamped Inductive Switching Waveforms



$$W_{DSR} = \left(\frac{1}{2} L I_O^2\right)\left(\frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}\right)$$

Figure 16. Capacitance Variation

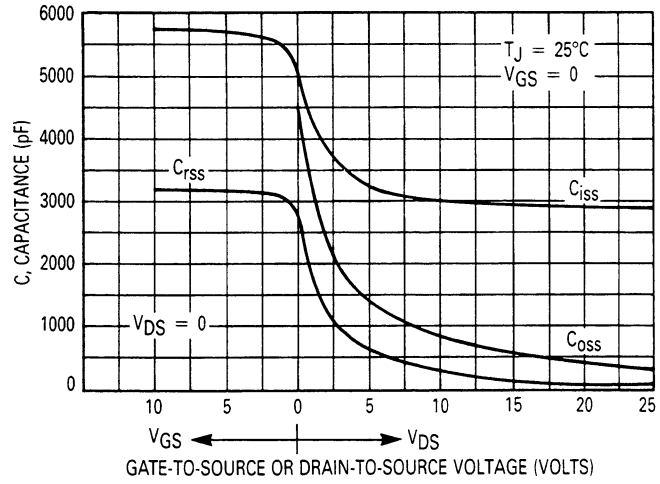


Figure 17. Gate Charge versus Gate-to-Source Voltage

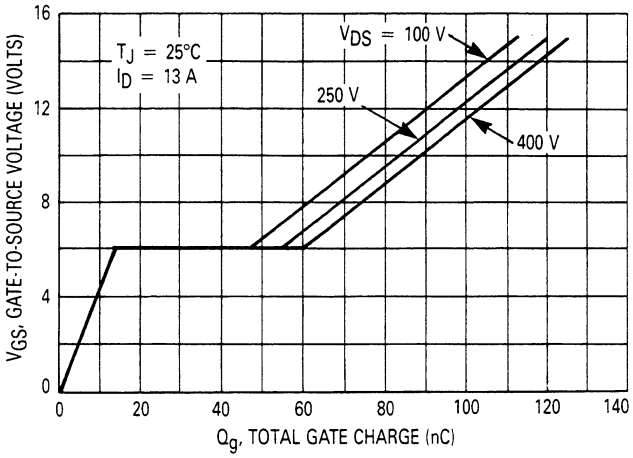
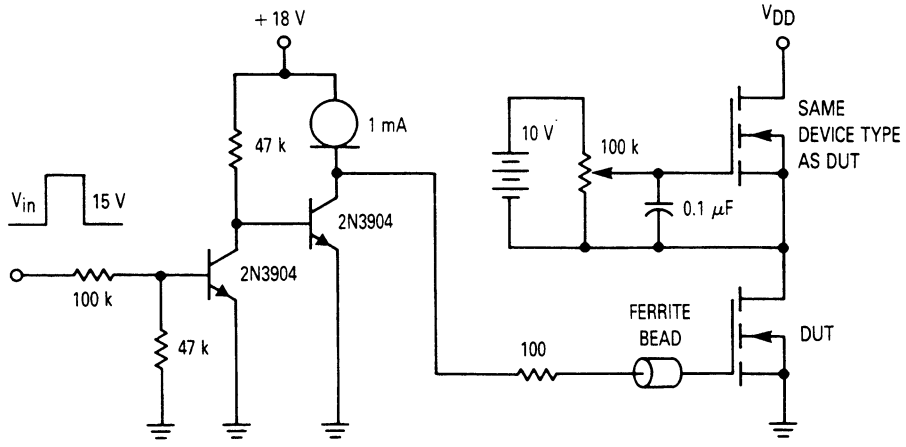


Figure 18. Gate Charge Test Circuit



V_{in} = 15 V_{pk}; PULSE WIDTH ≤ 100 μs, DUTY CYCLE ≤ 10%

TEST CONDITIONS FOR ISOLATION TESTS*

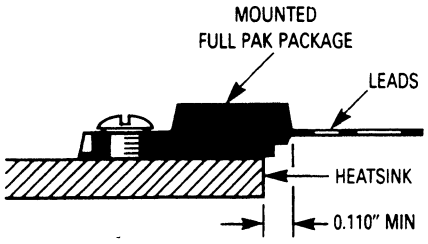


Figure 19. Screw or Clip Mounting Position for Isolation Test Number 1

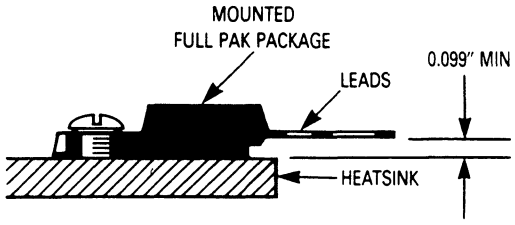
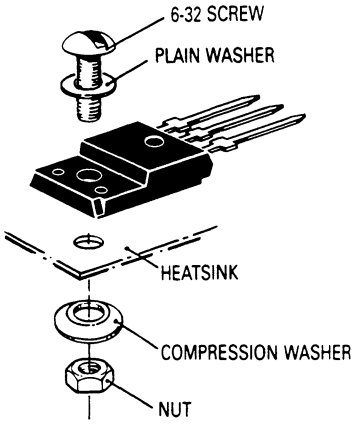


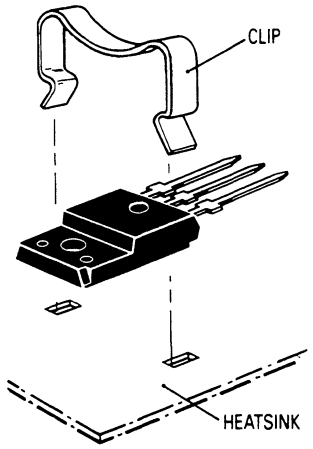
Figure 20. Screw or Clip Mounting Position for Isolation Test Number 2

*Measurement made between leads and heatsink with all leads shorted together.

MOUNTING INFORMATION**



21a. Screw-Mounted Full Pak



21b. Clip-Mounted Full Pak

Figure 21. Typical Mounting Techniques*

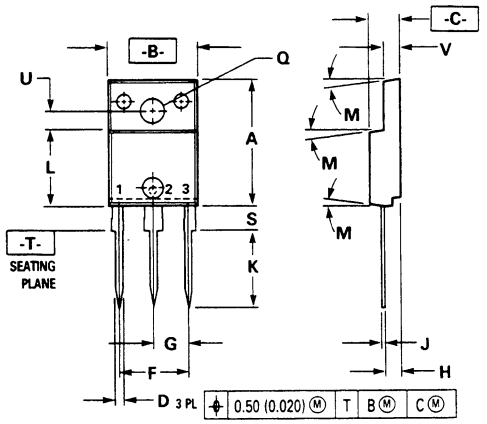
Laboratory tests on a limited number of samples indicate, when using the screw and compression washer mounting technique, a screw torque of 6 to 8 in • lbs is sufficient to provide maximum power dissipation capability. The compression washer helps to maintain a constant pressure on the package over time and during large temperature excursions.

Destructive laboratory tests show that using a hex head 4-40 screw, without washers, and applying a torque in excess of 20 in • lbs will cause the plastic to crack around the mounting hole, resulting in a loss of isolation capability.

Additional tests on slotted 4-40 screws indicate that the screw slot fails between 15 to 20 in • lbs without adversely affecting the package. However, in order to positively insure the package integrity of the Full Pak, Motorola does not recommend exceeding 10 in • lbs of mounting torque under any mounting conditions.

**For more information about mounting power semiconductors see Application Note AN1040.

OUTLINE DIMENSIONS



STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	19.97	20.21	0.786	0.796
B	13.97	14.47	0.550	0.570
C	4.81	5.05	0.189	0.199
D	1.10	1.24	0.043	0.049
F	10.98 BSC		0.432 BSC	
G	5.44 BSC		0.214 BSC	
H	2.52	2.71	0.099	0.107
J	0.51	0.71	0.020	0.028
K	11.94	12.31	0.470	0.485
L	11.82	12.06	0.465	0.475
M	7° NOM		7° NOM	
Q	3.41	3.60	0.134	0.142
S	3.56	4.06	0.140	0.160
U	2.95	3.05	0.116	0.120
V	2.52	2.76	0.099	0.109

CASE 340B-03

Literature Distribution Centers:
USA: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036.
EUROPE: Motorola Ltd.; European Literature Centre; 88 Tanners Drive, Blakelands, Milton Keynes, MK14 5BP, England.
JAPAN: Nippon Motorola Ltd.; 4-32-1, Nishi-Gotanda, Shinagawa-ku, Tokyo 141, Japan.
ASIA PACIFIC: Motorola Semiconductors H.K. Ltd.; Silicon Harbour Center, No. 2 Dai King Street, Tai Po Industrial Estate, Tai Po, N.T., Hong Kong.

MOTOROLA

24189 PRINTED IN USA (1994) MPS/POD YAAGAA

MTG9N50E/D