MOTOROLA

# SEMICONDUCTORS

P.O. BOX 20912 • PHOENIX, ARIZONA 85036

# MTH13N45
# MTH13N50
# MTH15N35
# MTH15N40

## Designer's Data Sheet

**13 and 15 AMPERES**

**N-CHANNEL TMOS POWER FETs**

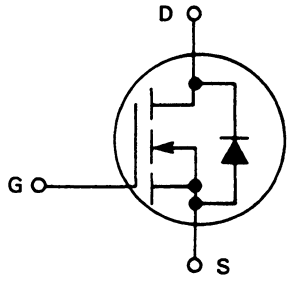
**$r_{DS(on)}$ = 0.4 OHM**
**450 and 500 VOLTS**
**$r_{DS(on)}$ = 0.3 OHM**
**350 and 400 VOLTS**

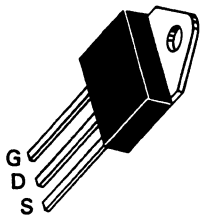
### N-CHANNEL ENHANCEMENT MODE SILICON GATE TMOS POWER FIELD EFFECT TRANSISTOR

These TMOS Power FETs are designed for medium voltage, high speed power switching applications such as switching regulators, converters, solenoid and relay drivers.

- Silicon Gate for Fast Switching Speeds — Switching Times Specified at 100°C
- Designer's Data — $I_{DSS}$, $V_{DS(on)}$, $V_{GS(th)}$ and SOA Specified at Elevated Temperature
- Rugged — SOA is Power Dissipation Limited
- Source-to-Drain Diode Characterized for Use With Inductive Loads

TMOS™




### MAXIMUM RATINGS

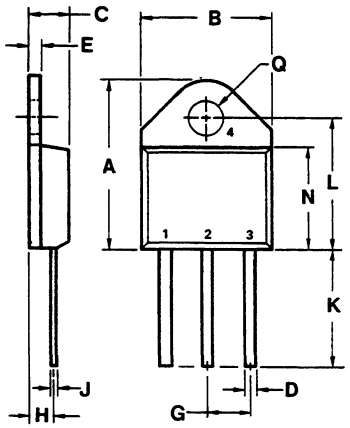
| Rating | Symbol | MTH 13N45 | MTH 13N50 | MTH 15N35 | MTH 15N40 | Unit |
|---|---|---|---|---|---|---|
| Drain-Source Voltage | $V_{DSS}$ | 450 | 500 | 350 | 400 | Vdc |
| Drain-Gate Voltage ($R_{GS}$ = 1.0 mΩ) | $V_{DGR}$ | 450 | 500 | 350 | 400 | Vdc |
| Gate-Source Voltage | $V_{GS}$ | ±20 | | | | Vdc |
| Drain Current<br>Continuous<br>Pulsed | <br>$I_D$<br>$I_{DM}$ | <br>13<br>60 | | <br>15<br>75 | | Adc |
| Gate Current — Pulsed | $I_{GM}$ | 1.5 | | | | Adc |
| Total Power Dissipation @ $T_C$ = 25°C<br>Derate above 25°C | $P_D$ | 150<br>1.2 | | | | Watts<br>W/°C |
| Operating and Storage Temperature Range | $T_J$,$T_{stg}$ | −65 to 150 | | | | °C |

### THERMAL CHARACTERISTICS

| | | | |
|---|---|---|---|
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | 0.83 | °C/W |
| Maximum Lead Temp. for Soldering Purposes, 1/8" from case for 5 seconds | $T_L$ | 275 | °C |

**Designer's Data for "Worst Case" Conditions**

The Designer's Data Sheet permits the design of most circuits entirely from the information presented. Limit data — representing device characteristics boundaries — are given to facilitate "worst case" design.




STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

| DIM | MILLIMETERS MIN | MILLIMETERS MAX | INCHES MIN | INCHES MAX |
|---|---|---|---|---|
| A | 20.32 | 21.08 | 0.800 | 0.830 |
| B | 15.49 | 15.90 | 0.610 | 0.626 |
| C | 4.19 | 5.08 | 0.165 | 0.200 |
| D | 1.02 | 1.65 | 0.040 | 0.065 |
| E | 1.35 | 1.65 | 0.053 | 0.065 |
| G | 5.21 | 5.72 | 0.205 | 0.225 |
| H | 2.41 | 3.20 | 0.095 | 0.126 |
| J | 0.38 | 0.64 | 0.015 | 0.025 |
| K | 12.70 | 15.49 | 0.500 | 0.610 |
| L | 15.88 | 16.51 | 0.625 | 0.650 |
| N | 12.19 | 12.70 | 0.480 | 0.500 |
| Q | 4.04 | 4.22 | 0.159 | 0.166 |

**CASE 340-01**

**ELECTRICAL CHARACTERISTICS** ($T_C$ = 25°C unless otherwise noted)

| Characteristic | | Symbol | Min | Max | Unit |
|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | |
| Drain-Source Breakdown Voltage ($V_{GS}$ = 0, $I_D$ = 0.25 mA) | MTH15N35 | $V_{(BR)DSS}$ | 350 | — | Vdc |
| | MTH15N40 | | 400 | — | |
| | MTH13N45 | | 450 | — | |
| | MTH13N50 | | 500 | — | |
| Zero Gate Voltage Drain Current ($V_{DS}$ = Rated $V_{DSS}$, $V_{GS}$ = 0) | | $I_{DSS}$ | — | 0.25 | mAdc |
| ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $V_{GS}$ = 0, $T_J$ = 125°C) | | | — | 1.00 | |
| Gate-Body Leakage Current, Forward ($V_{GSF}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSF}$ | — | 500 | nAdc |
| Gate-Body Leakage Current, Reverse ($V_{GSR}$ = 20 Vdc, $V_{DS}$ = 0) | | $I_{GSSR}$ | — | 500 | nAdc |
| **ON CHARACTERISTICS*** | | | | | |
| Gate Threshold Voltage ($V_{DS}$ = $V_{GS}$, $I_D$ = 1.0 mA) | | $V_{GS(th)}$ | 2.0 | 4.5 | Vdc |
| $T_J$ = 100°C | | | 1.5 | 4.0 | |
| Static Drain-Source On-Resistance ($V_{GS}$ = 10 Vdc, $I_D$ = 8.0 Adc) | MTH15N35/40 | $r_{DS(on)}$ | — | 0.3 | Ohm |
| ($V_{GS}$ = 10 Vdc, $I_D$ = 7.0 Adc) | MTH13N45/50 | | — | 0.4 | |
| Drain-Source On-Voltage ($V_{GS}$ = 10 V) | | $V_{DS(on)}$ | | | Vdc |
| ($I_D$ = 15 Adc) | MTH15N35/40 | | — | 4.5 | |
| ($I_D$ = 8.0 Adc, $T_J$ = 100°C) | MTH15N35/40 | | — | 3.5 | |
| ($I_D$ = 13 Adc) | MTH13N45/50 | | — | 5.2 | |
| ($I_D$ = 7.0 Adc, $T_C$ = 100°C) | MTH13N45/50 | | — | 5.0 | |
| Forward Transconductance ($V_{DS}$ = 10 V, $I_D$ = 8.0 A) | MTH15N35/40 | $g_{fs}$ | 4.0 | — | mhos |
| ($V_{DS}$ = 10 V, $I_D$ = 7.0 A) | MTH13N45/50 | | 5.0 | — | |
| **DYNAMIC CHARACTERISTICS** | | | | | |
| Input Capacitance | ($V_{DS}$ = 25 V, $V_{GS}$ = 0, f = 1.0 MHz) | $C_{iss}$ | — | 3000 | pF |
| Output Capacitance | | $C_{oss}$ | — | 500 | |
| Reverse Transfer Capacitance | | $C_{rss}$ | — | 200 | |
| **SWITCHING CHARACTERISTICS*** ($T_J$ = 100°C) | | | | | |
| Turn-On Delay Time | ($V_{DD}$ = 25 V, $I_D$ = 0.5 Rated $I_D$, $R_{gen}$ = 50 ohms) See Figures 10 and 11. | $t_{d(on)}$ | — | 60 | ns |
| Rise Time | | $t_r$ | — | 180 | |
| Turn-Off Delay Time | | $t_{d(off)}$ | — | 450 | |
| Fall Time | | $t_f$ | — | 180 | |
| Total Gate Charge | ($V_{DS}$ = 0.8 Rated $V_{DSS}$, $I_D$ = Rated $I_D$, $V_{GS}$ = 10 V) See Figures 15, 16 and 17. | $Q_g$ | 110 (typ) | 160 | nC |
| Gate-Source Charge | | $Q_{gs}$ | 50 (typ) | — | |
| Gate-Drain Charge | | $Q_{gd}$ | 60 (typ) | — | |
| **SOURCE DRAIN DIODE CHARACTERISTICS*** | | | | | |
| Forward On-Voltage | ($I_S$ = Rated $I_D$, $V_{GS}$ = 0) See Figures 18 and 19. | $V_{SD}$ | — | 1.4[1] | Vdc |
| Forward Turn-On Time | | $t_{on}$ | 210 (typ) | — | ns |
| Reverse Recovery Time | | $t_{rr}$ | 1200 (typ) | — | ns |

*Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

(1)Add 0.2 V for MTH15N35 and MTH15N40.

## TYPICAL CHARACTERISTICS

### ON-REGION CHARACTERISTICS

FIGURE 1 — MTH13N45/50

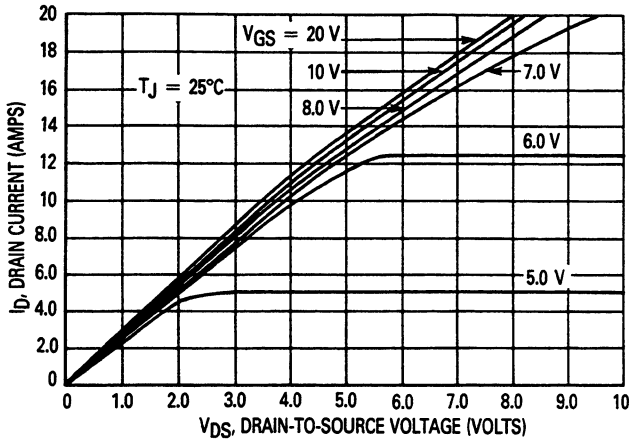
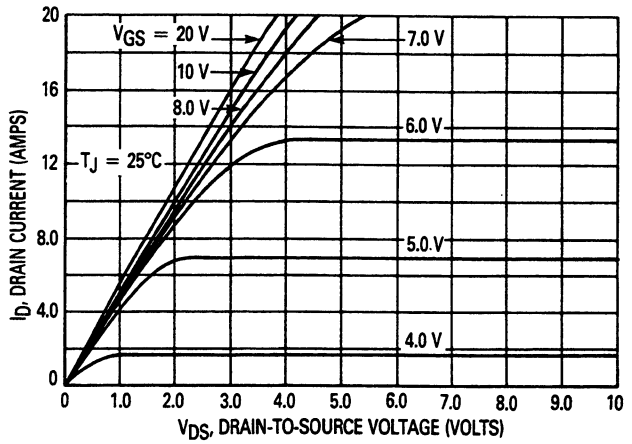



FIGURE 2 — MTH15N35/40




### TRANSFER CHARACTERISTICS

FIGURE 3 — MTH13N45/50

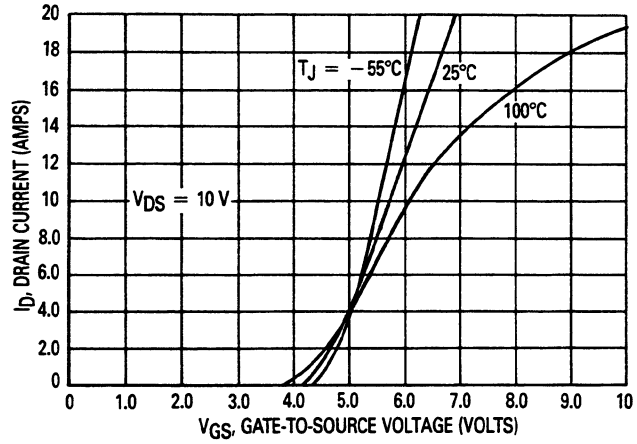
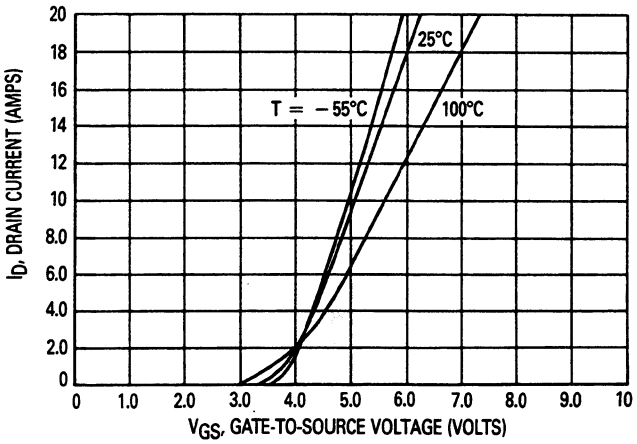



FIGURE 4 — MTH15N35/40




### ON-RESISTANCE versus DRAIN CURRENT

FIGURE 5 — MTH13N45/50

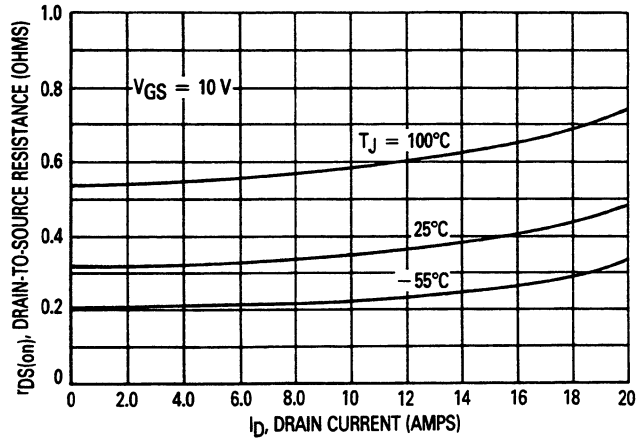
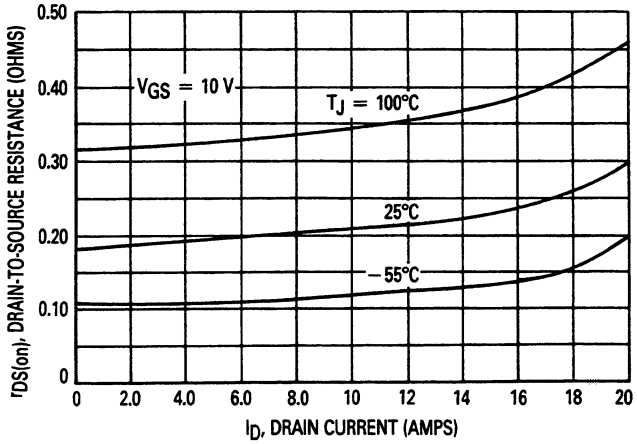



FIGURE 6 — MTH15N35/40



## TYPICAL CHARACTERISTICS (continued)

FIGURE 7 — GATE-THRESHOLD VOLTAGE VARIATION WITH TEMPERATURE

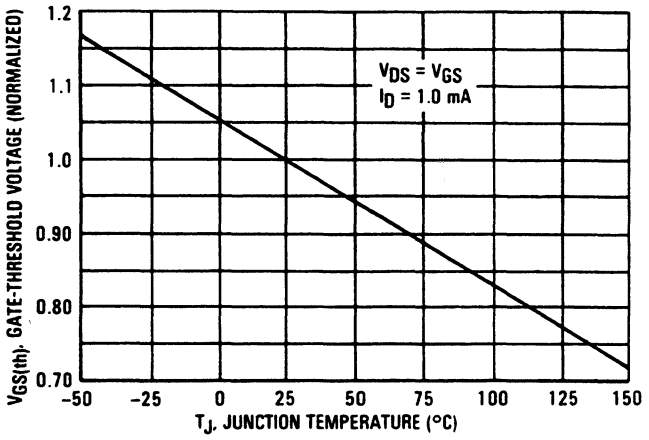
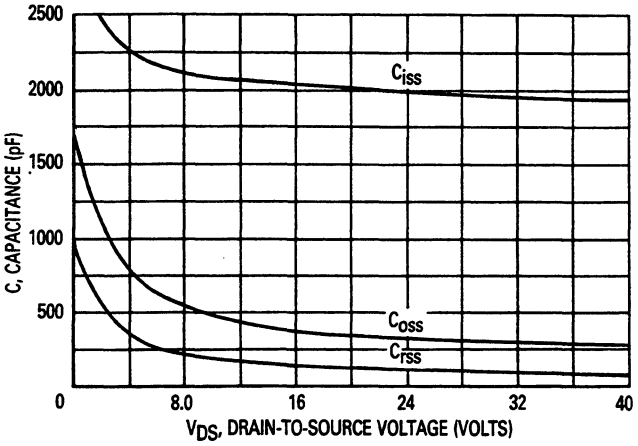
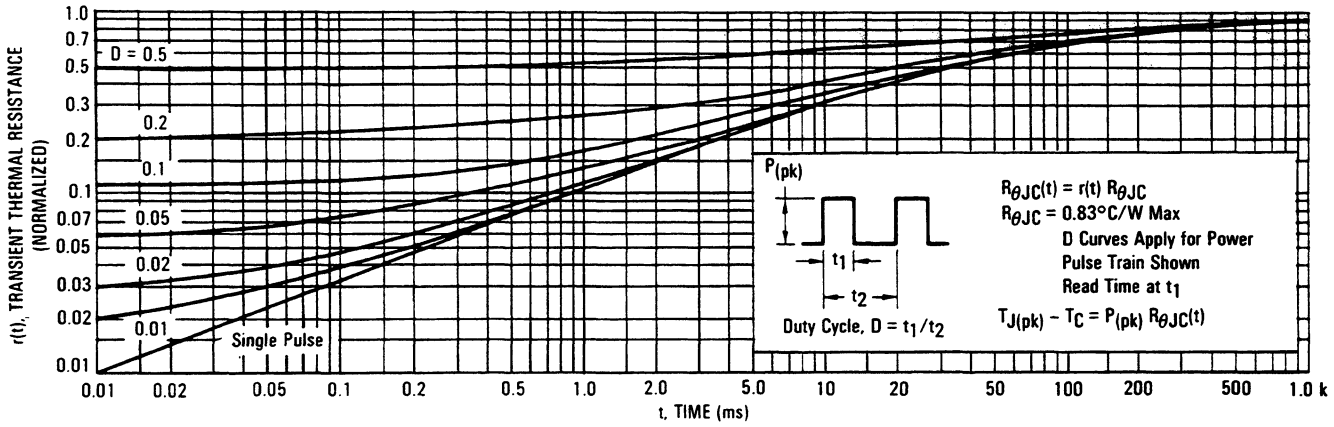



FIGURE 8 — MTH13N45/50 CAPACITANCE VARIATION




## THERMAL RESPONSE

FIGURE 9 — MTM3N45, MTM3N50, MTM4N35, MTM4N40




## RESISTIVE SWITCHING

FIGURE 10 — SWITCHING TEST CIRCUIT

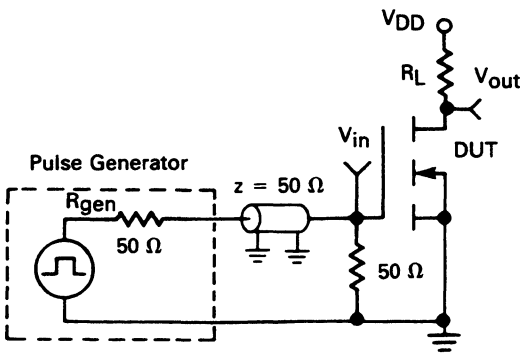
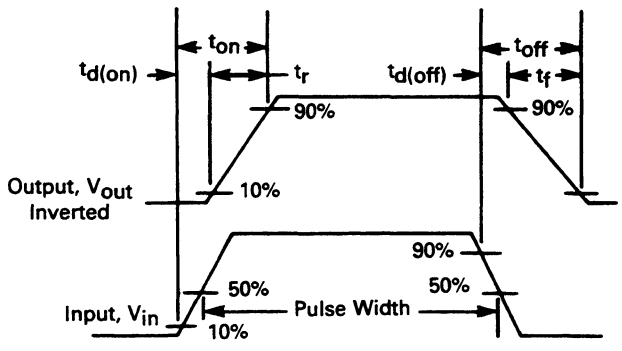



FIGURE 11 — SWITCHING WAVEFORMS



## SAFE OPERATING AREA INFORMATION

### MAXIMUM RATED FORWARD BIASED SAFE OPERATING AREA

FIGURE 12 — MTH13N45, MTH13N50

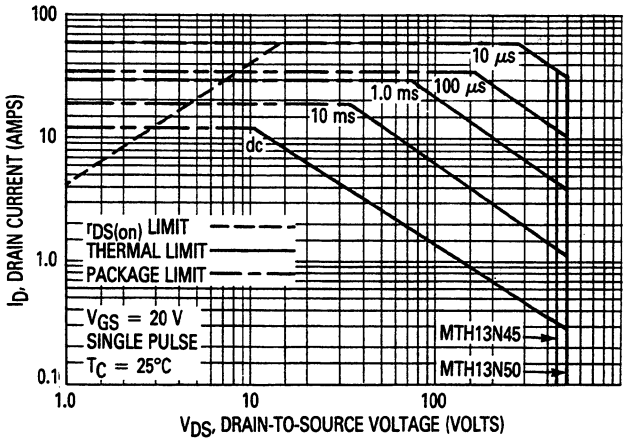
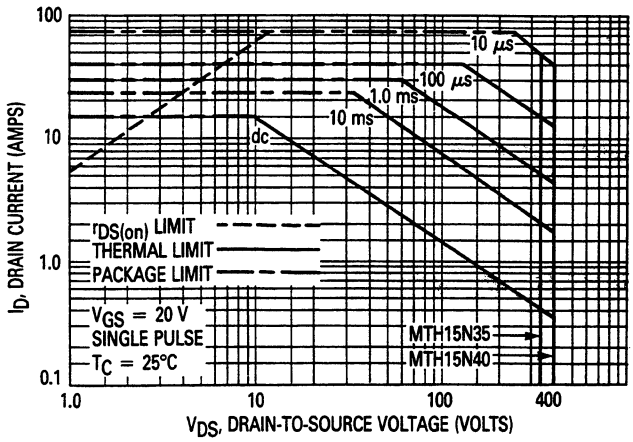



FIGURE 13 — MTH15N35, MTH15N40




**FORWARD BIASED SAFE OPERATING AREA**

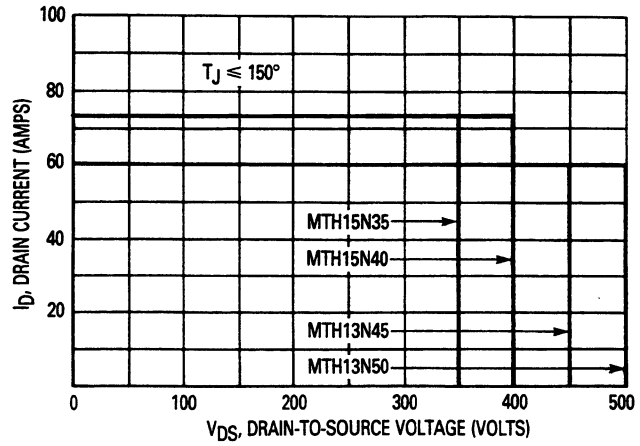
The dc data of Figures 12 and 13 is based on a case temperature ($T_C$) of 25°C and a maximum junction temperature ($T_{J(max)}$) of 150°. The actual junction temperature depends on the power dissipated in the device and its case temperature. For various pulse widths, duty cycles, and case temperatures, the peak allowable drain current ($I_{DM}$) may be calculated with the aid of the following equation:

$$I_{DM} = I_{D(25°C)}\left[\frac{T_{J(max)} - T_C}{P_D \cdot R_{\theta JC} \cdot r(t)}\right]$$

where

$I_{D(25°C)}$ = the dc drain current at $T_C$ = 25°C from Figures 12 and 13.
$T_{J(max)}$ = rated maximum junction temperature.
$T_C$ = device case temperature.
$P_D$ = rated power dissipation at $T_C$ = 25°C.
$R_{\theta JC}$ = rated steady state thermal resistance.
r(t) = normalized thermal response from Figure 9.

FIGURE 14 — MAXIMUM RATED SWITCHING SAFE OPERATING AREA




**SWITCHING SAFE OPERATING AREA**

The switching safe operating area (SOA) of Figure 14, is the boundary that the load line may traverse without incurring damage to the MOSFET. The fundamental limits are the peak current, $I_{DM}$ and the breakdown voltage, $V_{(BR)DSS}$. The switching SOA shown in Figure 14 is applicable for both turn-on and turn-off of the devices for switching times less than one microsecond.

The power averaged over a complete switching cycle must be less than:

$$\frac{T_{J(max)} - T_C}{R_{\theta JC}}$$

**FIGURE 15 — MTH13N45/50**
**GATE CHARGE versus GATE-TO-SOURCE VOLTAGE**

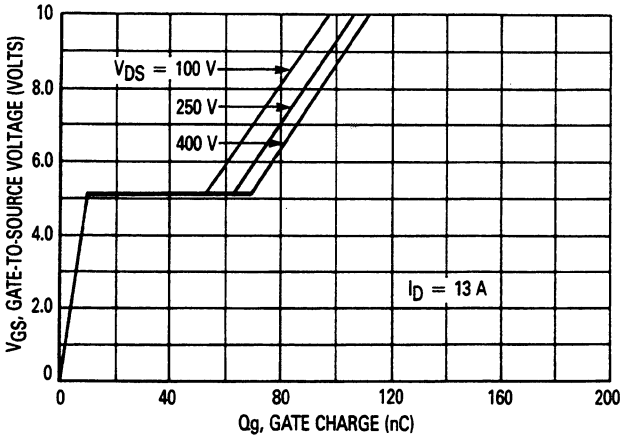



**FIGURE 16 — MTH15N35/40**
**TYPICAL GATE CHARGE versus GATE-TO-SOURCE VOLTAGE**

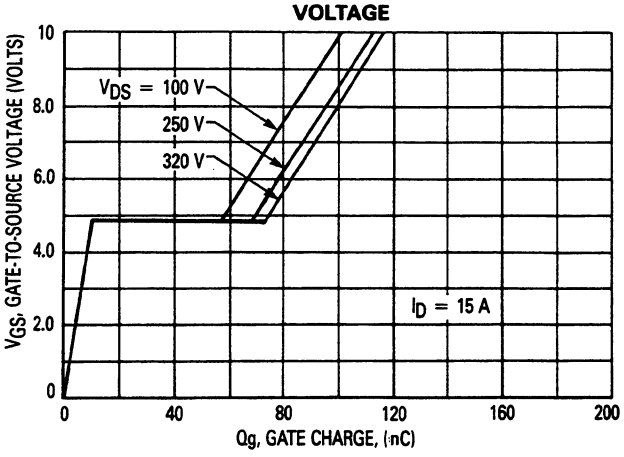
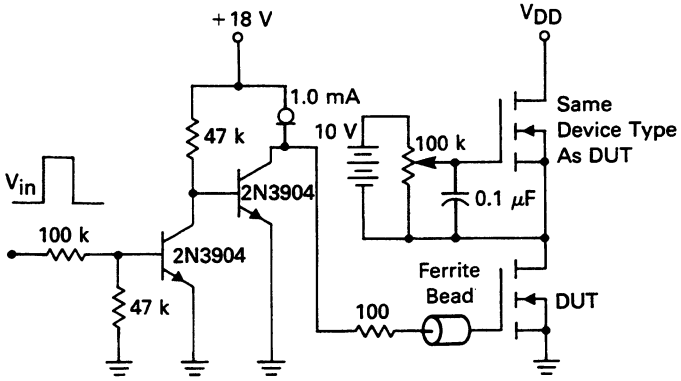



**FIGURE 17 — GATE CHARGE TEST CIRCUIT**




$V_{in}$ = 15 $V_{pk}$; Pulse Width ≤ 100 μs, Duty Cycle ≤ 10%

**FIGURE 18 — DIODE SWITCHING WAVEFORM**

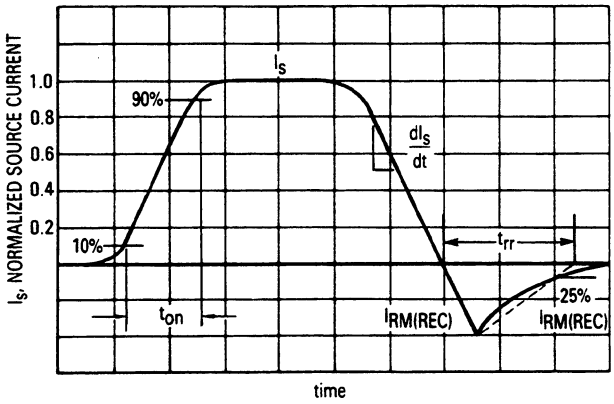
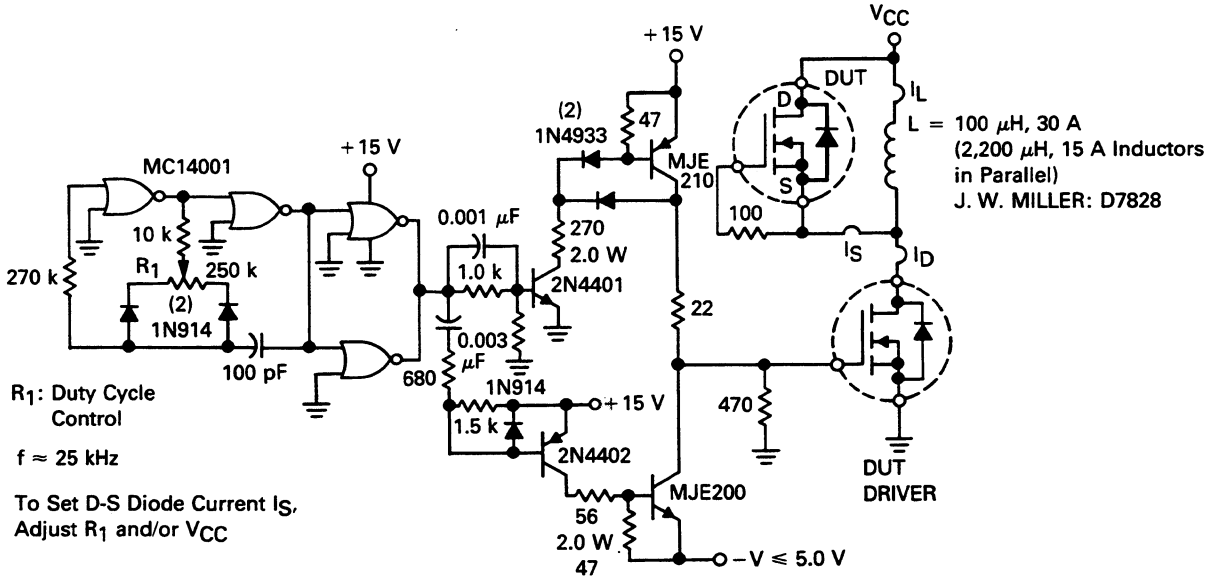



**FIGURE 19 — TMOS DIODE SWITCHING TEST CIRCUIT**




NOTE: DUT is Shown as an N-Channel TMOS but can also be a P-Channel when appropriately connected. DUT Driver is the same device as DUT Diode (or Complement for P-Channel DUT Diode)

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