Microsemi

SANTA ANA DIVISION

MSAFA75N10C

N-CHANNEL ENHANCEMENT MODE POWER MOSFET

PRODUCT PREVIEW

DESCRIPTION

New generation N-channel enhancement mode power MOSFET with rugged polysilicon gate structure and fast switching intrinsic rectifier. The very rugged Coolpack2™ surface-mount package is lightweight, space saving and hermetically sealed for high reliability and/or military/space application.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- Ultrafast body diode
- Increased Unclamped Inductive Switching (UIS) capability
- Hermetically sealed, surface mount power package
- Very low package inductance
- Very low thermal resistance
- Reverse polarity available upon request

APPLICATIONS/BENEFITS

- DC-DC converters
- Motor controls
- Uninterruptible Power Supply(UPS)
- DC choppers
- Synchronous rectification
- Inverters

MAXIMUM RATINGS @ 25°C (unless otherwise specified)

Description		Symbol	Max.	Unit
Drain-to-Source Voltage (Gate Shorted to Source)		V_{DSS}	100	Volts
Continuous Gate-to-Source Voltage		V_{GS}	+/-30	Volts
Transient Gate-to-Source Voltage		V_{GSM}	+/-40	Volts
Continuous Drain Current	T_j= 25°C T_j= 100°C	I_{D25} I_{D100}	75 60	Amps
Peak Drain Current, pulse width limited by T_{Jmax}		I_{DM}	300	Amps
Repetitive Avalanche Current		I_{AR}	75	Amps
Repetitive Avalanche Energy		E_{AR}	30	mJ
Single Pulse Avalanche Energy (3)		E_{AS}	1500	mJ
Total Power Dissipation @T_c=25°C		P_D	540	Watts
Junction Temperature Range		T_j	-55 to +150	°C
Storage Temperature Range		T_{stg}	-55 to +150	°C
Continuous Source Current (Body Diode)		I_S	75	Amps
Pulse Source Current (Body Diode)		I_{SM}	300	Amps
Thermal Resistance, Junction to Case		θ_{JC}	0.23	°C/W

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ELECTRICAL PARAMETERS @ 25°C (unless otherwise specified)

Description	Symbol	Conditions	Min	Typ.	Max	Unit
Drain-to-Source Breakdown Voltage (Gate Shorted to Source)	BV_{DSS}	V_{GS} = 0 V, I_D = 250 µA	100			V
Gate-to-Source Leakage Current	I_{GSS}	V_{GS} = ± 30 V_{DC}, V_{DS} = 0			±100	nA
Drain-to-Source Leakage Current (Zero Gate Voltage Drain Current)	I_{DSS}	V_{DS} =0.8•BV_{DSS} T_J = 25°C V_{GS} = 0 V T_J = 125°C			250 1000	µA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1 mA	2.0		4.0	V
Static Drain-to-Source On-State Resistance (1)	$R_{DS(on)}$	V_{GS}= 10V, I_D= 37.5A T_J = 25°C I_D= 75A T_J = 25°C I_D= 37.5A T_J = 125°C		 0.02 0.035	0.019	Ω
Input Capacitance Output Capacitance Reverse Transfer Capacitance	C_{iss} C_{oss} C_{rss}	V_{GS} = 0 V, V_{DS} = 25 V, f = 1 MHz		5100 1900 800	6120 2660 1200	pF
Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$t_{d(on)}$ t_r $t_{d(off)}$ t_f	V_{GS} = 15 V, V_{DS} = 50 V, I_D = 37.5 A, R_G = 1.6 Ω		16 40 50 20	32 40 75 40	ns
Total Gate Charge Gate-to-Source Charge Gate-to-Drain (Miller) Charge	$Q_{g(on)}$ Q_{gs} Q_{gd}	V_{GS} = 10 V, V_{DS} = 50V, I_D = 37.5A		200 40 92	300 60 180	nC
Body Diode Forward Voltage (1)	V_{SD}	I_S = 75A, V_{GS} = 0 V			1.3	V
Reverse Recovery Time (Body Diode)	t_{rr}	I_F = 10 A, di/dt = 100 A/µs		200		ns
Reverse Recovery Charge	Q_{rr}	I_F = 10 A, di/dt = 100 A/µs		1.4		µC

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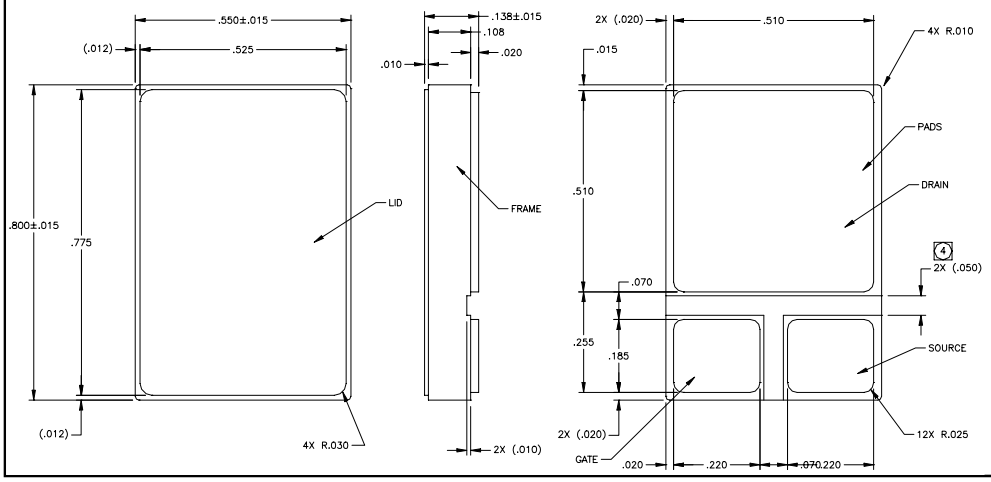
Mechanical Outline
CoolPack™2



Note: Pin-out shown for standard polarity

PACKAGE DATA

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