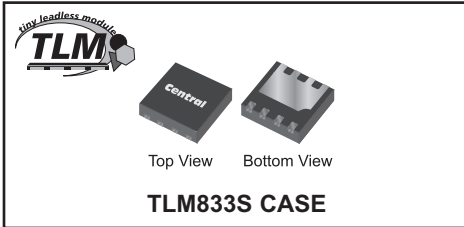


CTLT953-M833S

**SURFACE MOUNT  
HIGH CURRENT  
PNP SILICON TRANSISTOR**



www.centrasemi.com



**DESCRIPTION:**

The CENTRAL SEMICONDUCTOR CTLT953-M833S is a high performance 5.0A high current PNP transistor designed for applications where small size and operational efficiency are prime requirements. With a maximum power dissipation of 4.5W, and a very small package footprint, this device is 80% smaller than a comparable SOT-223 device. This leadless package design has a power density at least twice that of equivalent package devices.

**MARKING CODE: CHA4S**

**APPLICATIONS:**

- Motor control
- Load switches
- Display drives
- Relay drives

**FEATURES:**

- High Voltage (140V)
- High Current (5.0A)
- Low  $V_{CE(SAT)}$  (420mV MAX @ 4.0A)
- High Thermal Efficiency
- 3 x 3mm TLM™ case

**MAXIMUM RATINGS:** ( $T_A=25^\circ\text{C}$ )

Collector-Base Voltage
Collector-Emitter Voltage
Emitter-Base Voltage
Continuous Collector Current
Power Dissipation (Note 1)
Power Dissipation (Note 2)
Power Dissipation (Note 3)
Operating and Storage Junction Temperature
Thermal Resistance (Note 1)
Thermal Resistance (Note 2)
Thermal Resistance (Note 3)

SYMBOL		UNITS
$V_{CBO}$	140	V
$V_{CEO}$	100	V
$V_{EBO}$	6.0	V
$I_C$	5.0	A
$P_D$	4.5	W
$P_D$	4.0	W
$P_D$	2.5	W
$T_J, T_{stg}$	-65 to +150	$^\circ\text{C}$
$\theta_{JA}$	27.78	$^\circ\text{C/W}$
$\theta_{JA}$	31.25	$^\circ\text{C/W}$
$\theta_{JA}$	50.00	$^\circ\text{C/W}$

**ELECTRICAL CHARACTERISTICS:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$I_{CBO}$	$V_{CB}=100\text{V}$			50	nA
$I_{CBO}$	$V_{CB}=100\text{V}, T_A=100^\circ\text{C}$			1.0	$\mu\text{A}$
$I_{CER}$	$V_{CE}=100\text{V}, R_{BE}\leq 1.0\text{k}\Omega$			50	nA
$I_{EBO}$	$V_{EB}=6.0\text{V}$			10	nA
$BV_{CBO}$	$I_C=100\mu\text{A}$	140	170		V
$BV_{CER}$	$I_C=10\text{mA}, R_{BE}\leq 1.0\text{k}\Omega$	140	150		V
$BV_{CEO}$	$I_C=10\text{mA}$	100	120		V
$BV_{EBO}$	$I_E=100\mu\text{A}$	6.0	9.0		V
$V_{CE(SAT)}$	$I_C=100\text{mA}, I_B=10\text{mA}$		20	50	mV
$V_{CE(SAT)}$	$I_C=1.0\text{A}, I_B=100\text{mA}$		90	120	mV
$V_{CE(SAT)}$	$I_C=2.0\text{A}, I_B=200\text{mA}$		170	220	mV
$V_{CE(SAT)}$	$I_C=4.0\text{A}, I_B=400\text{mA}$		320	420	mV
$V_{BE(SAT)}$	$I_C=4.0\text{A}, I_B=400\text{mA}$		1.0	1.2	V

Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 75 mm<sup>2</sup>  
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 75 mm<sup>2</sup>  
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 25 mm<sup>2</sup>

R0 (8-August 2012)

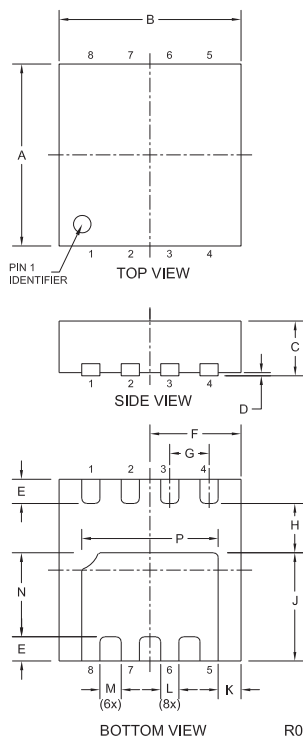
**CTLT953-M833S**  
**SURFACE MOUNT**  
**HIGH CURRENT**  
**PNP SILICON TRANSISTOR**



**ELECTRICAL CHARACTERISTICS - Continued:** ( $T_A=25^\circ\text{C}$  unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
$h_{FE}$	$V_{CE}=1.0\text{V}, I_C=10\text{mA}$	100			
$h_{FE}$	$V_{CE}=1.0\text{V}, I_C=1.0\text{A}$	100	200	300	
$h_{FE}$	$V_{CE}=1.0\text{V}, I_C=3.0\text{A}$	50	70		
$h_{FE}$	$V_{CE}=1.0\text{V}, I_C=4.0\text{A}$	30	45		
$h_{FE}$	$V_{CE}=1.0\text{V}, I_C=10\text{A}$		15		
$f_T$	$V_{CE}=10\text{V}, I_C=100\text{mA}, f=50\text{MHz}$		150		MHz
$C_{ob}$	$V_{CB}=10\text{V}, I_E=0, f=1.0\text{MHz}$		45		pF

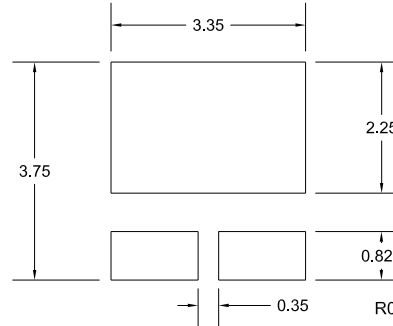
**TLM833S CASE - MECHANICAL OUTLINE**



SYMBOL	DIMENSIONS			
	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.112	0.124	2.85	3.15
B	0.112	0.124	2.85	3.15
C	0.031	0.039	0.80	1.00
D	0.000	0.002	0.00	0.05
E	0.012	0.020	0.30	0.50
F	0.056	0.062	1.43	1.57
G	0.026		0.65	
H	0.030	0.033	0.75	0.85
J	0.065	0.073	1.65	1.85
K	0.012	0.016	0.30	0.40
L	0.010	0.014	0.25	0.35
M	0.012	0.016	0.30	0.40
N	0.047	0.057	1.20	1.45
P	0.081	0.091	2.07	2.32

TLM833S (REV:R0)

**REQUIRED MOUNTING PADS**  
(Dimensions in mm)



Failure to use this mounting pad layout may result in damage to device.

R0 (8-August 2012)

**LEAD CODE:**

- |            |              |
|------------|--------------|
| 1) Emitter | 5) Collector |
| 2) Emitter | 6) Collector |
| 3) Base    | 7) Collector |
| 4) N.C.    | 8) Collector |

**MARKING CODE: CHA4S**