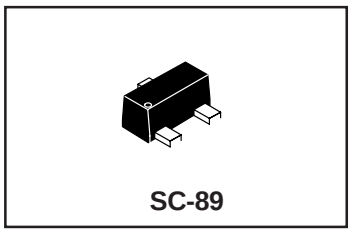
Bias Resistor Transistors

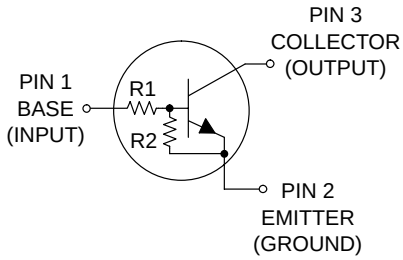
NPN Silicon Surface Mount Transistors with Monolithic Bias Resistor Network

LDTC114EET1G Series
S-LDTC114EET1G Series



This new series of digital transistors is designed to replace a single device and its external resistor bias network. The BRT (Bias Resistor Transistor) contains a single transistor with a monolithic bias network consisting of two resistors; a series base resistor and a base-emitter resistor. The BRT eliminates these individual components by integrating them into a single device. The use of a BRT can reduce both system cost and board space. The device is housed in the SC-89 package which is designed for low power surface mount applications.

- Simplifies Circuit Design
- Reduces Board Space
- Reduces Component Count
- The SC-89 package can be soldered using wave or reflow. The modified gull-winged leads absorb thermal stress during soldering eliminating the possibility of damage to the die.
- We declare that the material of product compliance with RoHS requirements.
- S- Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable.



MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	Vdc
Collector-Emitter Voltage	V_{CEO}	50	Vdc
Collector Current	I_C	100	mAdc

THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Total Device Dissipation, FR−4 Board (Note 1) @ T_A = 25°C Derate above 25°C	P_D	200 1.6	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 1)	$R_{\theta JA}$	600	°C/W
Total Device Dissipation, FR−4 Board (Note 2) @ T_A = 25°C Derate above 25°C	P_D	300 2.4	mW mW/°C
Thermal Resistance, Junction−to−Ambient (Note 2)	$R_{\theta JA}$	400	°C/W
Junction and Storage Temperature Range	T_J, T_{stg}	−55 to +150	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. FR−4 @ Minimum Pad
2. FR−4 @ 1.0 × 1.0 Inch Pad

LDTC114EET1G Series;S-LDTC114EET1G Series

ORDERING INFORMATION AND RESISTOR VALUES

Device	Marking	R1 (K)	R2 (K)	Package	Shipping†
LDTC114EET1G S-LDTC114EET1G	8A	10	10	SC−89	3000 Tape & Reel
LDTC124EET1G S-LDTC124EET1G	8B	22	22	SC−89	3000 Tape & Reel
LDTC144EET1G S-LDTC144EET1G	8C	47	47	SC−89	3000 Tape & Reel
LDTC114YET1G S-LDTC114YET1G	8D	10	47	SC−89	3000 Tape & Reel
LDTC114TET1G S-LDTC114TET1G	94	10	∞	SC−89	3000 Tape & Reel
LDTC143TET1G S-LDTC143TET1G	8F	4.7	∞	SC−89	3000 Tape & Reel
LDTC123EET1G S-LDTC123EET1G	8H	2.2	2.2	SC−89	3000 Tape & Reel
LDTC143EET1G S-LDTC143EET1G	8J	4.7	4.7	SC−89	3000 Tape & Reel
LDTC143ZET1G S-LDTC143ZET1G	8K	4.7	47	SC−89	3000 Tape & Reel
LDTC124XET1G S-LDTC124XET1G	8L	22	47	SC−89	3000 Tape & Reel
LDTC123JET1G S-LDTC123JET1G	8M	2.2	47	SC−89	3000 Tape & Reel
LDTC115EET1G S-LDTC115EET1G	8N	100	100	SC−89	3000 Tape & Reel
LDTC144WET1G S-LDTC144WET1G	8P	47	22	SC−89	3000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Collector−Base Cutoff Current (V_{CB} = 50 V, I_E = 0)		I_{CBO}	−	−	100	nAdc
Collector−Emitter Cutoff Current (V_{CE} = 50 V, I_B = 0)		I_{CEO}	−	−	500	nAdc
Emitter−Base Cutoff Current (V_{EB} = 6.0 V, I_C = 0)	LDTC114EET1G	I_{EBO}	−	−	0.5	mAdc
	LDTC124EET1G		−	−	0.2	
	LDTC144EET1G		−	−	0.1	
	LDTC114YET1G		−	−	0.2	
	LDTC114TET1G		−	−	0.9	
	LDTC143TET1G		−	−	1.9	
	LDTC123EET1G		−	−	2.3	
	LDTC143EET1G		−	−	1.5	
	LDTC143ZET1G		−	−	0.18	
	LDTC124XET1G		−	−	0.13	
	LDTC123JET1G		−	−	0.2	
	LDTC115EET1G		−	−	0.05	
	LDTC144WET1G		−	−	0.13	
Collector−Base Breakdown Voltage (I_C = 10 μA, I_E = 0)		$V_{(BR)CBO}$	50	−	−	Vdc
Collector−Emitter Breakdown Voltage (Note 3) (I_C = 2.0 mA, I_B = 0)		$V_{(BR)CEO}$	50	−	−	Vdc

LDTC114EET1G Series;S-LDTC114EET1G Series

Characteristic		Symbol	Min	Typ	Max	Unit
ON CHARACTERISTICS (Note 3)						
DC Current Gain	LDTC114EET1G	h_{FE}	35	60	–	
(V_{CE} = 10 V, I_C = 5.0 mA)	LDTC124EET1G		60	100	–	
	LDTC144EET1G		80	140	–	
	LDTC114YET1G		80	140	–	
	LDTC114TET1G		160	350	–	
	LDTC143TET1G		160	350	–	
	LDTC123EET1G		8.0	15	–	
	LDTC143EET1G		15	30	–	
	LDTC143ZET1G		80	200	–	
	LDTC124XET1G		80	150	–	
	LDTC123JET1G		80	140	–	
	LDTC115EET1G		80	150	–	
	LDTC144WET1G		80	140	–	
Collector−Emitter Saturation Voltage (I_C = 10 mA, I_B = 0.3 mA)		$V_{CE(sat)}$	–	–	0.25	Vdc
(I_C = 10 mA, I_B = 5 mA) LDTC123EET1G						
(I_C = 10 mA, I_B = 1 mA) LDTC143TET1G/LDTC114TET1G/ LDTC143EET1G/LDTC143ZET1G/LDTC124XET1G						
Output Voltage (on)		V_{OL}				Vdc
(V_{CC} = 5.0 V, V_B = 2.5 V, R_L = 1.0 kΩ)	LDTC114EET1G		–	–	0.2	
	LDTC124EET1G		–	–	0.2	
	LDTC114YET1G		–	–	0.2	
	LDTC114TET1G		–	–	0.2	
	LDTC143TET1G		–	–	0.2	
	LDTC123EET1G		–	–	0.2	
	LDTC143EET1G		–	–	0.2	
	LDTC143ZET1G		–	–	0.2	
	LDTC124XET1G		–	–	0.2	
	LDTC123JET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 3.5 V, R_L = 1.0 kΩ)	LDTC144EET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 5.5 V, R_L = 1.0 kΩ)	LDTC115EET1G		–	–	0.2	
(V_{CC} = 5.0 V, V_B = 4.0 V, R_L = 1.0 kΩ)	LDTC144WET1G		–	–	0.2	
Output Voltage (off) (V_{CC} = 5.0 V, V_B = 0.5 V, R_L = 1.0 kΩ)		V_{OH}	4.9	–	–	Vdc
(V_{CC} = 5.0 V, V_B = 0.25 V, R_L = 1.0 kΩ)	LDTC143TET1G					
	LDTC143ZET1G					
	LDTC114TET1G					
	LDTC115EET1G					

3. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) (Continued)

Characteristic		Symbol	Min	Typ	Max	Unit
Input Resistor	LDTC114EET1G	R1	7.0	10	13	kΩ
	LDTC124EET1G		15.4	22	28.6	
	LDTC144EET1G		32.9	47	61.1	
	LDTC114YET1G		7.0	10	13	
	LDTC114TET1G		7.0	10	13	
	LDTC143TET1G		3.3	4.7	6.1	
	LDTC123EET1G		1.5	2.2	2.9	
	LDTC143EET1G		3.3	4.7	6.1	
	LDTC143ZET1G		3.3	4.7	6.1	
	LDTC124XET1G		15.4	22	28.6	
	LDTC123JET1G		1.54	2.2	2.86	
	LDTC115EET1G		70	100	130	
	LDTC144WET1G		32.9	47	61.1	
Resistor Ratio	LDTC114EET1G/LDTC124EET1G/ LDTC144EET1G/LDTC115EET1G	R_1/R_2	0.8	1.0	1.2	
	LDTC114YET1G		0.17	0.21	0.25	
	LDTC143TET1G/LDTC114TET1G		–	–	–	
	LDTC123EET1G/LDTC143EET1G		0.8	1.0	1.2	
	LDTC143ZET1G		0.055	0.1	0.185	
	LDTC124XET1G		0.38	0.47	0.56	
	LDTC123JET1G		0.038	0.047	0.056	
	LDTC144WET1G		1.7	2.1	2.6	

LDTC114EET1G Series;S-LDTC114EET1G Series

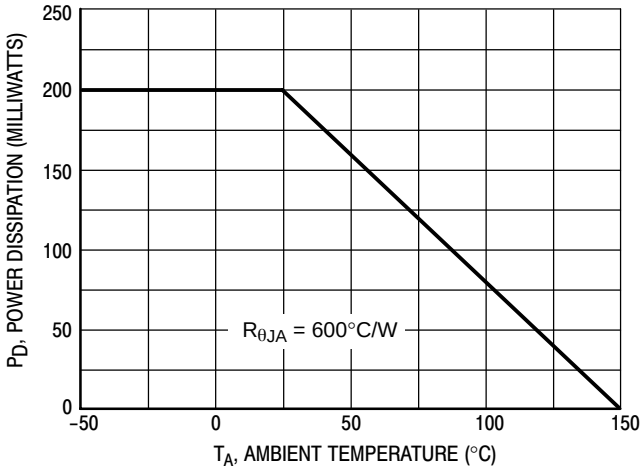


Figure 1. Derating Curve

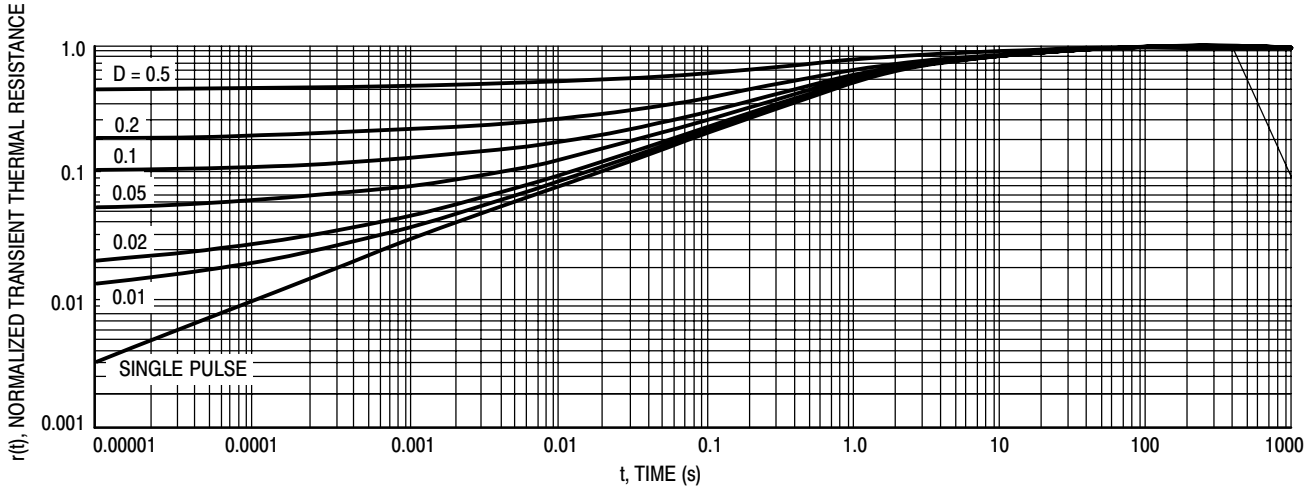


Figure 2. Normalized Thermal Response

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC114EET1G

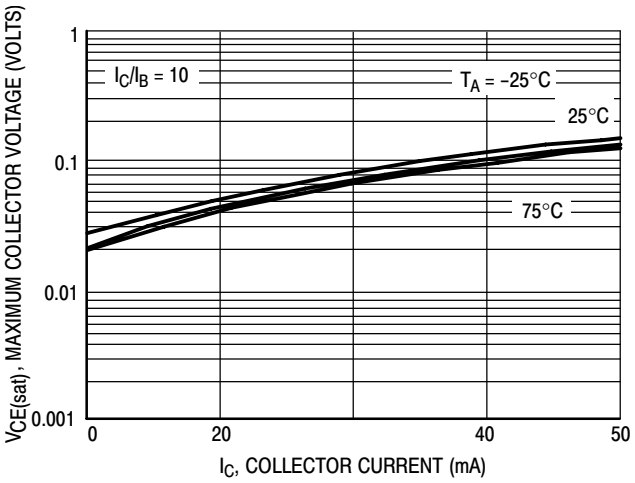


Figure 3. $V_{CE(sat)}$ versus I_C

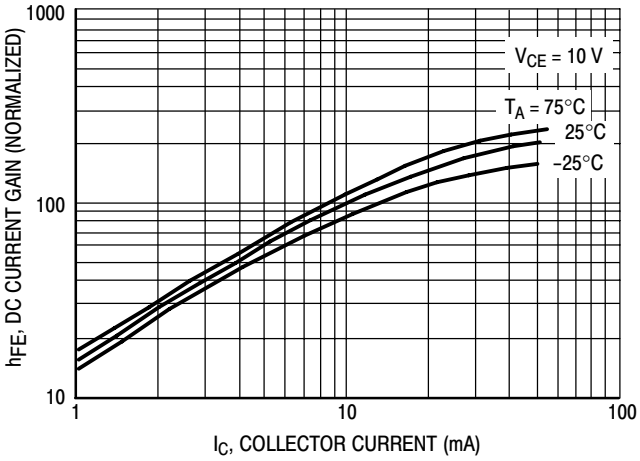


Figure 4. DC Current Gain

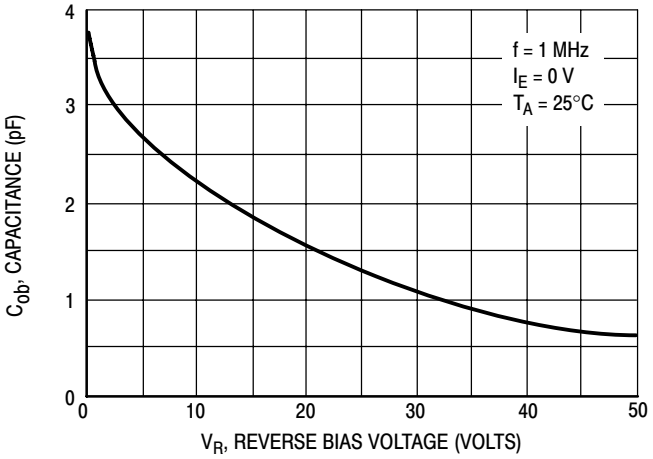


Figure 5. Output Capacitance

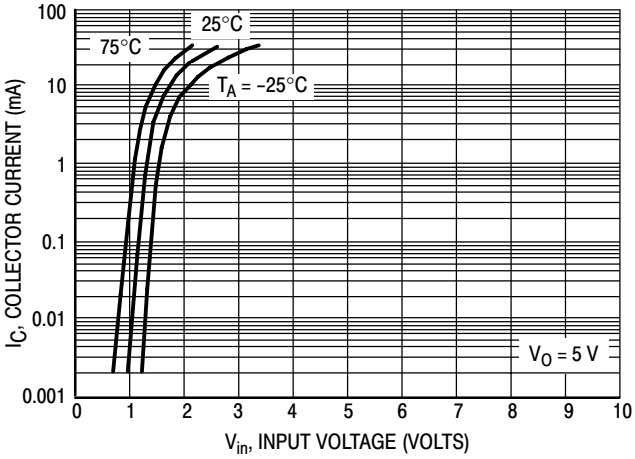


Figure 6. Output Current versus Input Voltage

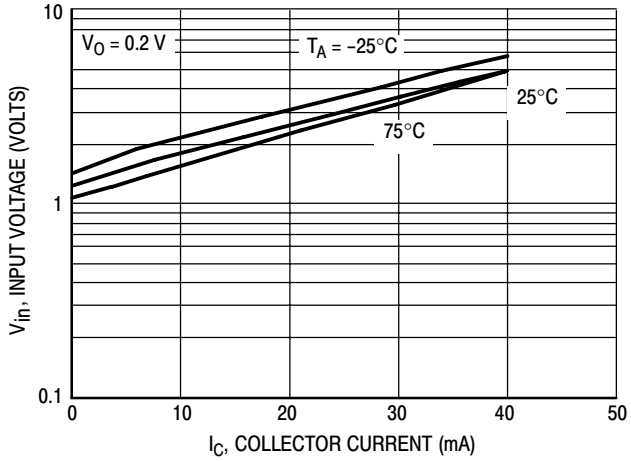


Figure 7. Input Voltage versus Output Current

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC123EET1G

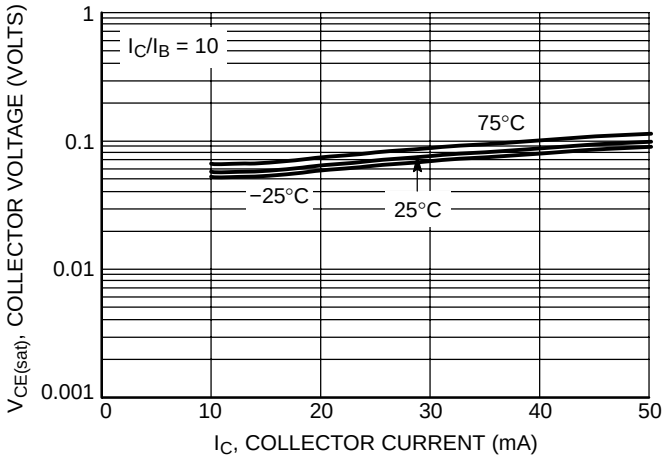


Figure 8. $V_{CE(sat)}$ versus I_C

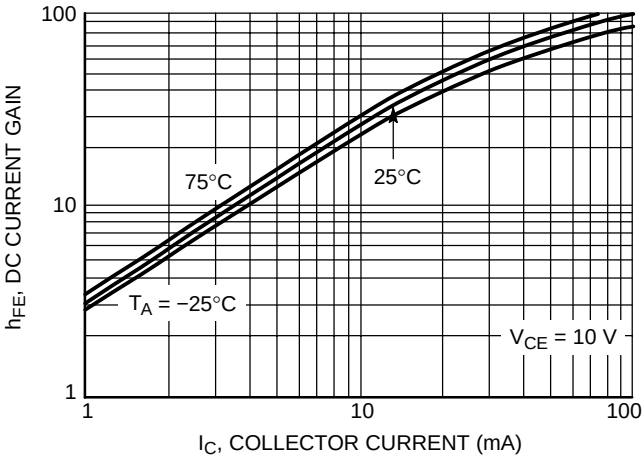


Figure 9. DC Current Gain

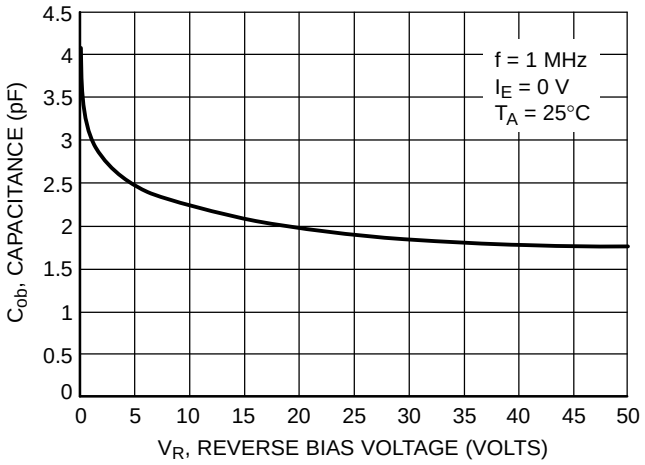


Figure 10. Output Capacitance

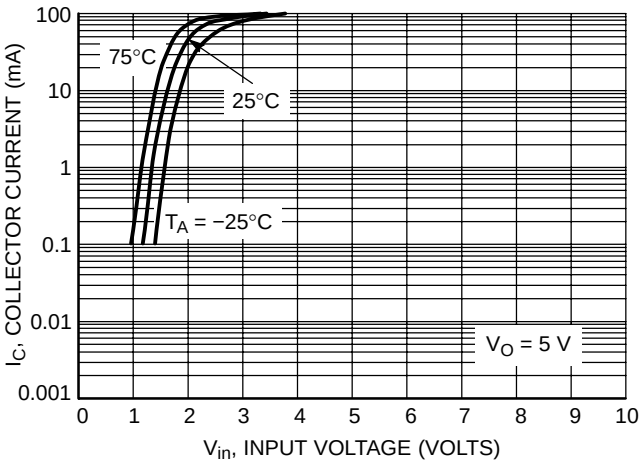


Figure 11. Output Current versus Input Voltage

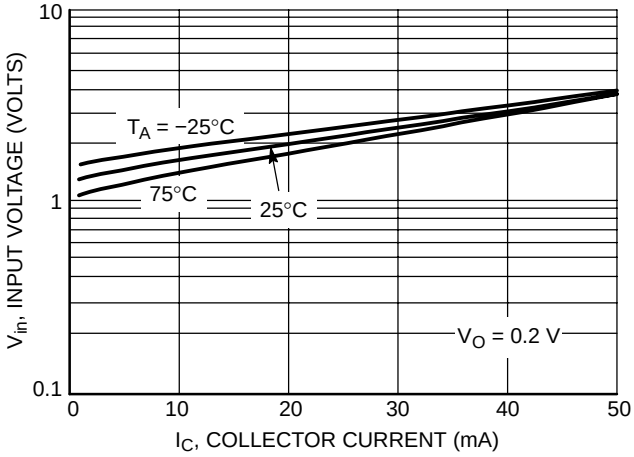


Figure 12. Input Voltage versus Output Current

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC124EET1G

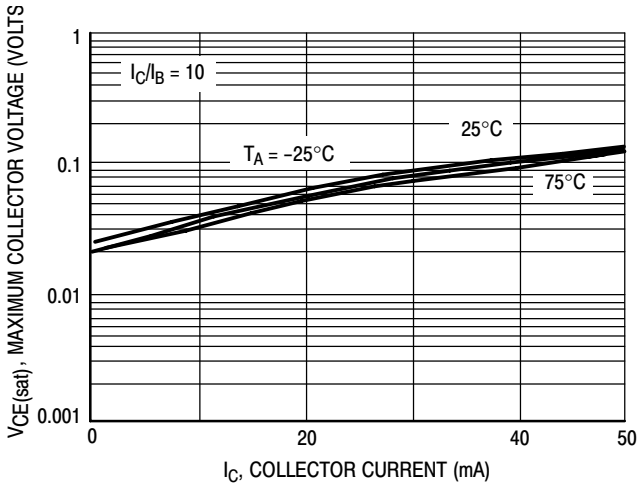


Figure 13. $V_{CE(sat)}$ versus I_C

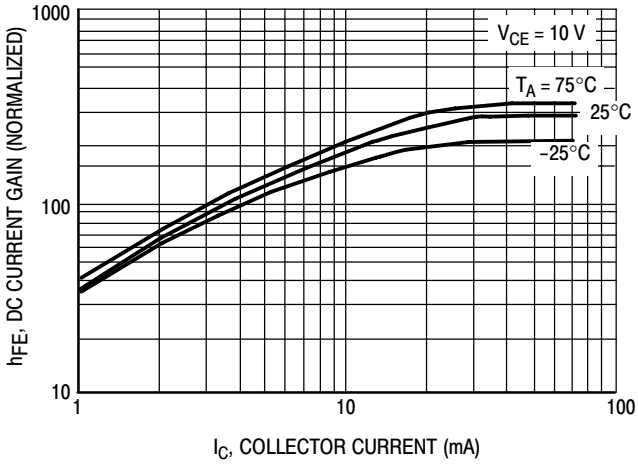


Figure 14. DC Current Gain

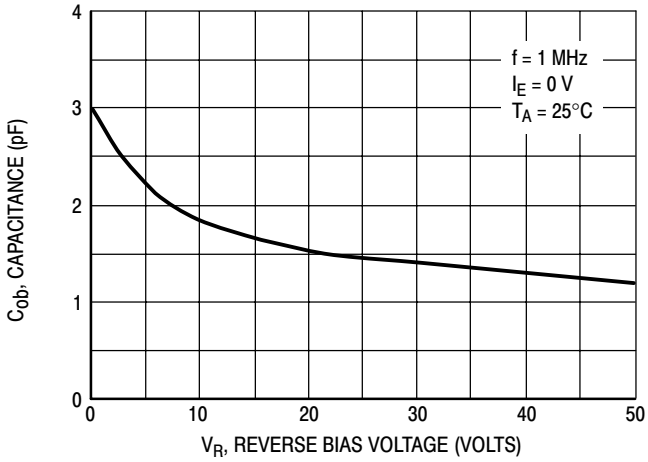


Figure 15. Output Capacitance

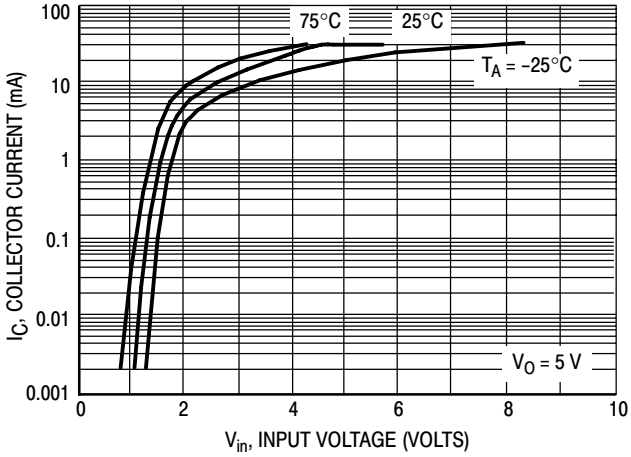


Figure 16. Output Current versus Input Voltage

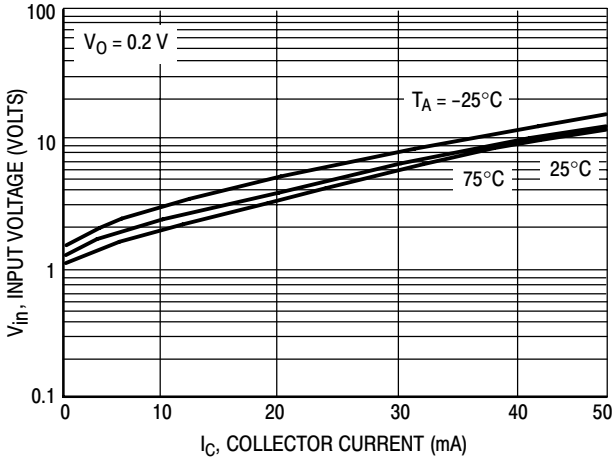


Figure 17. Input Voltage versus Output Current

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC144EET1G

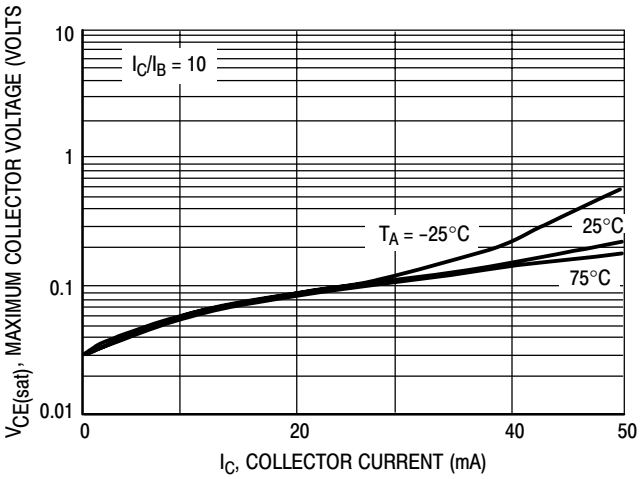


Figure 18. $V_{CE(sat)}$ versus I_C

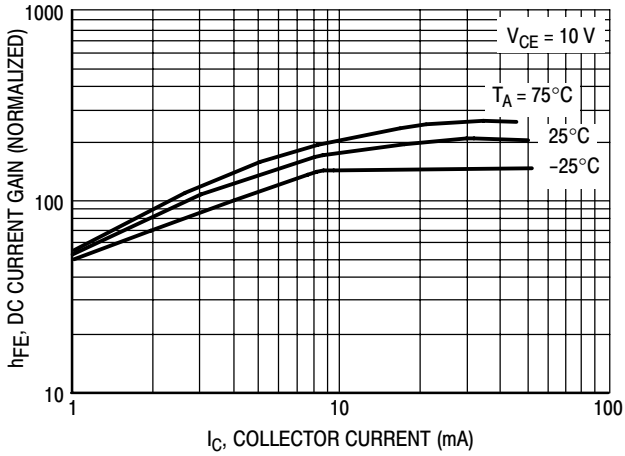


Figure 19. DC Current Gain

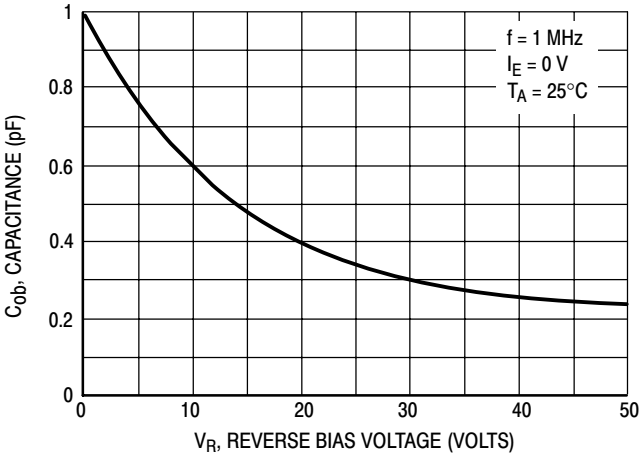


Figure 20. Output Capacitance

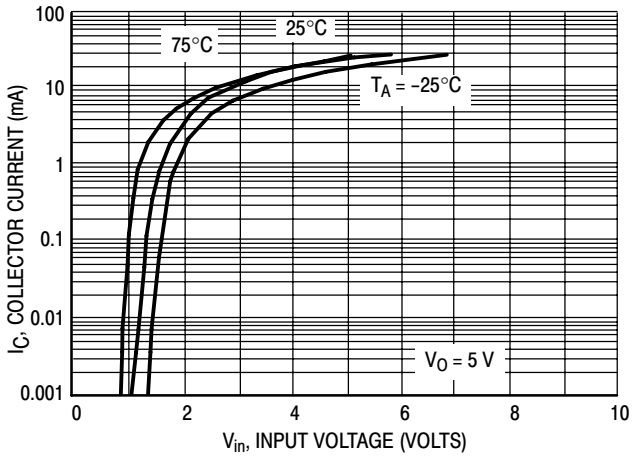


Figure 21. Output Current versus Input Voltage

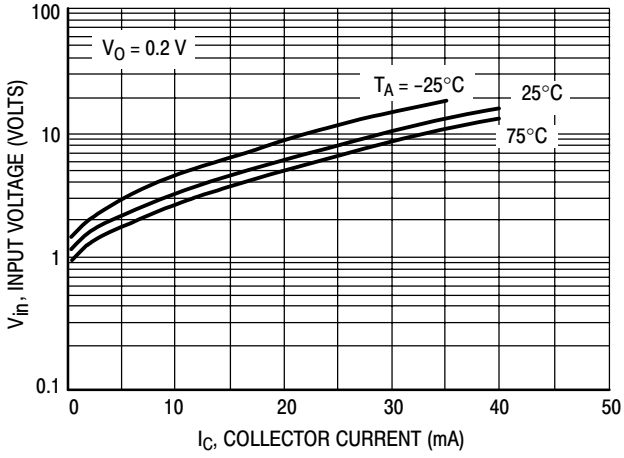


Figure 22. Input Voltage versus Output Current

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL ELECTRICAL CHARACTERISTICS − LDTC114YET1G

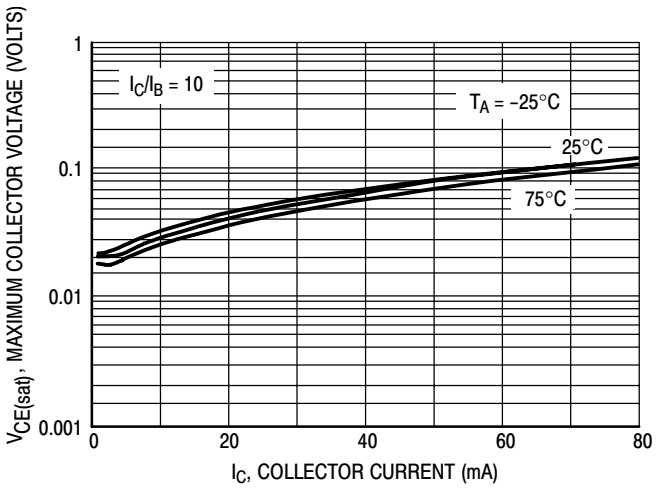


Figure 23. $V_{CE(sat)}$ versus I_C

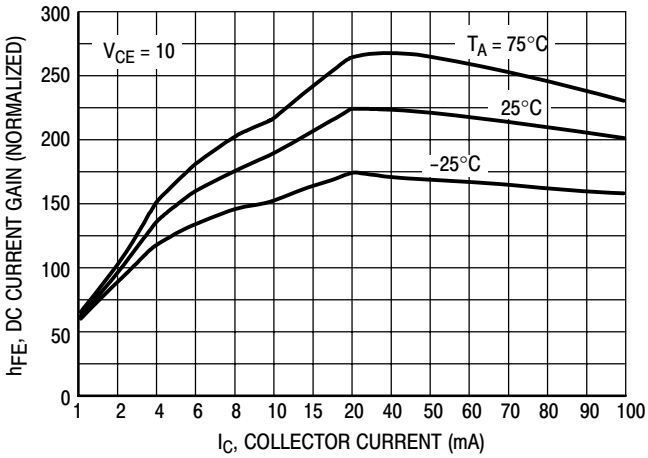


Figure 24. DC Current Gain

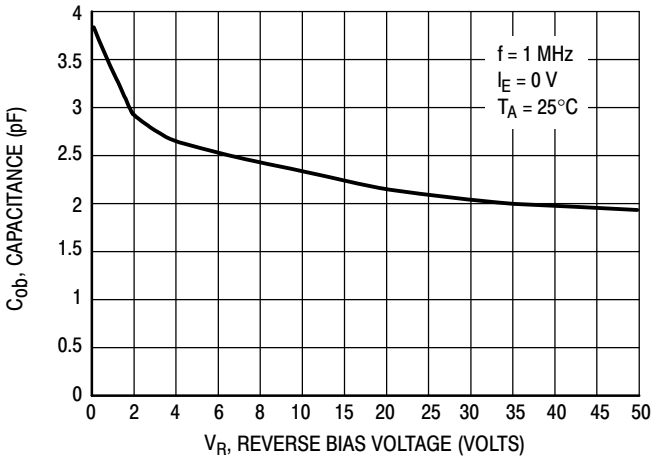


Figure 25. Output Capacitance

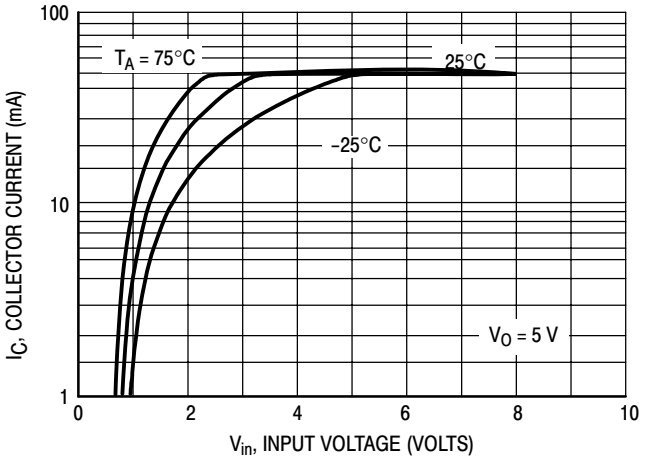


Figure 26. Output Current versus Input Voltage

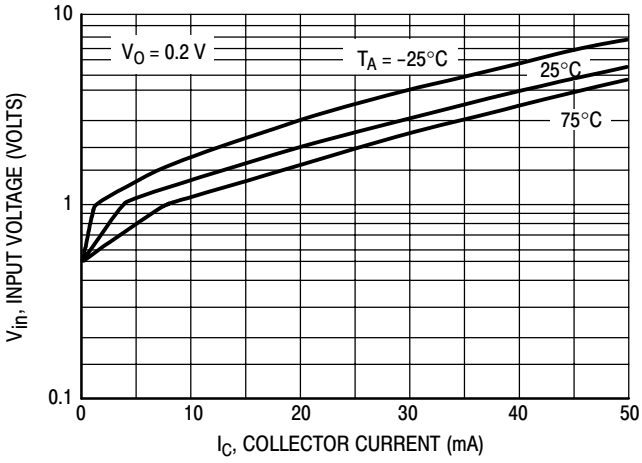


Figure 27. Input Voltage versus Output Current

LDTC114EET1G Series;S-LDTC114EET1G Series

TYPICAL APPLICATIONS FOR NPN BRTs

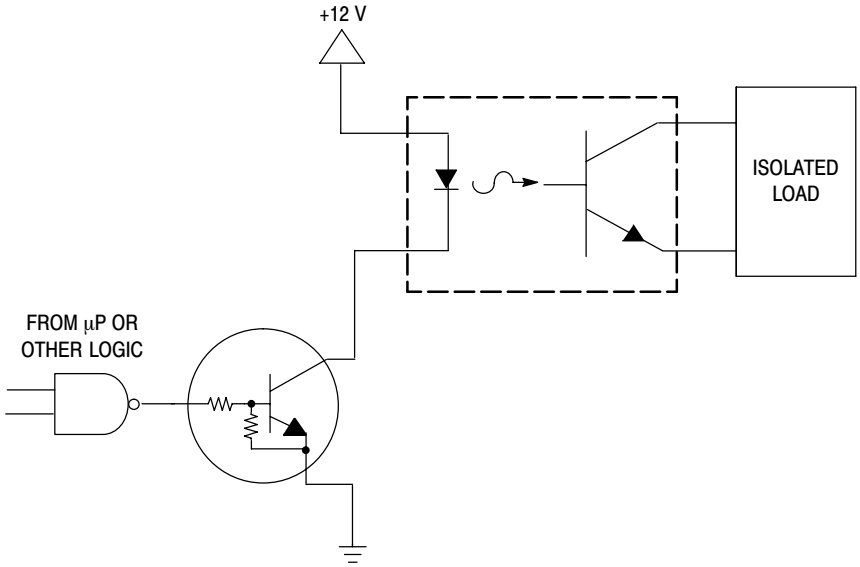


Figure 28. Level Shifter: Connects 12 or 24 Volt Circuits to Logic

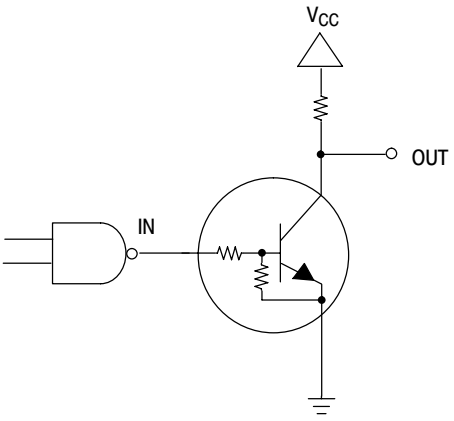


Figure 29. Open Collector Inverter: Inverts the Input Signal

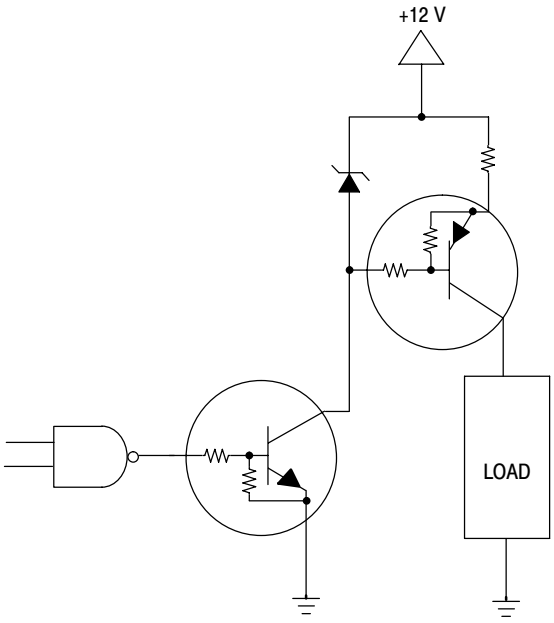
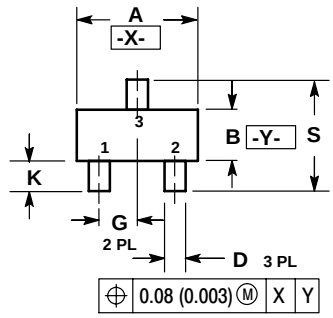
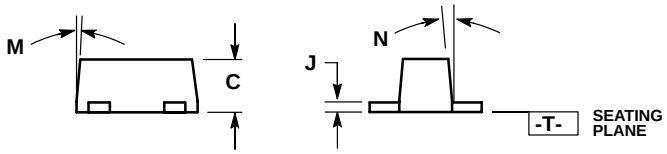


Figure 30. Inexpensive, Unregulated Current Source

LDTC114EET1G Series;S-LDTC114EET1G Series

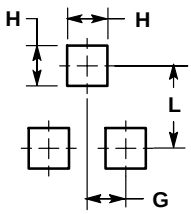
SC−89





NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. 463C-01 OBSOLETE, NEW STANDARD 463C-02.

	MILLIMETERS			INCHES		
DIM	MIN	NOM	MAX	MIN	NOM	MAX
A	1.50	1.60	1.70	0.059	0.063	0.067
B	0.75	0.85	0.95	0.030	0.034	0.040
C	0.60	0.70	0.80	0.024	0.028	0.031
D	0.23	0.28	0.33	0.009	0.011	0.013
G		0.50 BSC			0.020 BSC	
H		0.53 REF			0.021 REF	
J	0.10	0.15	0.20	0.004	0.006	0.008
K	0.30	0.40	0.50	0.012	0.016	0.020
L		1.10 REF			0.043 REF	
M	---	---	10 °	---	---	10 °
N	---	---	10 °	---	---	10 °
S	1.50	1.60	1.70	0.059	0.063	0.067



RECOMMENDED PATTERN OF SOLDER PADS