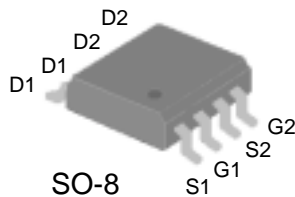


Dual N-channel Enhancement-mode Power MOSFETs

PRODUCT SUMMARY

BV_{DSS}	20V
$R_{DS(ON)}$	30m Ω
I_D	6A

 **Pb-free; RoHS-compliant SO-8**



DESCRIPTION

The SSM9926GM achieves fast switching performance with low gate charge without a complex drive circuit. It is suitable for low voltage applications such as DC/DC converters and general load-switching circuits.

The SSM9926GM is supplied in an RoHS-compliant SO-8 package, which is widely used for medium power commercial and industrial surface mount applications.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Units
V_{DS}	Drain-source voltage	20	V
V_{GS}	Gate-source voltage	± 12	V
I_D	Continuous drain current ³ , $T_A = 25^\circ\text{C}$ $T_A = 70^\circ\text{C}$	6	A
		4.8	A
I_{DM}	Pulsed drain current ^{1,2}	26	A
P_D	Total power dissipation ³ , $T_A = 25^\circ\text{C}$	2	W
	Linear derating factor	0.016	W/ $^\circ\text{C}$
T_{STG}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_J	Operating junction temperature range	-55 to 150	$^\circ\text{C}$

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Units
$R_{\theta JA}$	Maximum thermal resistance, junction-ambient ³	62.5	$^\circ\text{C}/\text{W}$

Notes:

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of 150 $^\circ\text{C}$.
2. Pulse width <300us, duty cycle <2%.
3. Mounted on a square inch of copper pad on FR4 board ; 135 $^\circ\text{C}/\text{W}$ when mounted on the minimum pad area required for soldering.

ELECTRICAL CHARACTERISTICS (at $T_j = 25^\circ\text{C}$, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-source breakdown voltage	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown voltage temperature coefficient	Reference to 25°C , $I_D=1\text{mA}$	-	0.03	-	$V/^\circ\text{C}$
$R_{DS(ON)}$	Static drain-source on-resistance ²	$V_{GS}=4.5V, I_D=6A$	-	-	30	$\text{m}\Omega$
		$V_{GS}=2.5V, I_D=5.2A$	-	-	45	$\text{m}\Omega$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	-	-	1.2	V
g_{fs}	Forward transconductance	$V_{DS}=10V, I_D=6A$	-	20	-	S
I_{DSS}	Drain-source leakage current	$V_{DS}=20V, V_{GS}=0V$	-	-	25	μA
		$V_{DS}=20V, V_{GS}=0V, T_j = 70^\circ\text{C}$	-	-	250	μA
I_{GSS}	Gate-source leakage current	$V_{GS}=\pm 12V$	-	-	± 100	nA
Q_g	Total gate charge ²	$I_D=6A$	-	23	35	nC
Q_{gs}	Gate-source charge	$V_{DS}=20V$	-	4.5	7	nC
Q_{gd}	Gate-drain ("Miller") charge	$V_{GS}=5V$	-	7	11	nC
$t_{d(on)}$	Turn-on delay time ²	$V_{DS}=10V$	-	30	60	ns
t_r	Rise time	$I_D=1A$	-	70	140	ns
$t_{d(off)}$	Turn-off delay time	$R_G=6\Omega, V_{GS}=5V$	-	40	80	ns
t_f	Fall time	$R_D=10\Omega$	-	65	130	ns
C_{iss}	Input capacitance	$V_{GS}=0V$	-	1035	-	pF
C_{oss}	Output capacitance	$V_{DS}=20V$	-	320	-	pF
C_{rss}	Reverse transfer capacitance	$f=1.0\text{MHz}$	-	150	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward voltage ²	$I_S=1.7A, V_{GS}=0V$	-	0.78	1.2	V
I_S	Continuous source current (body diode)	$V_D=V_G=0V, V_S=1.3V$	-	-	1.54	A

Notes:

1. Pulse width must be limited to avoid exceeding the maximum junction temperature of 150°C .

2. Pulse width $<300\mu s$, duty cycle $<2\%$.

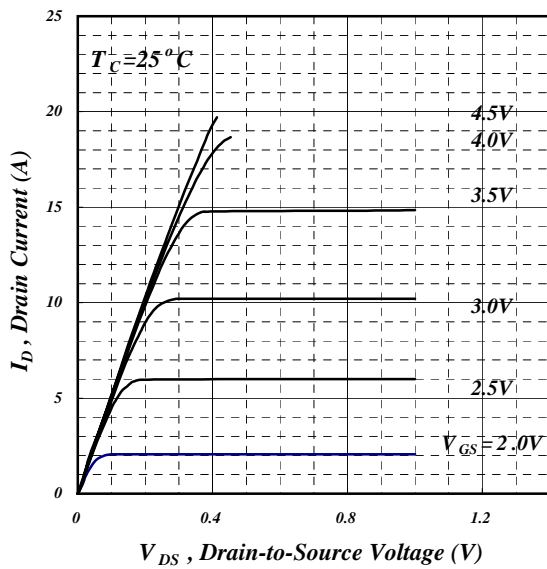


Fig 1. Typical Output Characteristics

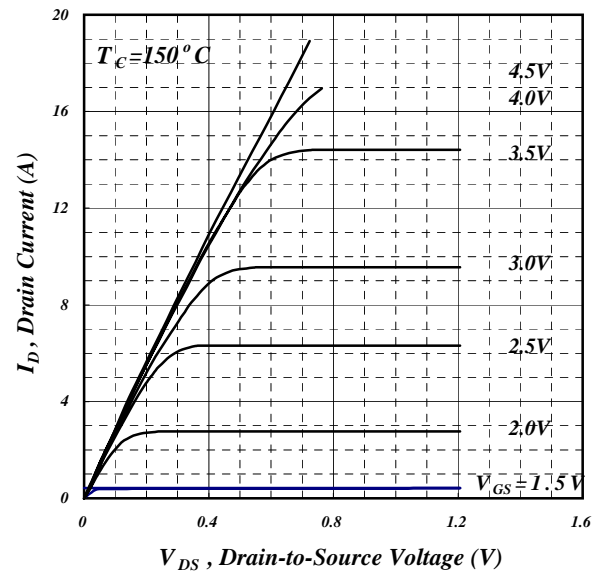


Fig 2. Typical Output Characteristics

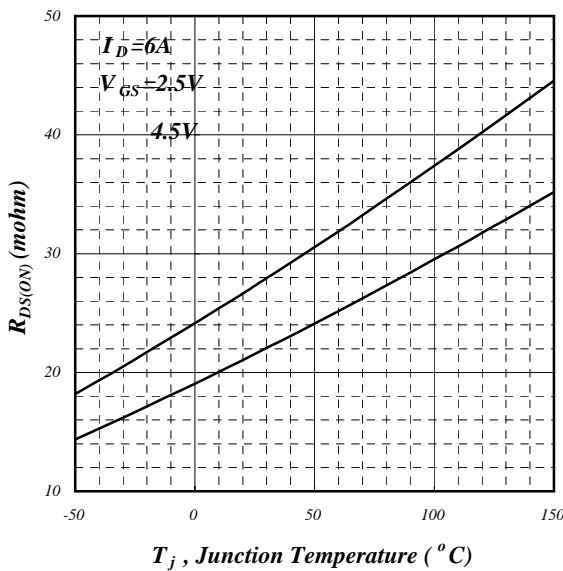


Fig 3. $R_{DS(ON)}$ vs. Junction Temperature

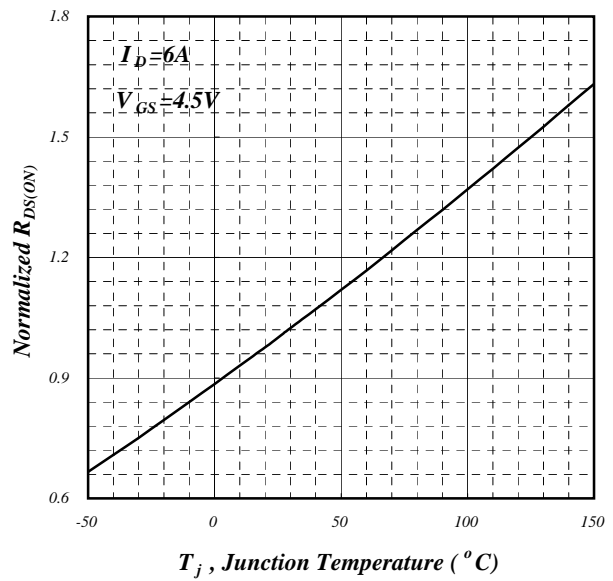


Fig 4. Normalized On-Resistance vs. Temperature

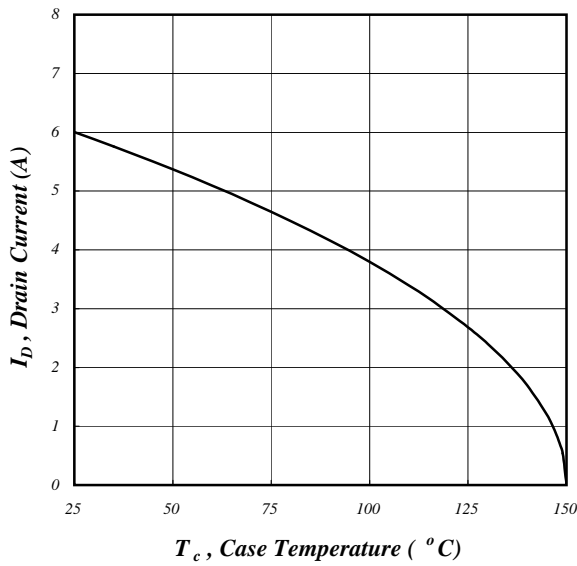


Fig 5. Maximum Drain Current vs. Case Temperature

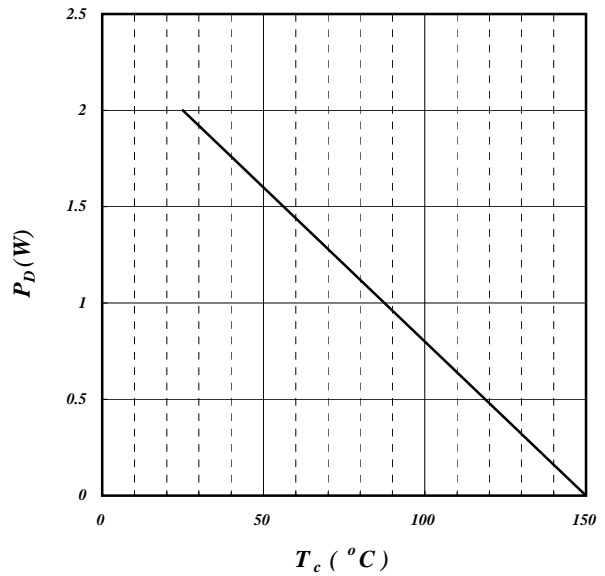


Fig 6. Typical Power Dissipation

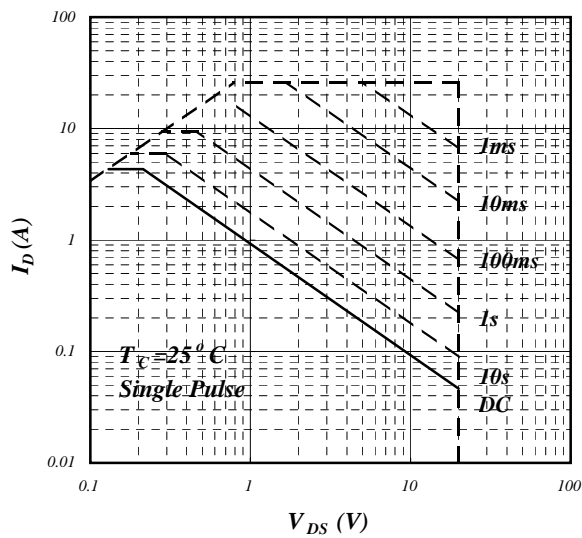


Fig 7. Maximum Safe Operating Area

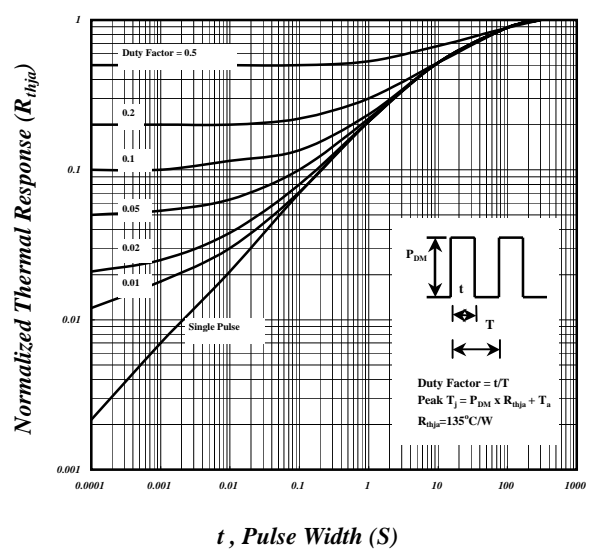


Fig 8. Effective Transient Thermal Impedance

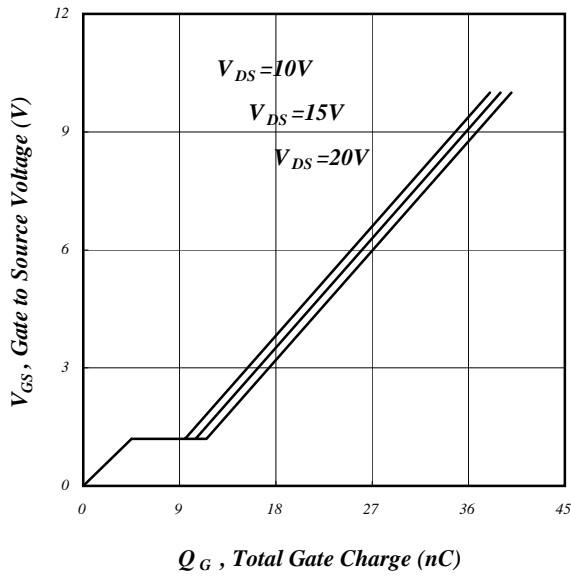


Fig 9. Typical Gate Charge vs. V_{GS}

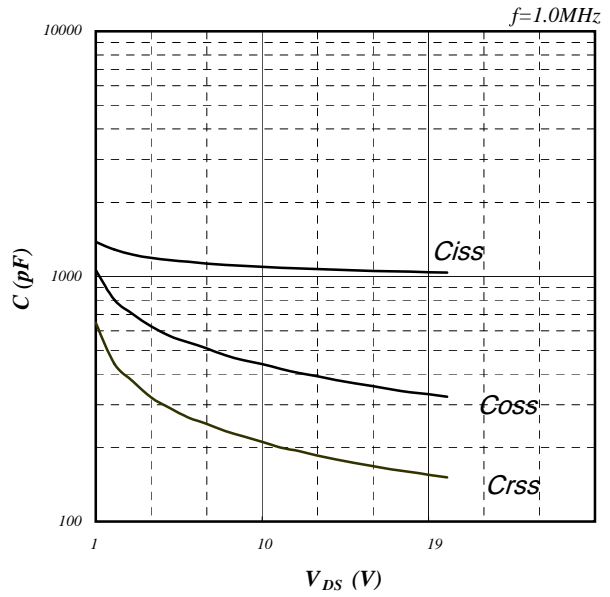


Fig 10. Typical Capacitance vs. V_{DS}

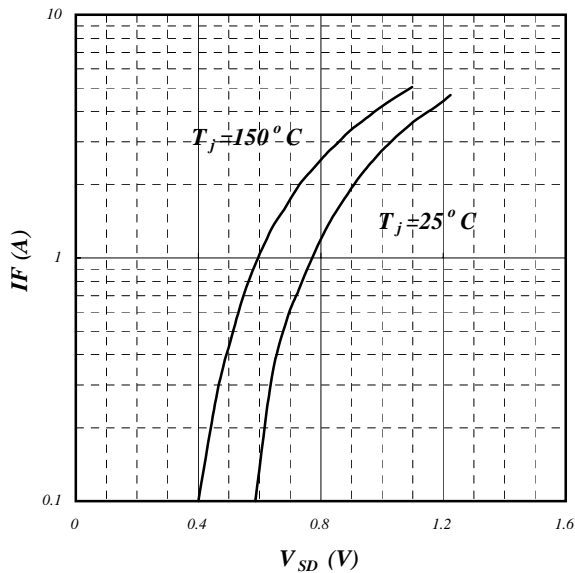


Fig 11. Forward Characteristic of Reverse Diode

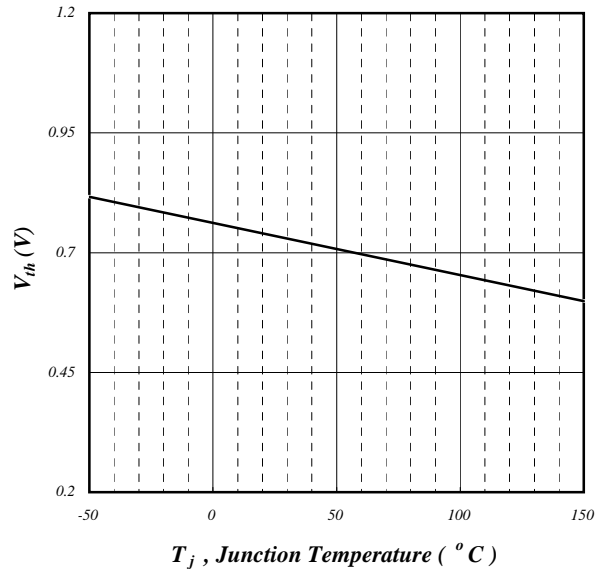


Fig 12. Gate Threshold Voltage vs. Junction Temperature

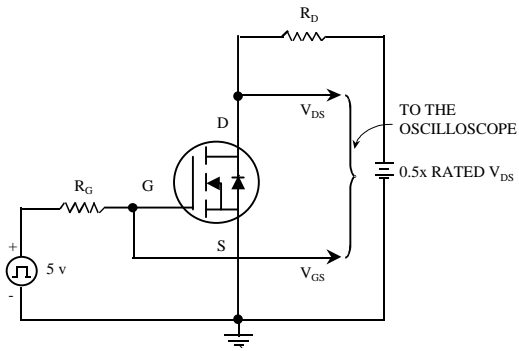


Fig 13. Switching Time Circuit

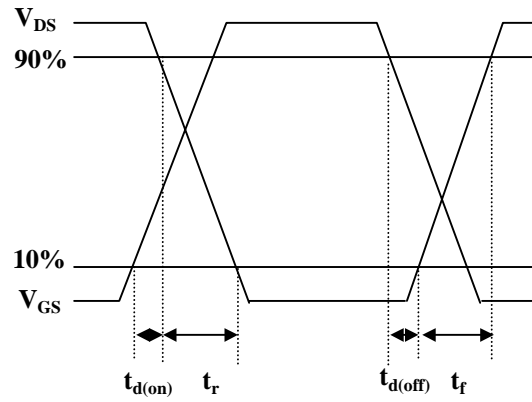


Fig 14. Switching Time Waveform

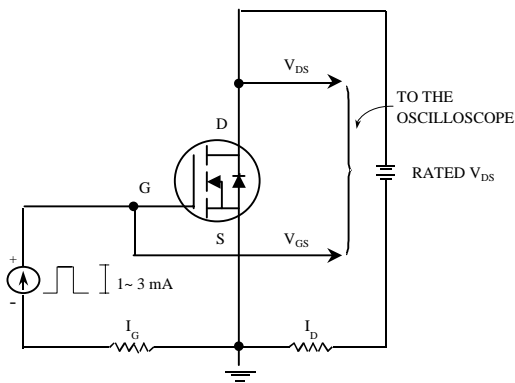


Fig 15. Gate Charge Circuit

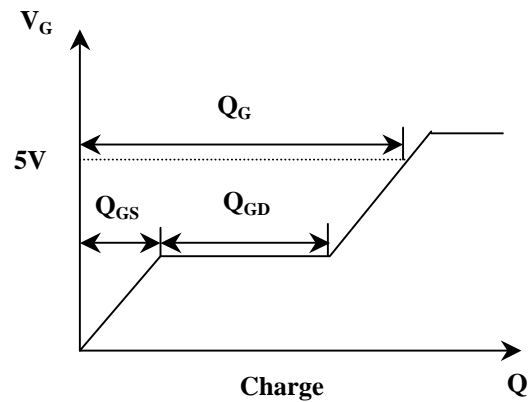
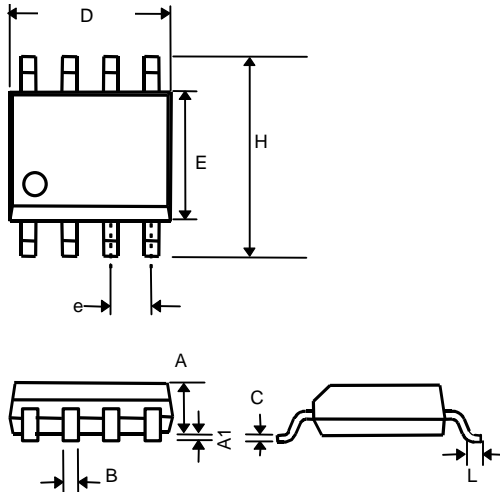


Fig 16. Gate Charge Waveform

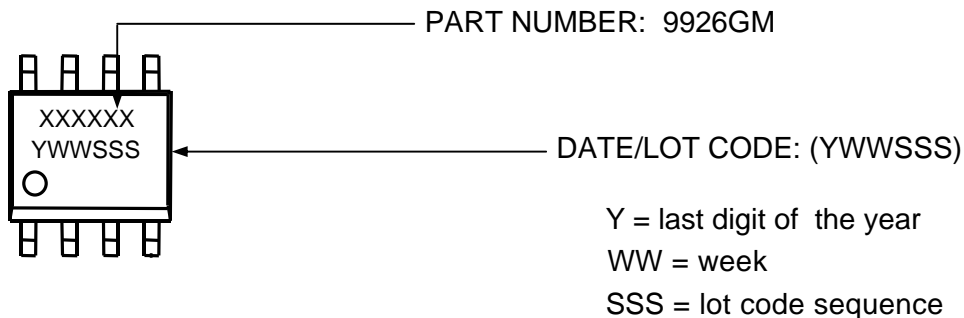
PHYSICAL DIMENSIONS



SYMBOL	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.33	0.51
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27(TYP)	
H	5.80	6.50
L	0.38	1.27

All dimensions in millimeters.
Dimensions do not include mold protrusions.

PART MARKING



PACKING: Moisture sensitivity level MSL3

3000 pcs in antistatic tape on a 13 inch (330mm) reel packed in a moisture barrier bag (MBB).

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