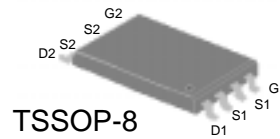


DUAL N-CANNEL ENHANCEMENT-MODE POWER MOSFETS

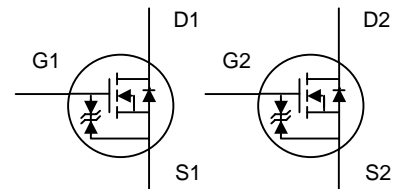
Low on-resistance
 Capable of 2.5V gate drive
 Ideal for DC/DC battery applications



BV_{DSS} 20V
 $R_{DS(ON)}$ 15m Ω
 I_D 6.8A

Description

Power MOSFETs from Silicon Standard provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



 This device is available with Pb-free lead finish (second-level interconnect) as SSM9922GEO.

Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units |
|------------------------------|---|------------|---------------------|
| V_{DS} | Drain-Source Voltage | 20 | V |
| V_{GS} | Gate-Source Voltage | ± 12 | V |
| $I_D @ T_A=25^\circ\text{C}$ | Drain Current ³ , $V_{GS} @ 4.5\text{V}$ | 6.8 | A |
| $I_D @ T_A=70^\circ\text{C}$ | Drain Current ³ , $V_{GS} @ 4.5\text{V}$ | 5.4 | A |
| I_{DM} | Pulsed Drain Current ¹ | 25 | A |
| $P_D @ T_A=25^\circ\text{C}$ | Total Power Dissipation | 1 | W |
| | Linear Derating Factor | 0.008 | W/ $^\circ\text{C}$ |
| T_{STG} | Storage Temperature Range | -55 to 150 | $^\circ\text{C}$ |
| T_J | Operating Junction Temperature Range | -55 to 150 | $^\circ\text{C}$ |

Thermal Data

| Symbol | Parameter | Value | Unit |
|--------|---|-------|---------------------------|
| Rthj-a | Thermal Resistance Junction-ambient ³ Max. | 125 | $^\circ\text{C}/\text{W}$ |

Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|------------------------------|---|---|------|------|----------|---------------------|
| BV_{DSS} | Drain-Source Breakdown Voltage | $V_{GS}=0V, I_D=250\mu A$ | 20 | - | - | V |
| $\Delta BV_{DSS}/\Delta T_j$ | Breakdown Voltage Temperature Coefficient | Reference to $25^\circ\text{C}, I_D=1\text{mA}$ | - | 0.05 | - | V/ $^\circ\text{C}$ |
| $R_{DS(ON)}$ | Static Drain-Source On-Resistance ² | $V_{GS}=4.5V, I_D=6A$ | - | - | 15 | m Ω |
| | | $V_{GS}=2.5V, I_D=4A$ | - | - | 20 | m Ω |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}=V_{GS}, I_D=1\text{mA}$ | 0.5 | - | 1.2 | V |
| g_{fs} | Forward Transconductance | $V_{DS}=4.5V, I_D=6A$ | - | 22 | - | S |
| I_{DSS} | Drain-Source Leakage Current ($T_j=25^\circ\text{C}$) | $V_{DS}=20V, V_{GS}=0V$ | - | - | 25 | μA |
| | Drain-Source Leakage Current ($T_j=70^\circ\text{C}$) | $V_{DS}=16V, V_{GS}=0V$ | - | - | 100 | μA |
| I_{GSS} | Gate-Source Leakage | $V_{GS}=\pm 12V$ | - | - | ± 10 | μA |
| Q_g | Total Gate Charge ² | $I_D=6A$ | - | 25 | 40 | nC |
| Q_{gs} | Gate-Source Charge | $V_{DS}=16V$ | - | 3 | - | nC |
| Q_{gd} | Gate-Drain ("Miller") Charge | $V_{GS}=4.5V$ | - | 9 | - | nC |
| $t_{d(on)}$ | Turn-on Delay Time ² | $V_{DS}=15V$ | - | 11 | - | ns |
| t_r | Rise Time | $I_D=1A$ | - | 12 | - | ns |
| $t_{d(off)}$ | Turn-off Delay Time | $R_G=3.3\Omega, V_{GS}=4.5V$ | - | 47 | - | ns |
| t_f | Fall Time | $R_D=15\Omega$ | - | 23 | - | ns |
| C_{iss} | Input Capacitance | $V_{GS}=0V$ | - | 1730 | 2770 | pF |
| C_{oss} | Output Capacitance | $V_{DS}=20V$ | - | 280 | - | pF |
| C_{rss} | Reverse Transfer Capacitance | $f=1.0\text{MHz}$ | - | 240 | - | pF |
| R_g | Gate Resistance | $f=1.0\text{MHz}$ | - | 2.2 | - | Ω |

Source-Drain Diode

| Symbol | Parameter | Test Conditions | Min. | Typ. | Max. | Units |
|----------|------------------------------------|--------------------------|------|------|------|-------|
| V_{SD} | Forward On Voltage ² | $I_S=0.84A, V_{GS}=0V$ | - | - | 1.2 | V |
| t_{rr} | Reverse Recovery Time ² | $I_S=6A, V_{GS}=0V,$ | - | 24 | - | ns |
| Q_{rr} | Reverse Recovery Charge | $dI/dt=100A/\mu\text{s}$ | - | 18 | - | nC |

Notes:

1. Pulse width limited by max. junction temperature.
2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Surface mounted on 1 in^2 copper pad of FR4 board; 208°C/W when mounted on min. copper pad.

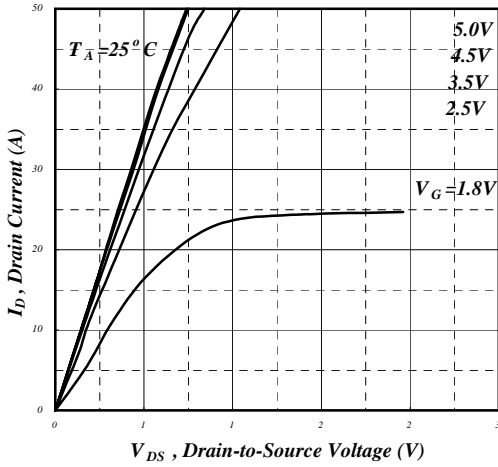


Fig 1. Typical Output Characteristics

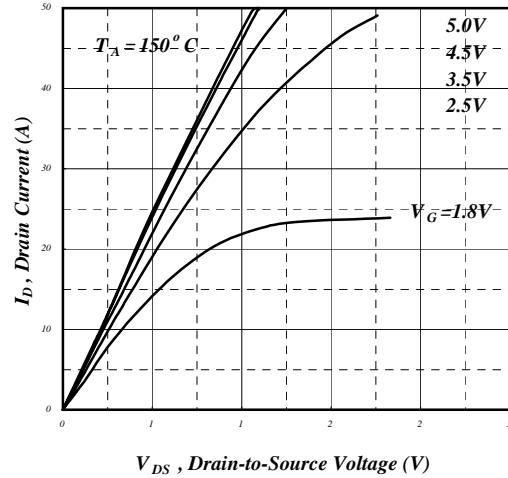


Fig 2. Typical Output Characteristics

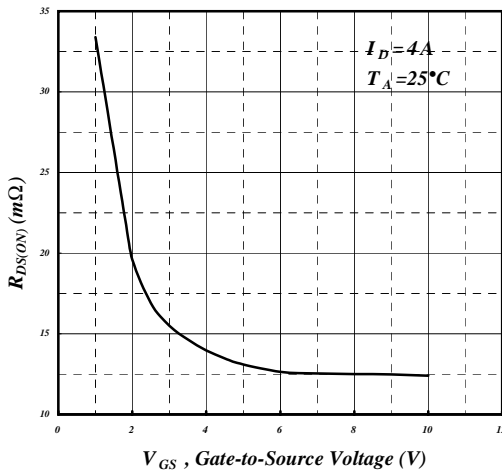


Fig 3. On-Resistance vs. Gate Voltage

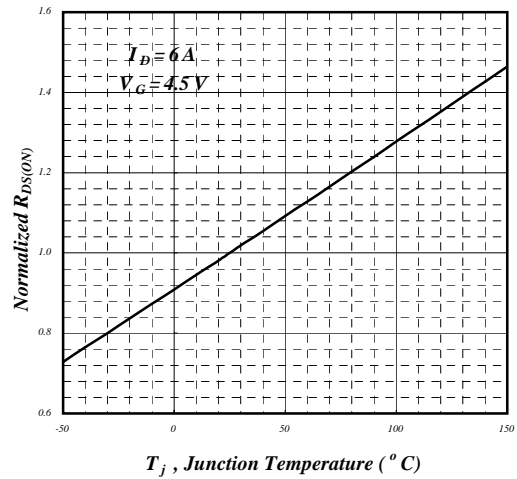


Fig 4. Normalized On-Resistance vs. Junction Temperature

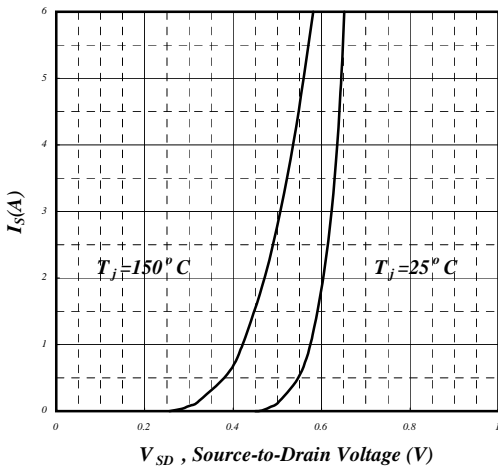


Fig 5. Forward Characteristic of Reverse Diode

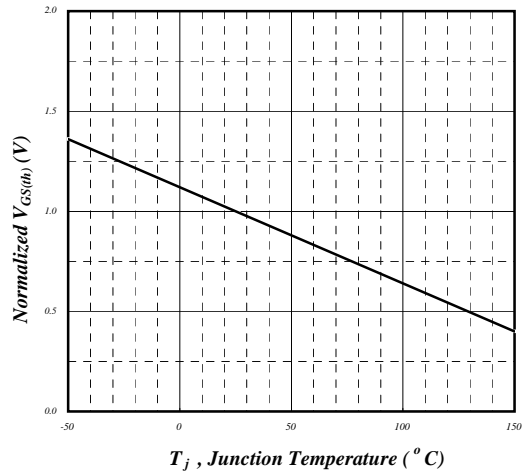


Fig 6. Gate Threshold Voltage vs. Junction Temperature

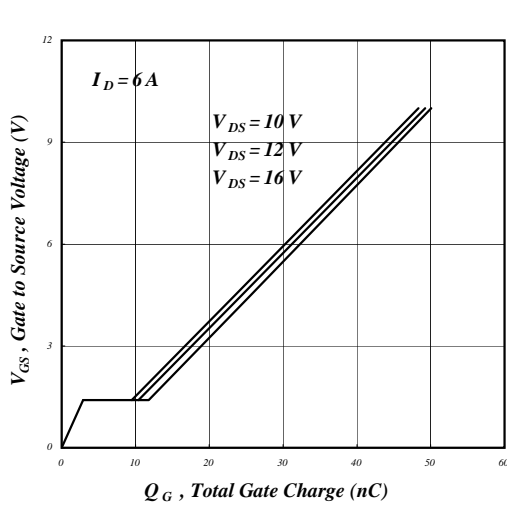


Fig 7. Gate Charge Characteristics

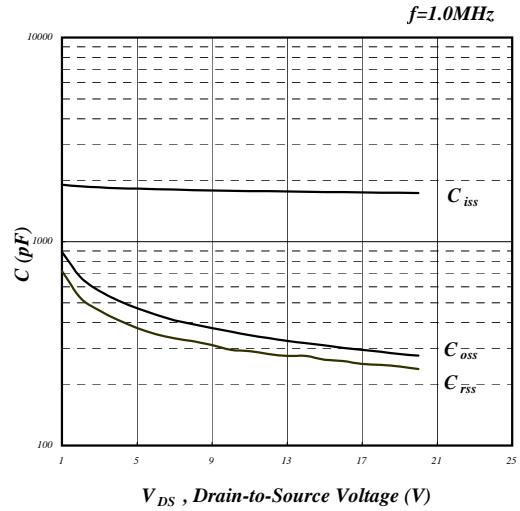


Fig 8. Typical Capacitance Characteristics

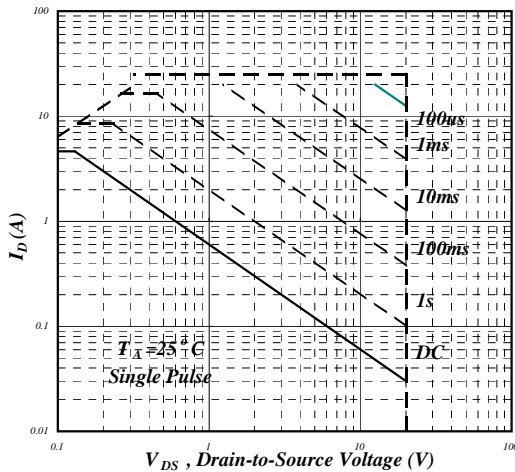


Fig 9. Maximum Safe Operating Area

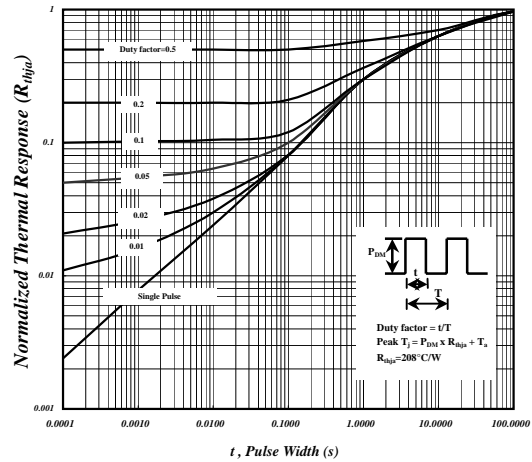


Fig 10. Effective Transient Thermal Impedance

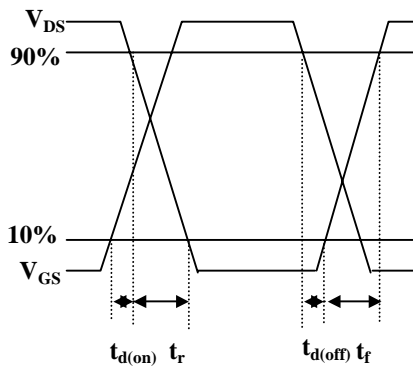


Fig 11. Switching Time Waveform

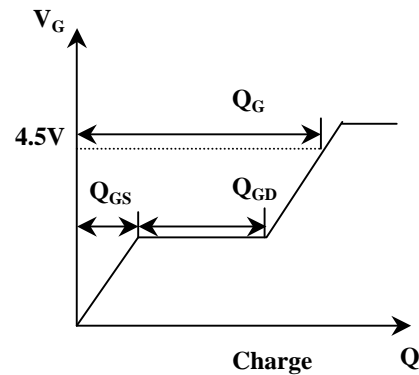


Fig 12. Gate Charge Waveform

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