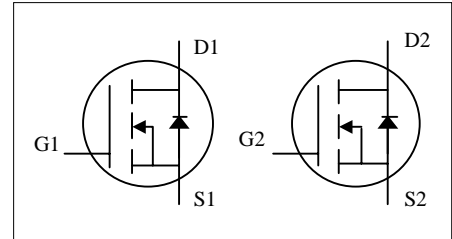


# N-CANNEL ENHANCEMENT MODE POWER MOSFET

## PRODUCT SUMMARY

- Low on-resistance
- Capable of 2.5V gate drive
- Low drive current
- Surface mount package

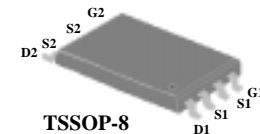


## DESCRIPTION

The Advanced Power MOSFETs from Silicon Standard Corp. provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.

$BV_{DSS}$	20V
$R_{DS(ON)}$	28m $\Omega$
$I_D$	4.6A

 **Pb-free; RoHS-compliant**



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating	Units
$V_{DS}$	Drain-Source Voltage	20	V
$V_{GS}$	Gate-Source Voltage		V
$I_D @ T_A=25^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	4.6	A
$I_D @ T_A=70^\circ\text{C}$	Continuous Drain Current <sup>3</sup>	3.7	A
$I_{DM}$	Pulsed Drain Current <sup>1</sup>	20	A
$P_D @ T_A=25^\circ\text{C}$	Total Power Dissipation	1	W
	Linear Derating Factor	0.008	W/ $^\circ\text{C}$
$T_{STG}$	Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$T_J$	Operating Junction Temperature Range	-55 to 150	$^\circ\text{C}$

## THERMAL DATA

Symbol	Parameter	Value	Unit
$R_{thj-a}$	Thermal Resistance Junction-ambient <sup>3</sup>	Max. 125	$^\circ\text{C}/\text{W}$

**ELECTRICAL CHARACTERISTICS @ $T_j=25^{\circ}\text{C}$  (unless otherwise specified)**

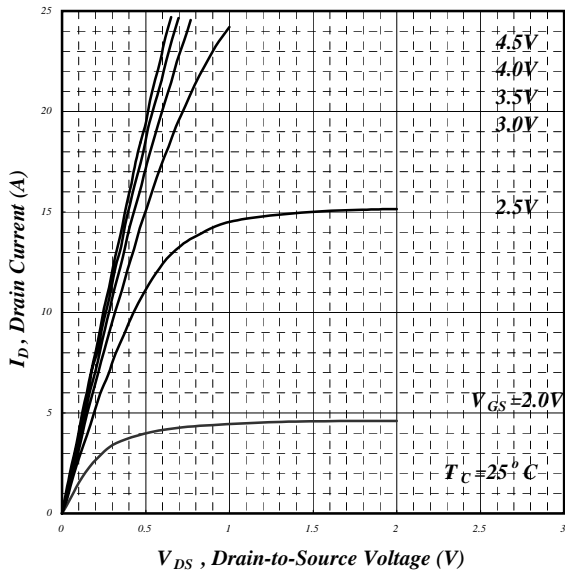
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=250\mu A$	20	-	-	V
$\Delta BV_{DSS}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to $25^{\circ}\text{C}, I_D=1\text{mA}$	-	0.1	-	$V/^{\circ}\text{C}$
$R_{DS(ON)}$	Static Drain-Source On-Resistance <sup>2</sup>	$V_{GS}=4.5V, I_D=4A$	-	23	28	$m\Omega$
		$V_{GS}=2.5V, I_D=2A$	-	-	40	$m\Omega$
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5	-	-	V
$g_{fs}$	Forward Transconductance	$V_{DS}=10V, I_D=4.6A$	-	9.7	-	S
$I_{DSS}$	Drain-Source Leakage Current ( $T_j=25^{\circ}\text{C}$ )	$V_{DS}=20V, V_{GS}=0V$	-	-	1	$\mu A$
	Drain-Source Leakage Current ( $T_j=70^{\circ}\text{C}$ )	$V_{DS}=20V, V_{GS}=0V$	-	-	25	$\mu A$
$I_{GSS}$	Gate-Source Leakage	$V_{GS}=\pm 8V$	-	-	$\pm 100$	nA
$Q_g$	Total Gate Charge <sup>2</sup>	$I_D=4.6A$	-	12.5	-	nC
$Q_{gs}$	Gate-Source Charge	$V_{DS}=20V$	-	1	-	nC
$Q_{gd}$	Gate-Drain ("Miller") Charge	$V_{GS}=5V$	-	6.5	-	nC
$t_{d(on)}$	Turn-on Delay Time <sup>2</sup>	$V_{DS}=10V$	-	7	-	ns
$t_r$	Rise Time	$I_D=1A$	-	14.5	-	ns
$t_{d(off)}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{GS}=5V$	-	19	-	ns
$t_f$	Fall Time	$R_D=10\Omega$	-	12	-	ns
$C_{iss}$	Input Capacitance	$V_{GS}=0V$	-	355	-	pF
$C_{oss}$	Output Capacitance	$V_{DS}=20V$	-	190	-	pF
$C_{rss}$	Reverse Transfer Capacitance	$f=1.0\text{MHz}$	-	85	-	pF

**SOURCE-DRAIN DIODE**

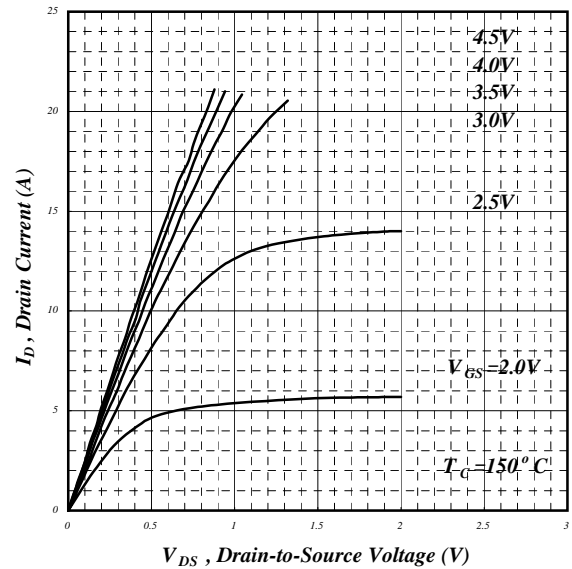
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$I_S$	Continuous Source Current ( Body Diode )	$V_D=V_G=0V, V_S=1.2V$	-	-	0.83	A
$V_{SD}$	Forward On Voltage <sup>2</sup>	$T_j=25^{\circ}\text{C}, I_S=1.25A, V_{GS}=0V$	-	-	1.2	V

**Notes:**

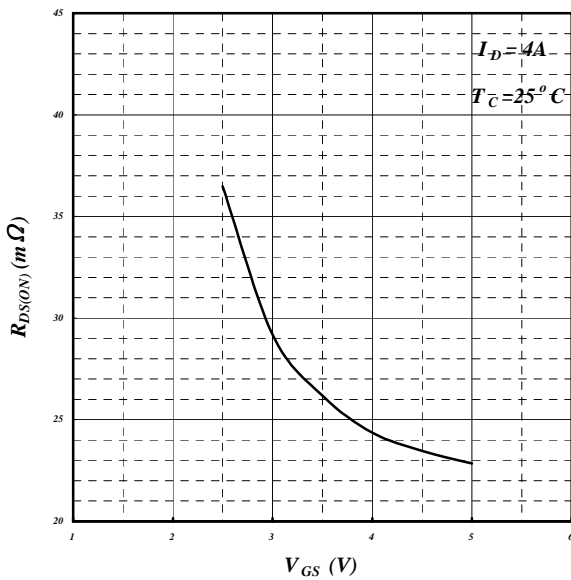
1. Pulse width limited by Max. junction temperature.
2. Pulse width  $\leq 300\mu s$ , duty cycle  $\leq 2\%$ .
3. Surface mounted on 1 in<sup>2</sup> copper pad of FR4 board ;  $208^{\circ}\text{C}/\text{W}$  when mounted on Min. copper pad.



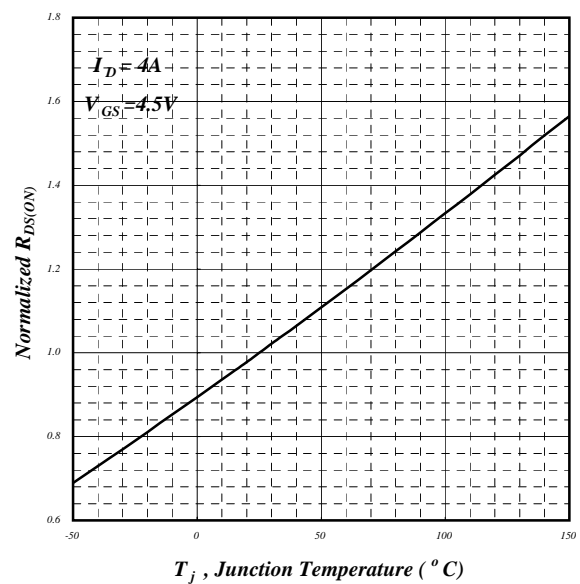
**Fig 1. Typical Output Characteristics**



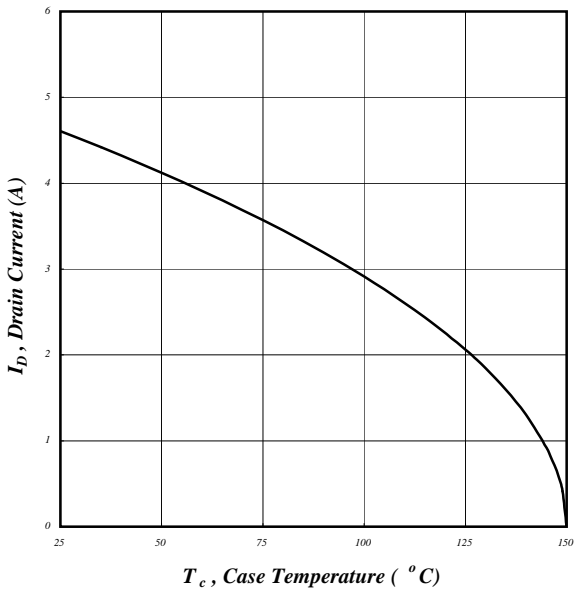
**Fig 2. Typical Output Characteristics**



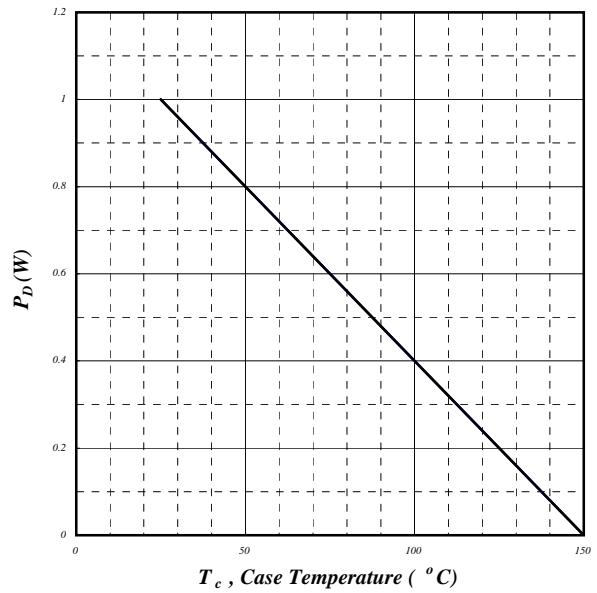
**Fig 3. On-Resistance v.s. Gate Voltage**



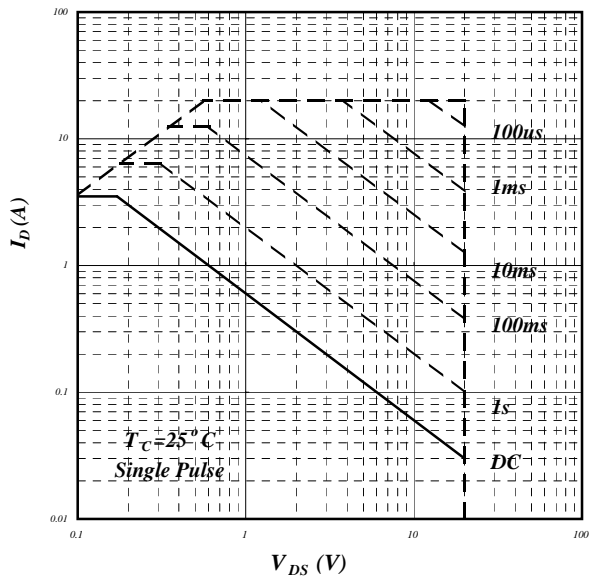
**Fig 4. Normalized On-Resistance v.s. Junction Temperature**



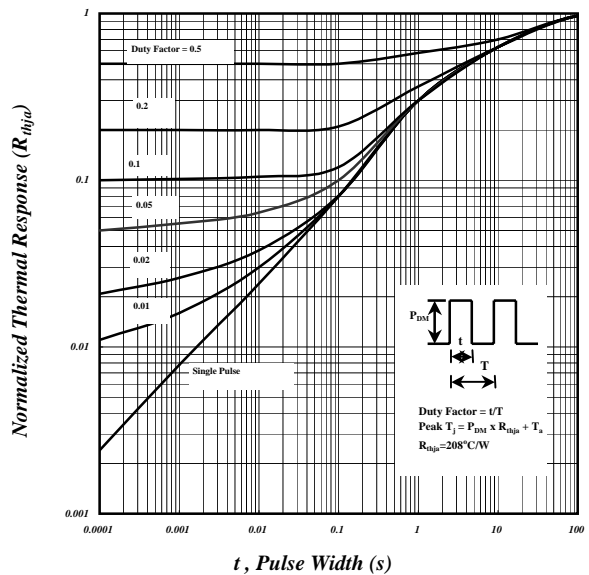
**Fig 5. Maximum Drain Current v.s. Case Temperature**



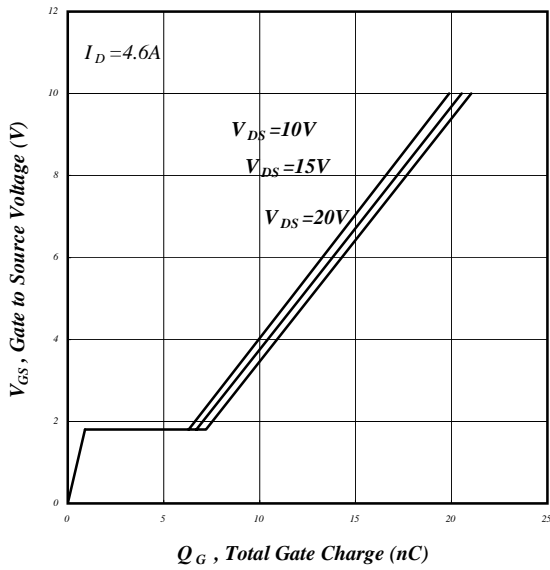
**Fig 6. Typical Power Dissipation**



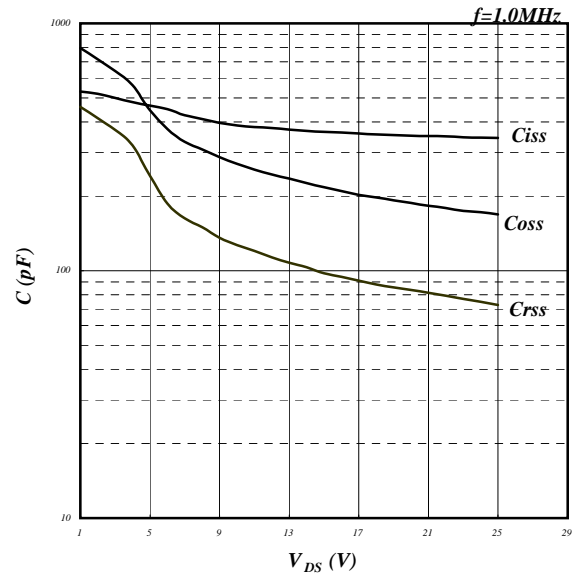
**Fig 7. Maximum Safe Operating Area**



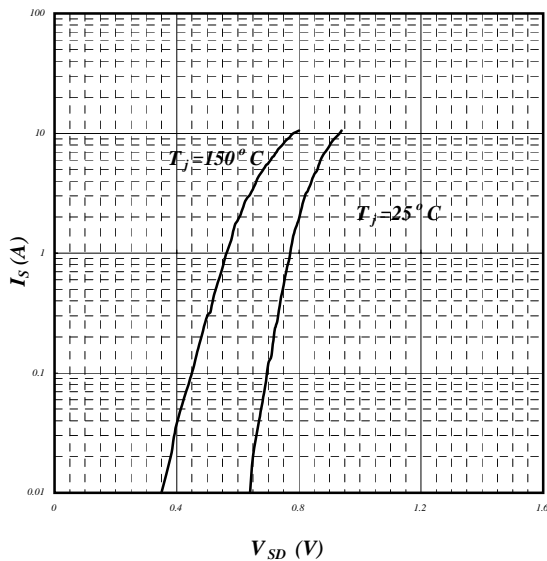
**Fig 8. Effective Transient Thermal Impedance**



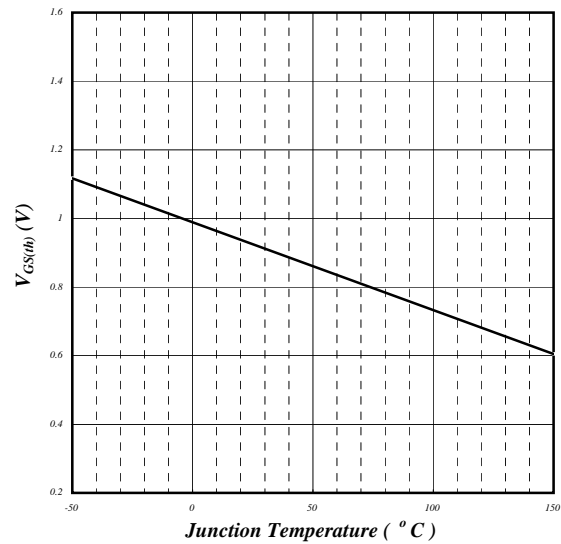
**Fig 9. Gate Charge Characteristics**



**Fig 10. Typical Capacitance Characteristics**



**Fig 11. Forward Characteristic of Reverse Diode**



**Fig 12. Gate Threshold Voltage v.s. Junction Temperature**

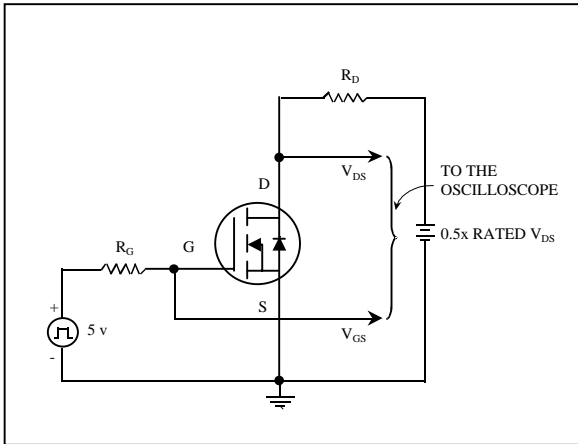


Fig 13. Switching Time Circuit

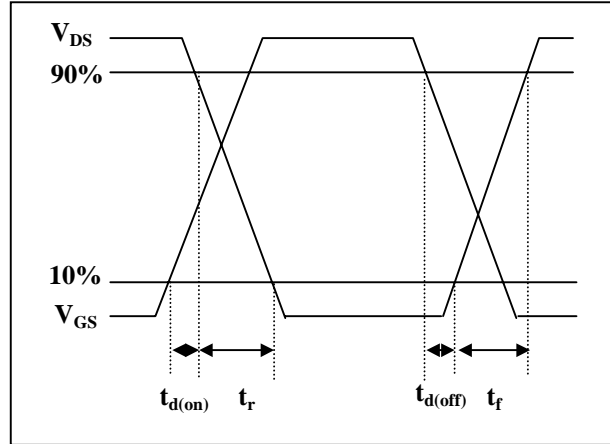


Fig 14. Switching Time Waveform

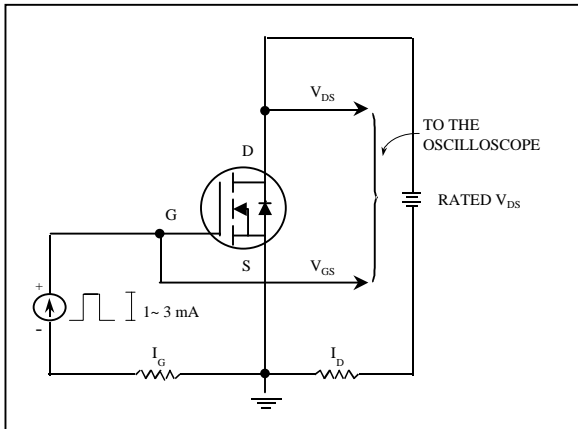


Fig 15. Gate Charge Circuit

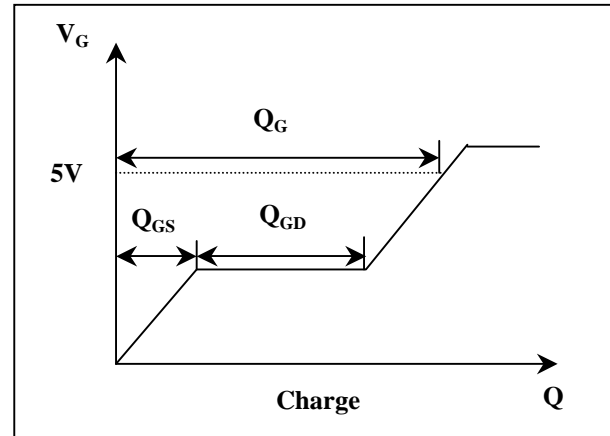


Fig 16. Gate Charge Waveform

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